MN38663S

NTSC-Compatible CCD Video Signal Delay Element

■ Overview

The MN38663S is a CCD signal delay element for video signal processing applications.

It contains such components as a threefold-frequency circuit, a shift register clock driver, charge I/O blocks, two CCD analog shift registers switchable between 680.5 and 605 stages, a clamp bias circuit, resampling output amplifiers, and booster circuits.

When the switch input is "L" level, the MN38663S samples the input using the supplied clock signal with a frequency of three times the NTSC color signal subcarrier frequency (3.579545 MHz) and, after adding in the attached filter delay, produces independent delays of 1 H (the horizontal scan period) each for the two lines. When the switch input is "H" level, the MN38663S disables the threefold-frequency circuit and samples the input with the image sensor drive frequency (9.545454 MHz) for the camera's 510 horizontal pixels and, after adding in the attached filter delay, produces independent delays of 1 H (the horizontal scan period) each for the two lines.

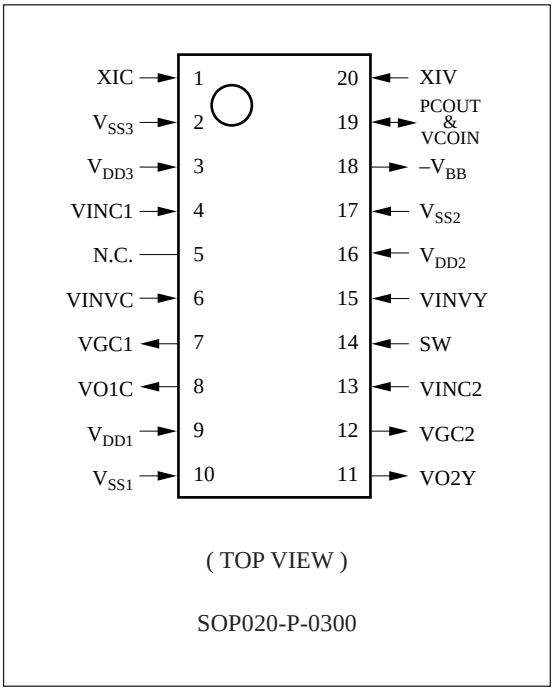
■ Features

- Single 4.4 V power supply
- Choice of camera and VCR modes, so that both the camera and VCR portions of a video camera with 510 horizontal pixels can use the same MN38663S for signal processing

■ Applications

- Video cameras

■ Pin Assignment



(TOP VIEW)

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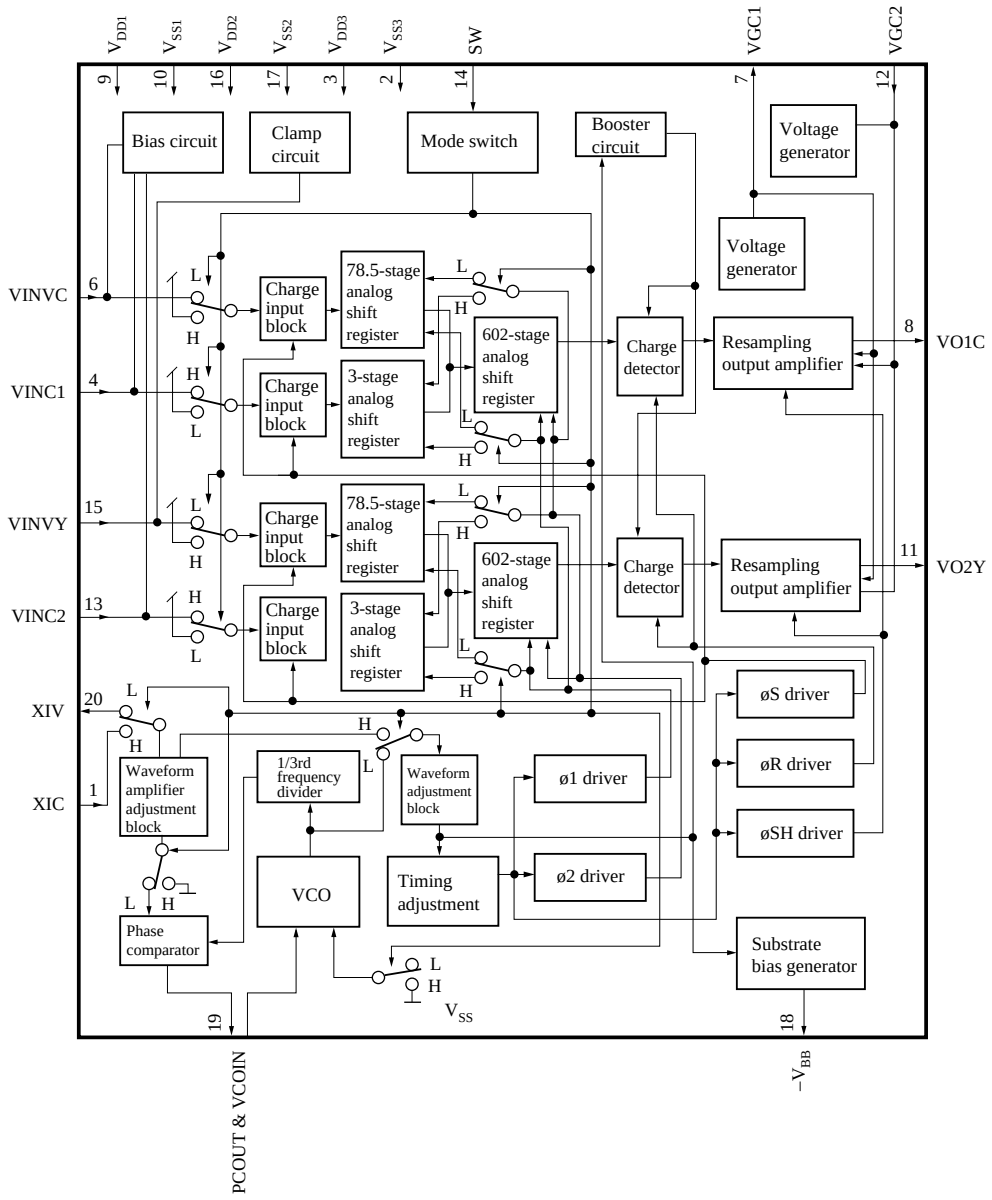
■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Pin Name	Function Description
1	XIC	9.545454 MHz clock input	
2	V_{SS3}	GND (3)	Ground for clock multiplier circuit
3	V_{DD3}	Power supply (3)	Power supply for clock multiplier circuit
4	VINC1	Camera signal input (1)	
5	N.C.	No connection	
6	VINVC	Video signal input (C)	
7	VGC1	Output gate connection (1)	
8	VO1C	Signal output (1C)	Output pin for signal fed to pin 4 or pin 6
9	V_{DD1}	Power supply (1)	Power supply for analog circuits
10	V_{SS1}	GND (1)	Ground for analog circuits
11	VO2Y	Signal output (2Y)	Output pin for signal fed to pin 13 or pin 15
12	VGC2	Output gate connection (2)	
13	VINC2	Power supply (2)	
14	SW	Camera/video mode switch	
15	VINVY	Video signal input (Y)	
16	V_{DD2}	Power supply (2)	Power supply for digital circuits other than frequency multiplier
17	V_{SS2}	GND (2)	Ground for digital circuits other than frequency multiplier
18	$-V_{BB}$	Substrate connection	Negative voltage pin
19	PCOUT&VCOIN	Phase comparator output and voltage controlled oscillator input	
20	XIV	3.579545 MHz clock input	

Notes

1: Always connect V_{DD1}, V_{DD2}, and V_{DD3} to the same voltage.

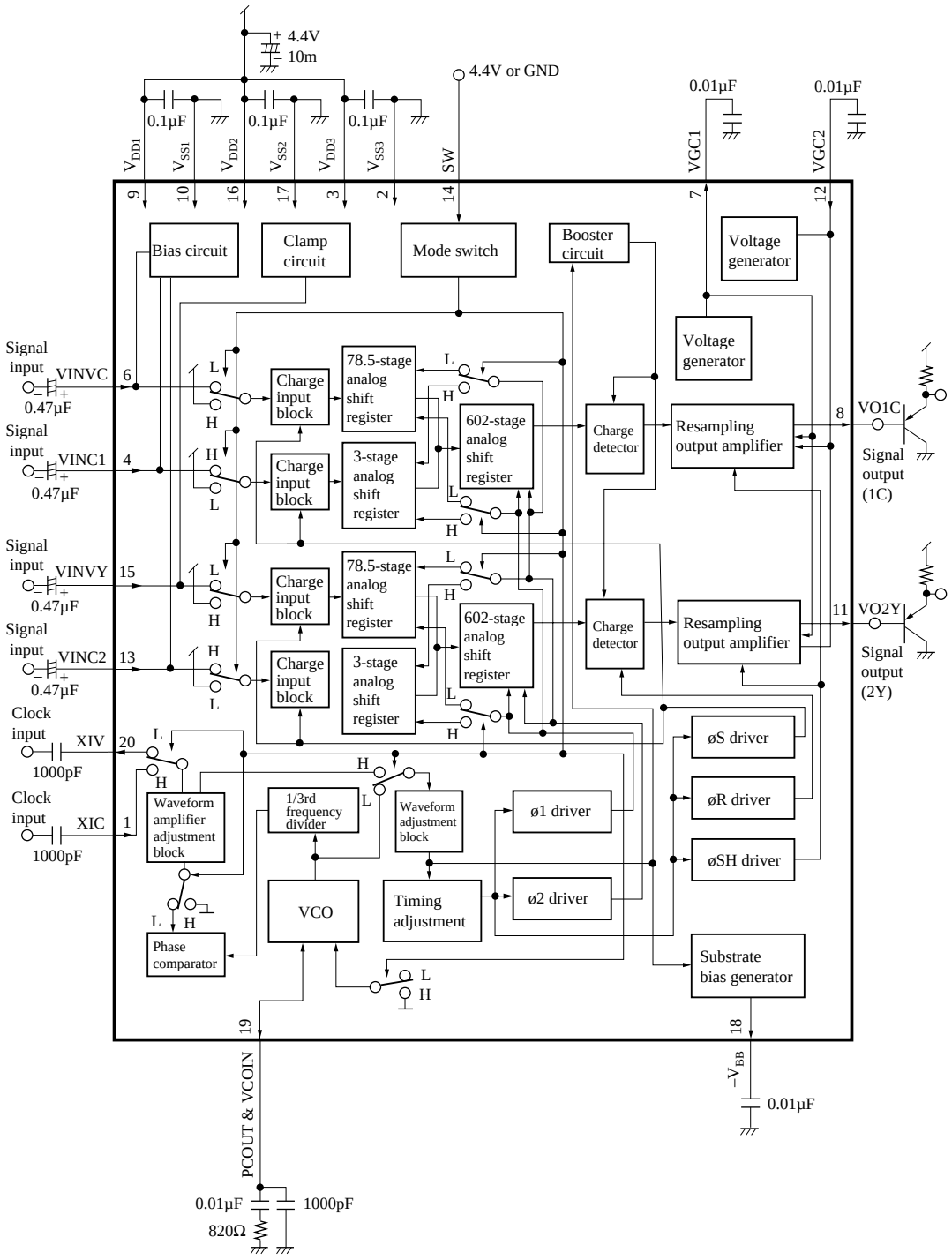
2: Always connect V_{SS1}, V_{SS2}, and V_{SS3} to ground.

■ Electrical Characteristics

V_{DD}=4.4V, V_{ckv}=0.3V_{P-P} (sine wave), f_{ckv}=3.579545MHz (Converted to 10.738635 MHz internally)
V_{ckc}=0.3V_{P-P} (sine wave), f_{ckc}=9.545454MHz, V_{in}=0.5V_{P-P} (sine wave), Ta=25˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply current (Video signal I/O)	I_{DDV}	Average current for 4.4-V power supply when SW is "L" level		30	48	mA
Power supply current (Camera signal I/O)	I_{DDC}	Average current for 4.4-V power supply when SW is "H" level		28	46	
Signal bandwidth (Video signal I/O)	BWV	–3 dB for 200 kHz value when SW is "L" level	3.0	4.2		MHz
Signal bandwidth (Camera signal I/O)	BWC	–3 dB for 200 kHz value when SW is "H" level	2.7	3.7		
Insertion gain	IG	f_{sig}=200kHz	1	4	7	dB
Total harmonic distortion	THD	f_{sig}=200kHz		1	4	%
Signal-to-noise ratio	S/N	Signal output (V_{P-P})/noise output (rms)	50	56		dB
Clock leak (V1)	NCV1	3.579545-MHz component output/main output signal when SW is "L" level		–50	–40	dB
Clock leak (C)	NCC	9.545454-MHz component output/main output signal when SW is "H" level		–15	–10	dB
Clock leak (V2)	NCV2	10.738635-MHz component output/main output signal when switch signal is "L" level		–15	–10	dB
Crosstalk	CT	f_{sig}=200kHz			–37	dB
Delay (Video signal I/O)	τ_{DV}	When SW is "L" level		63.40		μs
Delay (Camera signal I/O)	τ_{DC}	When SW is "H" level		63.42		
VO pin output impedance	ZO			350	700	Ω
Input bias voltage	V_{BINC}	Applicable to signal input pins VINC1 and VINC2	2.20	2.50	2.80	V
Input bias voltage	V_{BINY}	Applicable to signal input pin VINC1	2.10	2.40	2.70	V
Input clamp voltage	V_{CLIN}	Applicable to signal input pin VINVY	1.90	2.20	2.50	V
Output bias voltage	V_{BOC}	Applicable to signal output pins VO1C and VO2Y when SW is "H" level	1.30	2.30	3.30	V
Output bias voltage	V_{BOY}	Applicable to signal output pin VO1C when SW is "L" level	1.35	2.35	3.35	V
Output clamp voltage	V_{CLO}	Applicable to signal output pin VO2Y when SW is "L" level	1.05	2.05	3.05	V
Substrate voltage	$-V_{BB}$			–2.5		V

■ Application Circuit Example



Note: If the capacitor attached to pin 18 has a polarity, attach the negative pole to pin 18.

■ Package Dimensions (Unit:mm)

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