

TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF5G48, SF5J48, USF5G48, USF5J48

MEDIUM POWER CONTROL APPLICATIONS

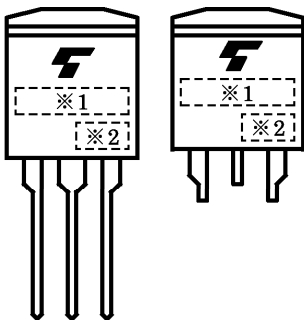
- Repetitive Peak Off-State Voltage : V_{DRM}
- Repetitive Peak Reverse Voltage : V_{RRM} } = 400, 600V
- Average On-State Current : $I_T(AV) = 5A$
- Gate Trigger Current : $I_{GT} = 10mA$ Max.

Unit in mm

SF5G48-SF5J48		USF5G48-USF5J48	
JEDEC	—	JEDEC	—
EIAJ	—	EIAJ	—
TOSHIBA	13-10J1B	TOSHIBA	13-10J2B

Weight : 1.7g

MARKING



※ 1	MARK	F5G48	TYPE NAME	SF5G48, USF5G48
		F5J48		SF5J48, USF5J48
※ 2	Lot Number			
	□ □	← Month (Starting from Alphabet A)		
		← Year (Last Decimal Digit of the Current Year)		

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MAXIMUM RATINGS

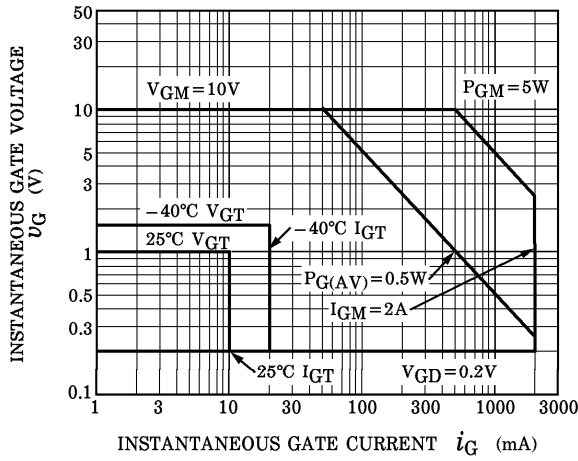
CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF5G48	V _{DRM}	400	V
	USF5G48			
	SF5J48	V _{R RM}	600	
	USF5J48			
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms T _j = 0~125°C)	SF5G48	V _{R SM}	500	V
	USF5G48			
	SF5J48	720		
	USF5J48			
Average On-State Current		I _{T (AV)}	5	A
R.M.S On-State Current		I _{T (RMS)}	7.8	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I _{T SM}	80 (50Hz)	A
			88 (60Hz)	
I ² t Limit Value		I ² t	32	A ² s
Critical Rate of Rise of On-State Current (Note 1)		di / dt	100	A / μs
Peak Gate Power Dissipation		P _{GM}	5	W
Average Gate Power Dissipation		P _{G (AV)}	0.5	W
Peak Forward Gate Voltage		V _{FGM}	10	V
Peak Reverse Gate Voltage		V _{RGM}	-5	V
Peak Forward Gate Current		I _{GM}	2	A
Junction Temperature		T _j	-40~125	°C
Strage Temperature Range		T _{stg}	-40~125	°C

(Note 1) : V_{DRM} = 0.5 × Rated
 I_{TM} ≤ 15A
 t_{gw} ≥ 10 μs
 t_{gr} ≤ 250ns
 i_{gp} = I_{GT} × 2.0

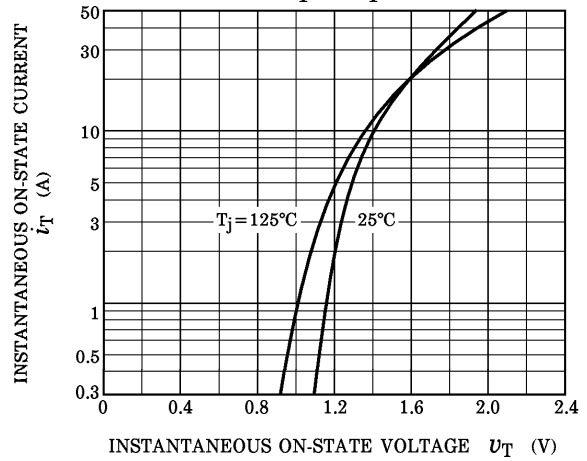
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse	I _{DRM} I _{RRM}	V _{DRM} = V _{R RM} = Rated	—	—	10	μA
Peak On-State Voltage	V _{TM}	I _{TM} = 15A	—	—	1.5	V
Gate Trigger Voltage	V _{GT}	V _D = 6V, R _L = 10Ω	—	—	1.0	V
Gate Trigger Current	I _{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V _{GD}	V _D = Rated × 2 / 3, T _c = 125°C	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv / dt	V _{DRM} = Rated, T _c = 125°C Exponential Rise	—	50	—	V / μs
Holding Current	I _H	V _D = 6V, I _{TM} = 1A	—	—	40	mA
Latching Current	I _L	V _D = 6V, f = 50Hz t _{gw} = 50 μs, i _G = 30mA	—	—	50	mA
Thermal Resistance	R _{th(j-c)}	Junction to Case, DC	—	—	3.2	°C / W

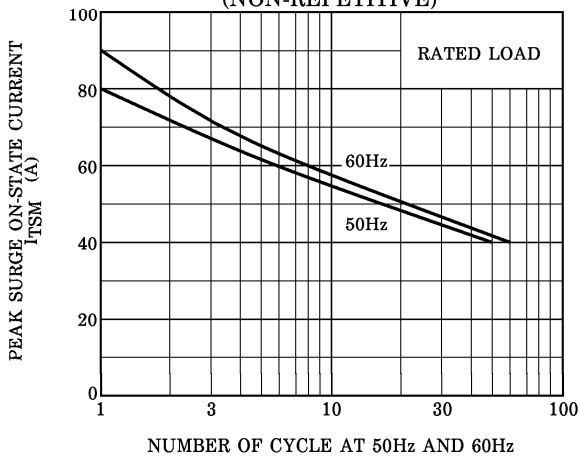
GATE TRIGGER CHARACTERISTIC



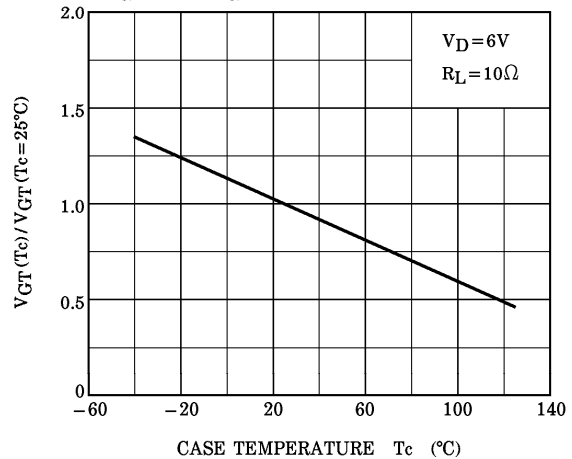
$i_T - v_T$



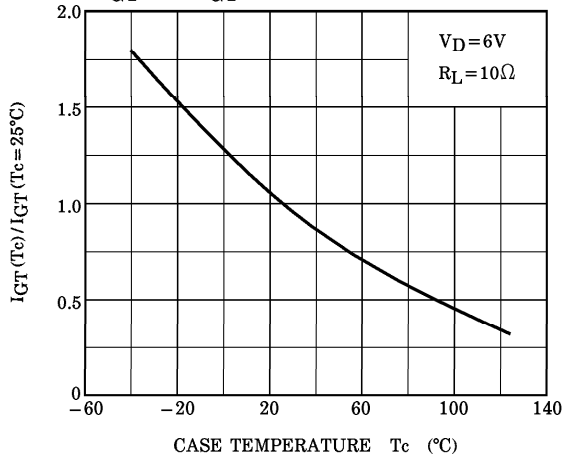
SURGE ON-STATE CURRENT (NON-REPETITIVE)



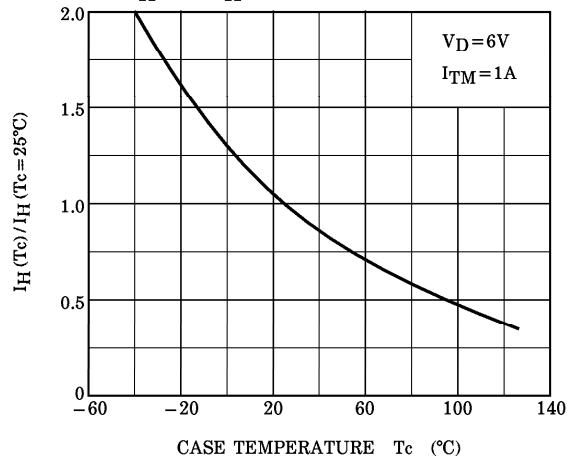
$V_{GT}(T_c) / V_{GT}(T_c=25^\circ C) - T_c$ (TYPICAL)

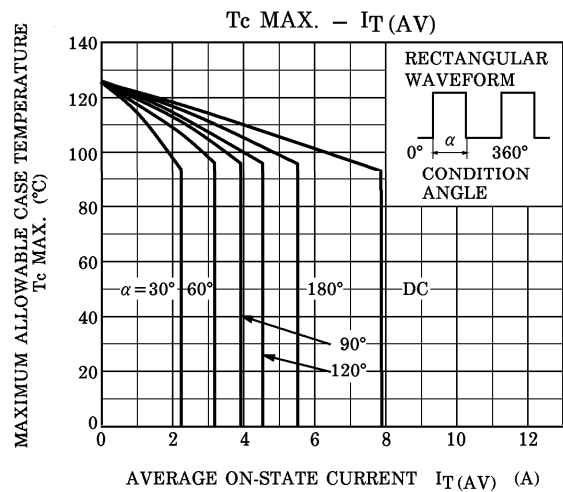
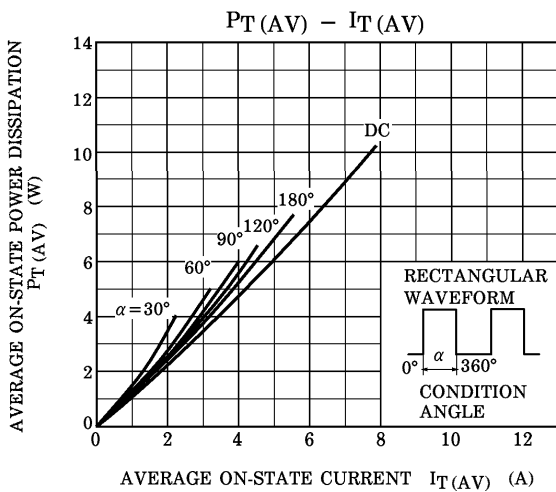
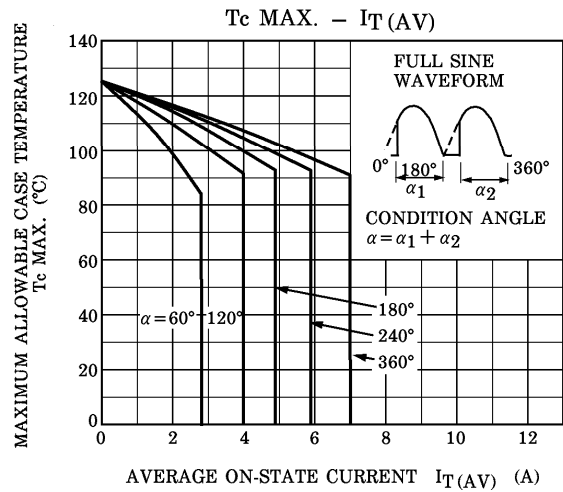
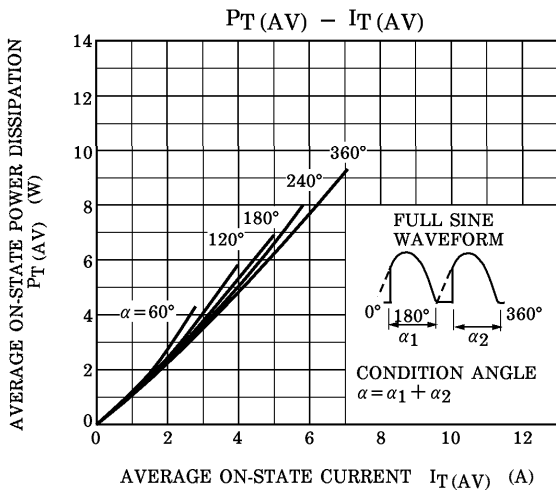
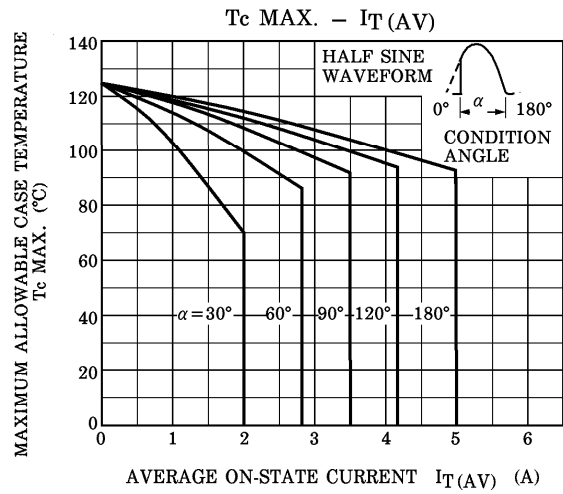
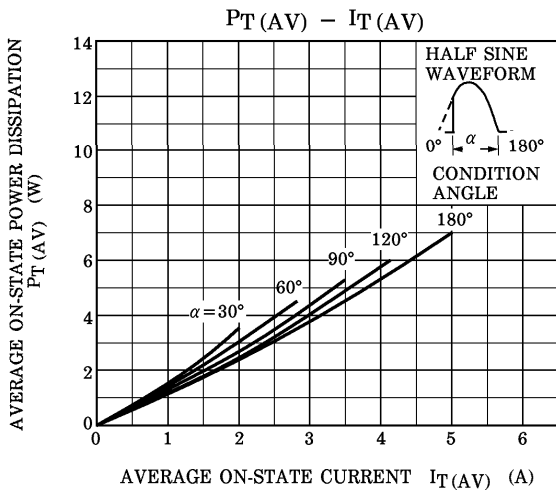


$I_{GT}(T_c) / I_{GT}(T_c=25^\circ C) - T_c$ (TYPICAL)

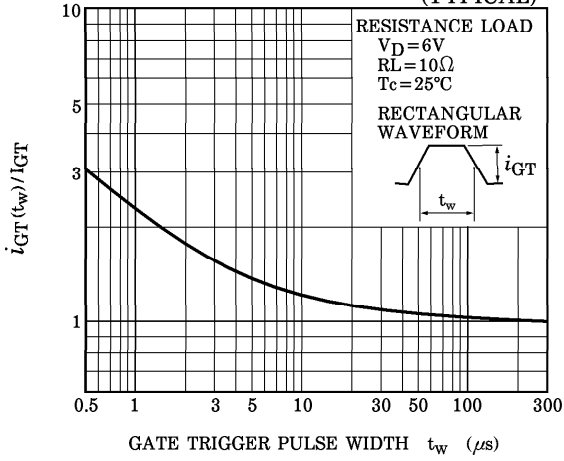


$I_H(T_c) / I_H(T_c=25^\circ C) - T_c$ (TYPICAL)





**PULSE TRIGGER CHARACTERISTIC
(TYPICAL)**



**TRANSIENT THERMAL IMPEDANCE
(JUNCTION TO CASE)**

