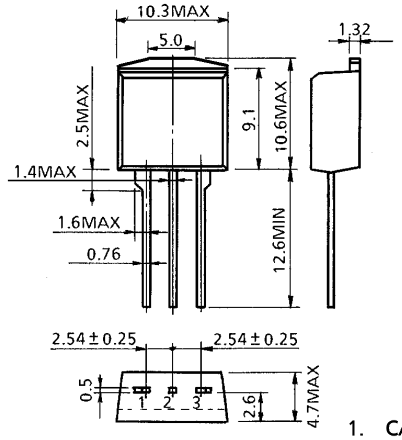
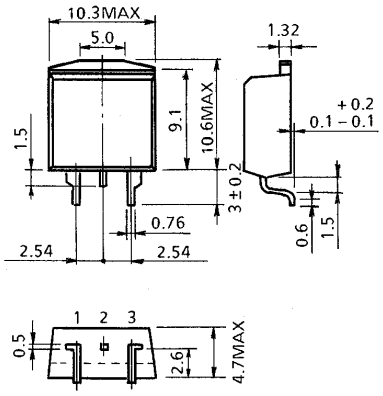
TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF5G48, SF5J48, USF5G48, USF5J48

MEDIUM POWER CONTROL APPLICATIONS

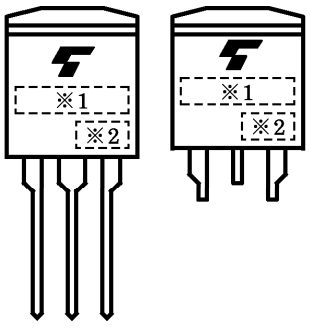
- Repetitive Peak Off-State Voltage : V_{DRM}
  Repetitive Peak Reverse Voltage : VRRM
  } =400, 600V
- Average On-State Current : $I_{T(AV)}$=5A
- Gate Trigger Current : I_{GT}=10mA Max.

Unit in mm

SF5G48·SF5J48	USF5G48·USF5J48
 1. CATHODE 2. ANODE 3. GATE	 1. CATHODE 2. ANODE (BACK SIDE) 3. GATE
JEDEC —	JEDEC —
EIAJ —	EIAJ —
TOSHIBA 13-10J1B	TOSHIBA 13-10J2B

Weight : 1.7g

MARKING



※ 1	MARK	F5G48	TYPE NAME	SF5G48, USF5G48
		F5J48		SF5J48, USF5J48
※ 2	Lot Number □□ ← Month (Starting from Alphabet A) Year (Last Decimal Digit of the Current Year)			

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MAXIMUM RATINGS

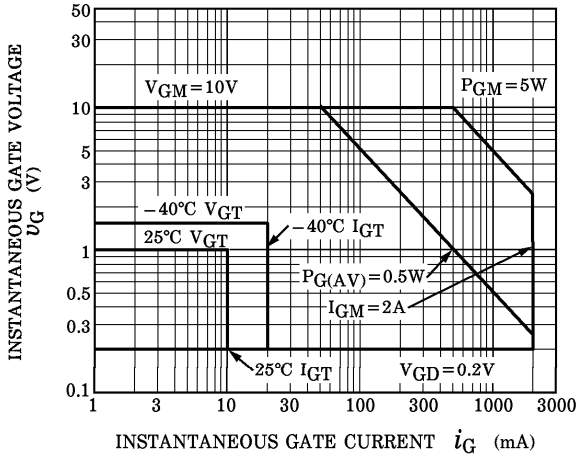
CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF5G48	V_{DRM} V_{RRM}	400	V
	USF5G48			
	SF5J48		600	
	USF5J48			
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms T_j = 0~125°C)	SF5G48	V_{RSM}	500	V
	USF5G48			
	SF5J48		720	
	USF5J48			
Average On-State Current		$I_{T(AV)}$	5	A
R.M.S On-State Current		$I_{T(RMS)}$	7.8	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I_{TSM}	80 (50Hz)	A
			88 (60Hz)	
I^2t Limit Value		I^2t	32	A^2s
Critical Rate of Rise of On-State Current (Note 1)		di/dt	100	A/μs
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissition		$P_{G(AV)}$	0.5	W
Peak Forward Gate Voltage		V_{FGM}	10	V
Peak Reverse Gate Voltage		V_{RGM}	−5	V
Peak Forward Gate Current		I_{GM}	2	A
Junction Temperature		T_j	−40~125	°C
Strage Temperature Range		T_{stg}	−40~125	°C

(Note 1) : V_{DRM} = 0.5 × Rated
$I_{TM} \leqq 15A$
$t_{gw} \geqq 10\mu s$
$t_{gr} \leqq 250ns$
$i_{gp} = I_{GT} \times 2.0$

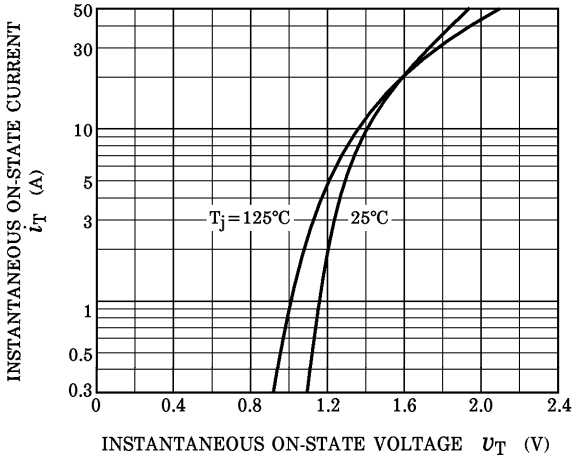
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse	I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$ = Rated	—	—	10	μA
Peak On-State Voltage	V_{TM}	I_{TM} = 15A	—	—	1.5	V
Gate Trigger Voltage	V_{GT}	V_D = 6V, R_L = 10Ω	—	—	1.0	V
Gate Trigger Current	I_{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V_{GD}	V_D = Rated × 2/3, Tc = 125°C	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv/dt	V_{DRM} = Rated, Tc = 125°C Exponential Rise	—	50	—	V/μs
Holding Current	I_H	V_D = 6V, I_{TM} = 1A	—	—	40	mA
Latching Current	I_L	V_D = 6V, f = 50Hz t_{gw} = 50μs, i_G = 30mA	—	—	50	mA
Thermal Resistance	$R_{th(j-c)}$	Junction to Case, DC	—	—	3.2	°C/W

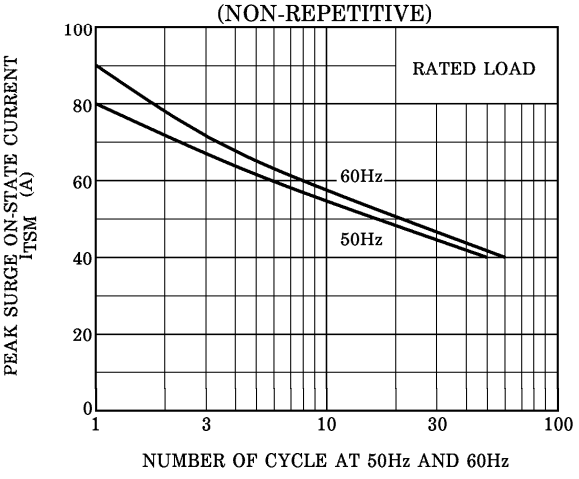
GATE TRIGGER CHARACTERISTIC



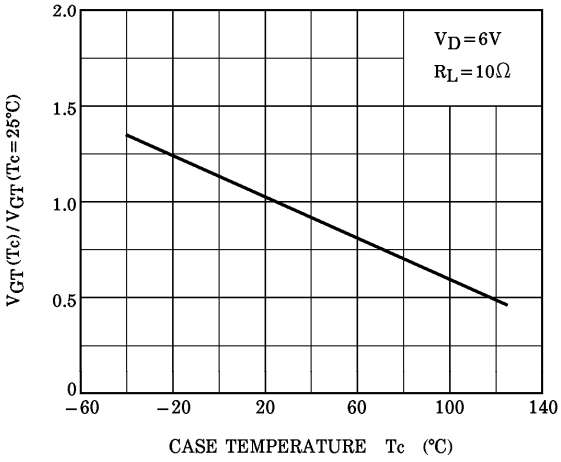
i_T – v_T



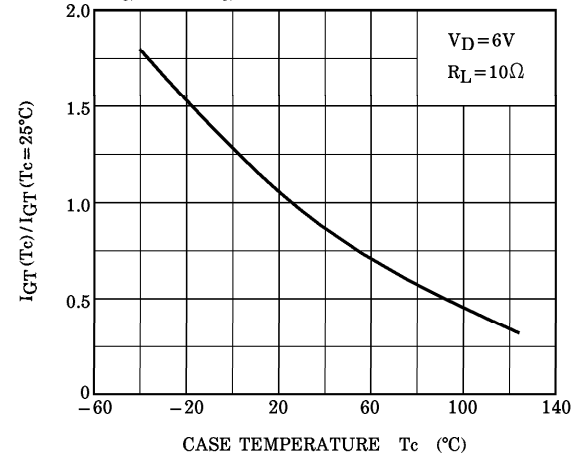
SURGE ON-STATE CURRENT
(NON-REPETITIVE)



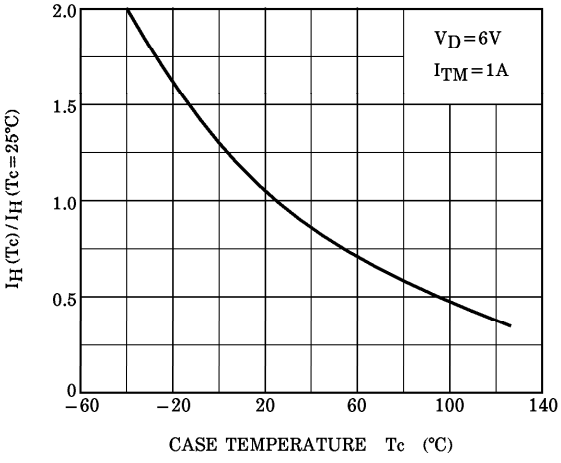
V_{GT} (Tc) / V_{GT} (Tc=25°C) – Tc (TYPICAL)



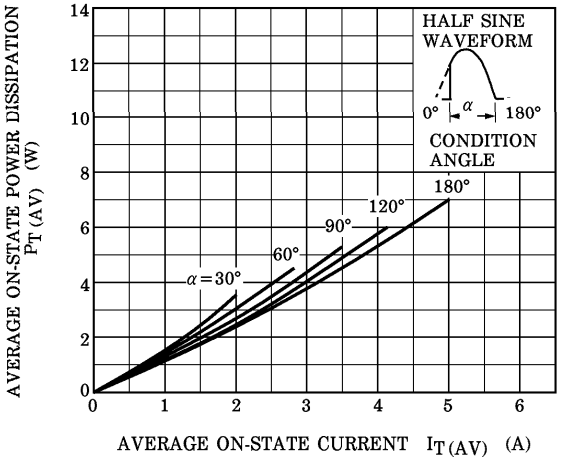
I_{GT} (Tc) / I_{GT} (Tc=25°C) – Tc (TYPICAL)



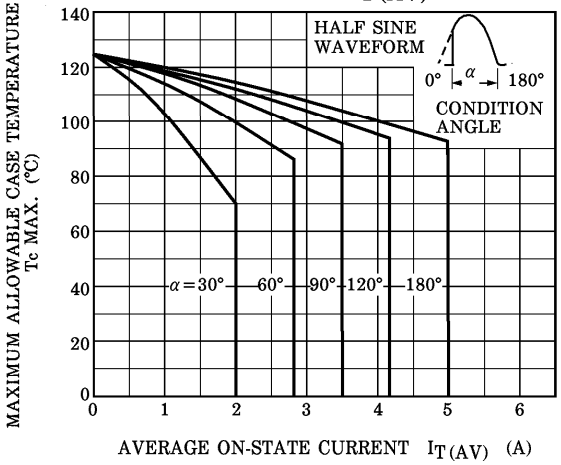
I_H (Tc) / I_H (Tc=25°C) – Tc (TYPICAL)



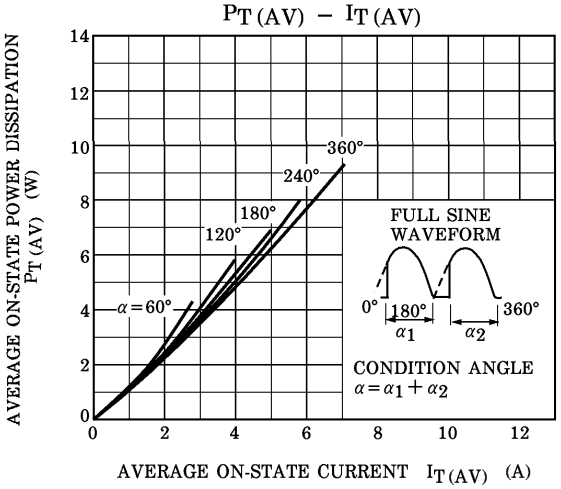
$P_{T(AV)}$ – $I_{T(AV)}$



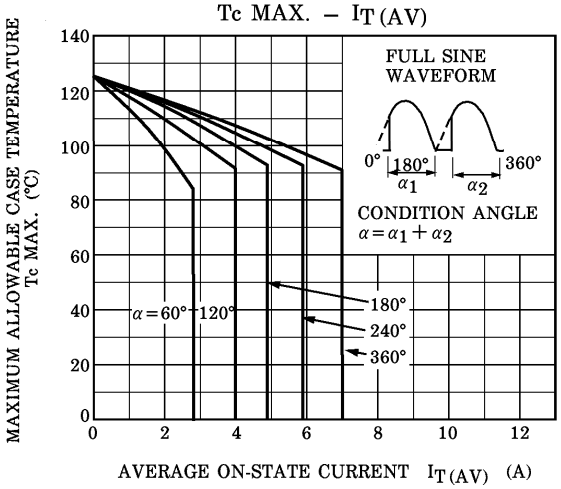
T_c MAX. – $I_{T(AV)}$



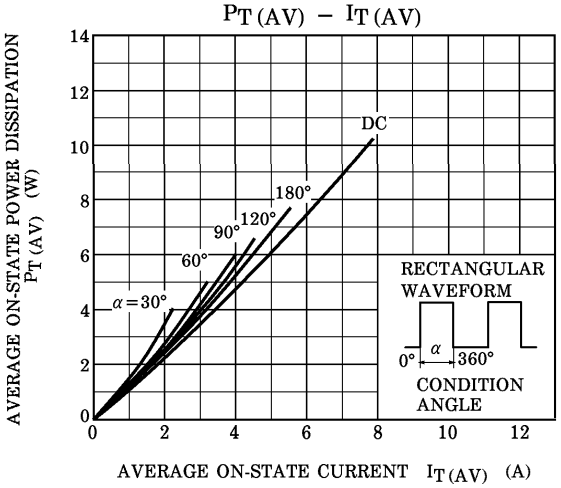
$P_{T(AV)}$ – $I_{T(AV)}$



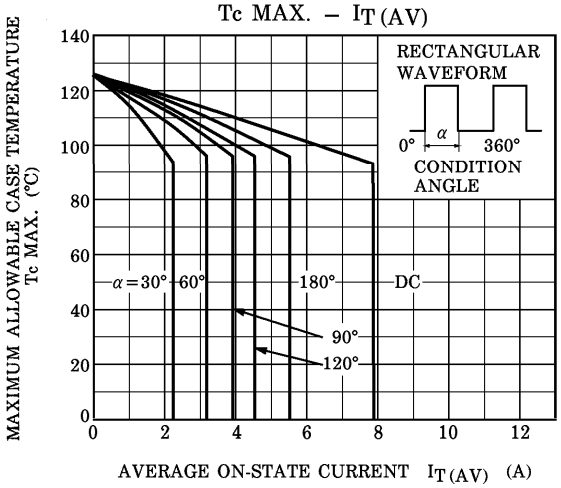
T_c MAX. – $I_{T(AV)}$



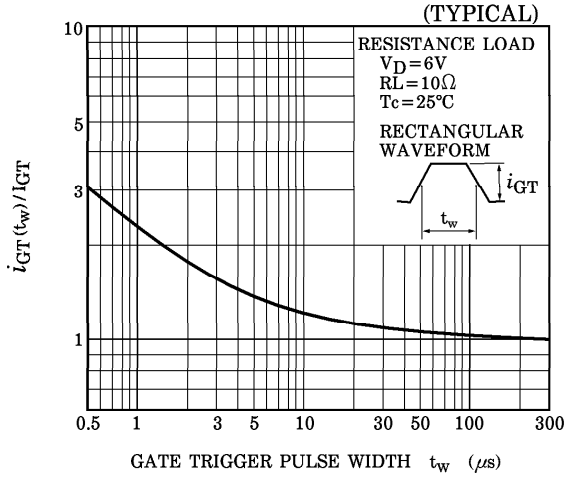
$P_{T(AV)}$ – $I_{T(AV)}$



T_c MAX. – $I_{T(AV)}$



PULSE TRIGGER CHARACTERISTIC
(TYPICAL)



TRANSIENT THERMAL IMPEDANCE
(JUNCTION TO CASE)