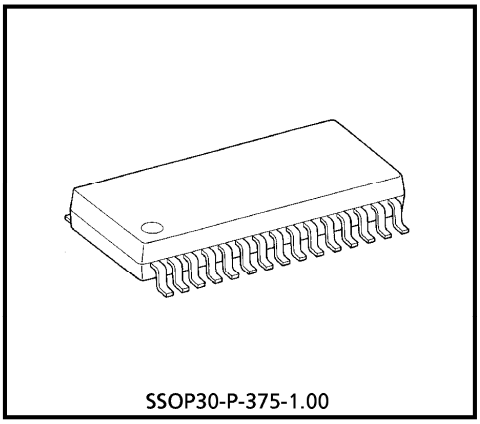
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB2104F

VFD DRIVER

The TB2104F is a VFD (fluorescent display tube) driver IC implemented by the Bi-CMOS process.
The logic section is configured with CMOS transistors, and the high voltage tolerant output driver section is configured with bipolar transistors.



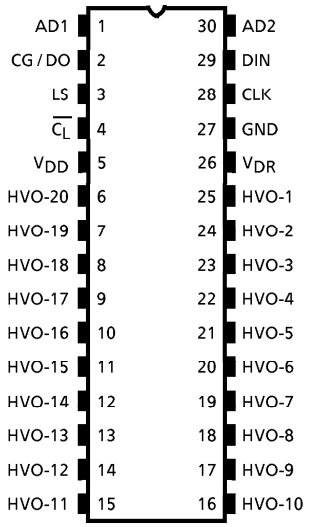
SSOP30-P-375-1.00

Weight : 0.7g (Typ.)

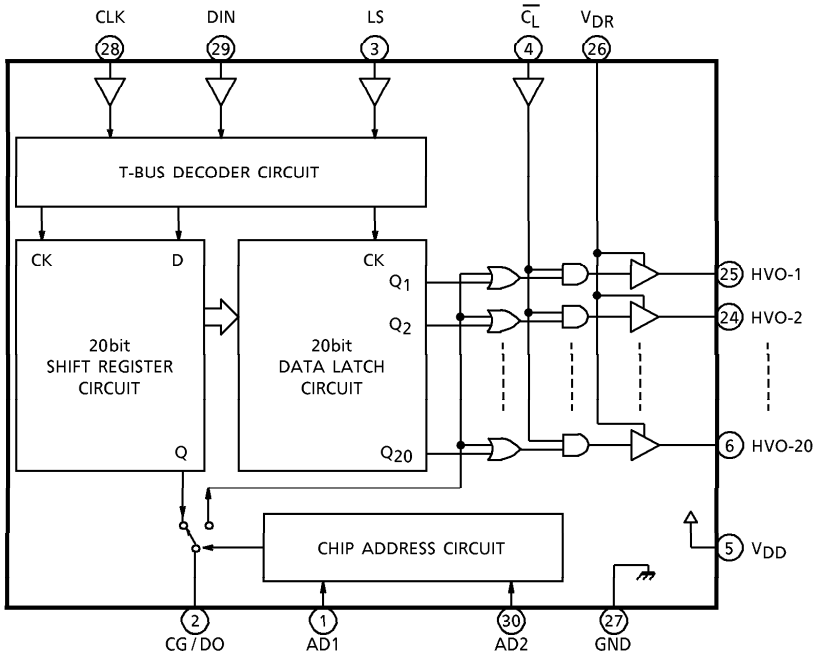
FEATURES

- Incorporates a shift register, latch, and driver capable of handling 20 bits of data.
- The output driver comes with an active pull-down, so it can function as a VFD grid, anode driver.
- Three serial data lines are used to input display data.
- The data receiver section can also accept general-purpose serial data and T-BUS (Toshiba Semiconductor Bus).
- In serial data mode, multiple drivers can be cascaded to expand the handling capacity in 20bit increments.

PIN CONNECTION



BLOCK DIAGRAM



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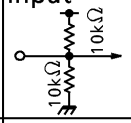
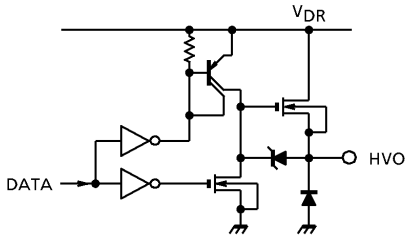
PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1 30	AD1 AD2	Address Setting Input	● Chip select / address setting inputs ● When using in Serial Mode, keep AD1 and AD2 "Open". ● In other settings than "Open", it becomes T-BUS Mode and addresses up to 8 kinds can be set.	3-value input 
3 28 29	LS CLK DIN	Strobe Input Clock Input Data Input	● Serial data input terminals ● Inputs display data through the DIN terminal synchronizing with rise of CLK input. ● Display data are updated when inputting "H" level into LS terminal after completing data input. ● In T-BUS Mode, LS terminal becomes "PERIOD" input.	CMOS Input
2	CG / DO	Lamp Test Input and Data Output	● Lamp test input terminal and data output terminal ● In Serial Mode (AD1 = AD2 = Open), this terminal serves as the serial data output terminal and enables cascade connection of driver IC. ● In T-BUS Mode, this terminal serves as the lamp test input and is able to use all the driver outputs (HVO-1 ~ –20) at "H" level by inputting "H" level signal. ● During the normal operation in T-BUS Mode, use this terminal by fixing at "L" level.	CMOS Input / CMOS Output built in pull-down resistor 20kΩ
4	$\overline{C_L}$	Clear Input	● Driver OFF (blanking) input terminal ● All the driver outputs are fixed at "L" level when "L" level signal is input. ● When "H" level signal is input, it becomes the normal mode.	CMOS Input built in pull-up resistor 20kΩ
5 26 27	V_{DD} V_{DR} GND	Logic Unit Power Supply Drive Unit Power Supply Ground	● Power supply and GND terminals	—
25 24 23 ⋮ 8 7 6	HVO-1 HVO-2 HVO-3 ⋮ HVO-18 HVO-19 HVO-20	Driver Output	● High-tension driver output terminal ● Equivalent circuit 	—

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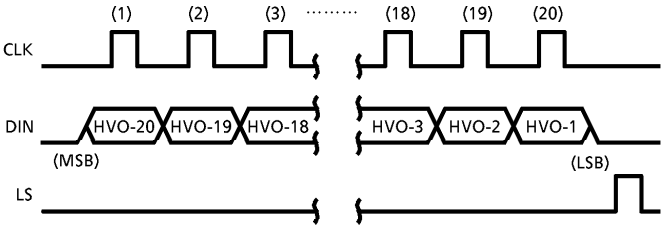
EXPLANATION OF OPERATION

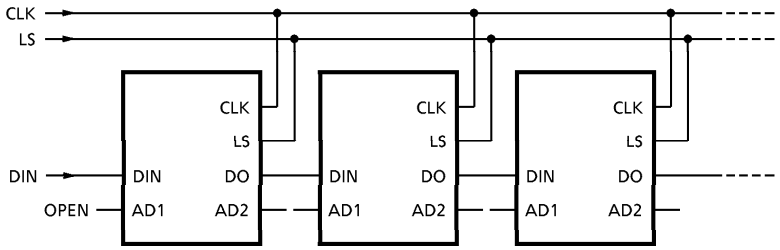
1. Serial data receiver circuit

- The serial data receiver circuit can be changed over to operate in the serial mode or the T-BUS Mode by switching, the AD1 / AD2 terminals.
- In T-BUS Mode, the AD1 / AD2 terminals become the chip select code inputs and it becomes possible to connect up to 8 drivers on the same bus line.

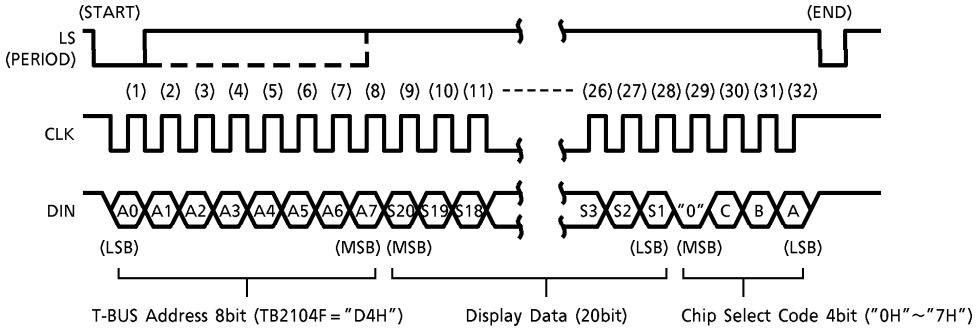
1) Input data format in serial data mode (AD1 = AD2 = "Open")



- Display data are updated when data for 20 bits are input from MSB side (HVO-20), synchronizing with rise of CLK signal and LS input is set to "H" level after inputting data.
- When increasing driver ICs, connect them through cascade connection as shown below :



2. Input data format in T-BUS Mode



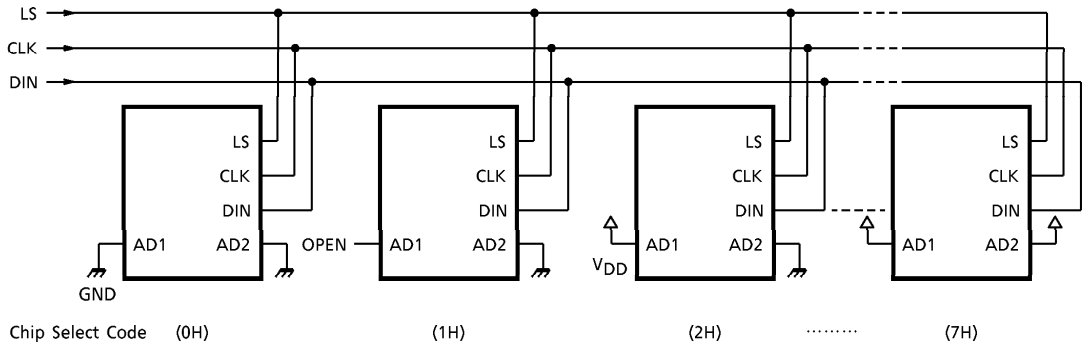
- In T-BUS Mode, start data transmission with the LS terminal (PERIOD) set at "L" level. Thereafter, send address data 8 bits, display data 20 bits, and chip select code 4 bits, synchronizing with rise of CLK signal.
- After sending data, set the LS terminal to "L" level again and terminate the data sending.
- On a driver IC when chip select code agrees with chip select code by AD1 / AD2, display data are updated at fall of LS signal.
- When increasing driver ICs, it is possible to connect up to 8 ICs on the same bus line in combination with AD1 / AD2.
- T-BUS address of the TB2104F is "D4H".
- When data are transferred using T-BUS address "00H", the data can be input to all the driver ICs on the bus line independently of chip select codes ("0H"~"7H"). (This function can be used for Power On reset.)

3. AD1 / AD2 input and chip select codes

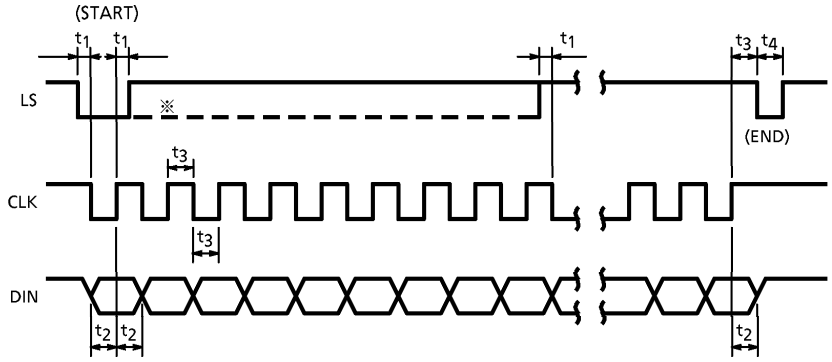
AD1 / AD2 input are 3-value level inputs and 9 kinds (3×3) of codes can be set.

AD1	AD2	A	B	C	CHIP SELECT CODE	MODE
V_{IH}	V_{IH}	1	1	1	"7H"	T-BUS
V_{IM}		0	1	1	"6H"	
V_{IL}		1	0	1	"5H"	
V_{IH}	V_{IM}	0	0	1	"4H"	
V_{IM}		—	—	—	—	Serial
V_{IL}		1	1	0	"3H"	T-BUS
V_{IH}	V_{IL}	0	1	0	"2H"	
V_{IM}		1	0	0	"1H"	
V_{IL}		0	0	0	"0H"	

4. Example of extension of driver ICs in T-BUS Mode chip select code



5. T-BUS Mode timing chart



- $f_{CLK} \leqq 500kHz$
- $t_1 \geqq 0.2\mu s$, $t_2 \geqq 0.2\mu s$
- $t_3 \geqq 1.0\mu s$, $t_4 \geqq 1.0\mu s$

Cautions for use

- Therefore, multiple driver outputs may possibly become "H" level simultaneously after the power is turned ON.
  (In this case, the allowable power dissipation of a device using this IC may possible be exceeded, destroying the device.)
- In order to avoid this, while keeping the clear terminal ($\overline{C_L}$) at "L" level, rise the power supply for the logic unit (V_{DD}) and then, that for the drivers (V_{DR}), reset all the contents of the data latch ("L" level) by serial data, and initialize the driver outputs.

MAXIMUM RATINGS (Ta = 25°C)

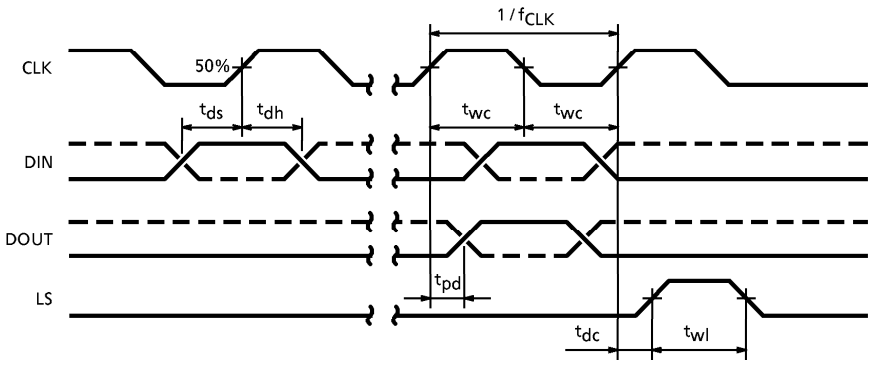
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Driver Voltage	V_{DR}	V_{DD}~60	V
Driver Current	I_{DR}	50	mA
Power Dissipation	P_D (Note)	800	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) In case it is used at more than Ta = 25°C, it is considered by reducing 6.4mW each 1°C.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{DD} = 5V, V_{DR} = 50V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V_{DD}	—	Logic unit		4.5	5.0	5.5	V
Operating Supply Voltage (2)		V_{DR}	—	Driver unit		10	~	50	V
Operating Supply Current (1)		I_{DD}	—	No load, No input		—	0.3	1.5	mA
Operating Supply Current (2)		I_{DR}	—	No load, Output V_{OL} level		—	2.3	3.5	mA
Input Voltage	"H" Level	V_{IH} (1)	—	CMOS input terminal DIN, CLK, LS, CG, $\overline{CL}$		V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL} (1)				GND	~	V_{DD} × 0.3	
Input Voltage	"H" Level	V_{IH} (2)	—	3-value input terminal AD1, AD2		V_{DD} − 0.5	~	V_{DD}	V
	Open	V_{IM}				—	V_{DD} × 0.5	—	
	"L" Level	V_{IL} (2)				GND	~	GND + 0.5	
Input Current	"H" Level	I_{IH}	—	CMOS input terminal	V_{IH} = 5V	− 1.0	~	1.0	μA
	"L" Level	I_{IL}			V_{IL} = 0V	− 1.0	~	1.0	
Input Resistance		R_{IN}	—	3-value input terminal		80	100	120	kΩ
Output Current	"H" Level	I_{OH} (1)	—	HVO-1~ − 20 Output terminal	V_{OH} = 45V	—	− 8.4	− 5	mA
	"L" Level	I_{OL} (1)			V_{OL} = 3V	2.0	2.7	—	
Output Current	"H" Level	I_{OH} (2)	—	DO output terminal	V_{OH} = 4V	—	− 0.3	− 0.1	mA
	"L" Level	I_{OL} (2)			V_{OL} = 1V	0.1	0.3	—	
Clock Frequency		f_{CLK}	Fig.1	CLK max. operating		—	5.0	4.0	MHz
Clock Pulse Width		t_{wc}		CLK min. operating		75	60	—	ns
Data Setup Time		t_{ds}		DIN min. operating pulse width		50	40	—	ns
Data Hold Time		t_{dh}				50	40	—	ns
LS Pulse Width		t_{wl}		LS min. operating		80	60	—	ns
CLK-LS Delay Time		t_{dc}		CLK→LS delay time		50	40	—	ns
CLK-DOUT Delay Time		t_{pd}		CLK→DOUT delay time CL = 30pF		—	120	160	ns

Fig.1 : Serial data timing chart



OUTLINE DRAWING

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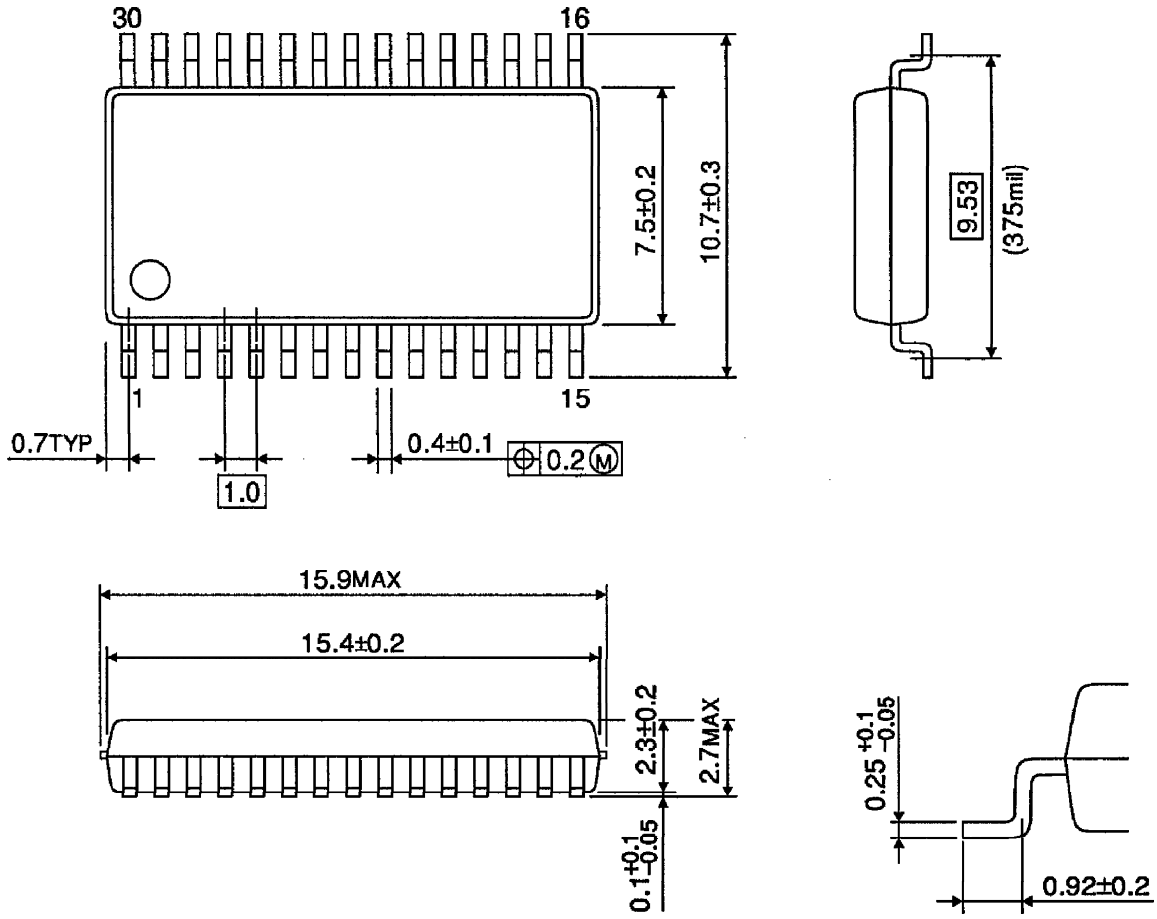
Unit : mm



Weight : 0.7g (Typ.)