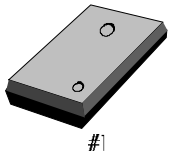
INTRODUCTION

24-QFN-3.5×4.5



The S1M8831A/33 is a Fractional-N frequency synthesizer with integrated prescalers, designed for RF operation up to 1.2GHz/K-PCS and for IF operation up to 520MHz. The fractional-N synthesizer allows fast-locking, low phase noise phase-locked loops to be built easily, thus having rapid channel switching and reducing standby time for extended battery life. The S1M8831A/33 based on $\sum$ - Δ fractional-N techniques solves the fractional spur problems in other fractional-N synthesizers based on charge pump compensation. The synthesizer also has an additional feature that the PCS/CDMA channel frequency in steps of 10kHz can be accurately programmed.

The S1M8831A/33 contains dual-modulus prescalers. The S1M8831A RF synthesizer adopts an 8/9 prescaler (16/17 for the S1M8833) and the IF synthesizer adopts an 8/9 prescaler. Phase detector gain is user-programmable for maximum flexibility to address IS-95 CDMA and IMT2000. Various program-controlled power down options as well as low supply voltage help the design of wireless cell phones having minimum power consumption.

Using the Samsung's proprietary digital phase-locked-loop technique, the S1M8831A/33 has a linear phase detector characteristic and can be used for very stable, low noise PLLs. Supply voltage can range from 2.7V to 4.0V. The S1M8831A/33 is available in a 24-QFN package.

FEATURES

- High operating frequency dual synthesizer
  - S1M8831A: 0.71 to 1.2GHz(RF)/ 45 to 520MHz(IF)
  - S1M8833: 1.6 to 1.65GHz(RF)/ 45 to 520MHz(IF)
- Operating voltage range: 2.7 to 4.0V
- Low current consumption (S1M8831A: 5.0mA, S1M8833: 7.0mA)
- Selectable power saving mode (I_{CC} = 1uA typical @ 3V)
- Dual-modulus prescaler and Fractional-N/Integer-N:
  - S1M8831A (RF) 8/9 Fractional-N
  - S1M8833 (RF) 16/17 Fractional-N
  - S1M8831A/33 (IF) 8/9 Integer-N
- Excellent in-band phase noise (– 85dBc/Hz @ PCS, -90dBc/Hz @CDMA)
  Improved fractional spurious performance (< 80dBc)
- Frequency resolution (= 10kHz/64 @ fref = 9.84MHz)
- Fast channel switching time: < 500us
- Programmable charge pump output current: from 50uA to 800uA in 50uA steps
- Programmability via on-chip serial bus interface

APPLICATIONS

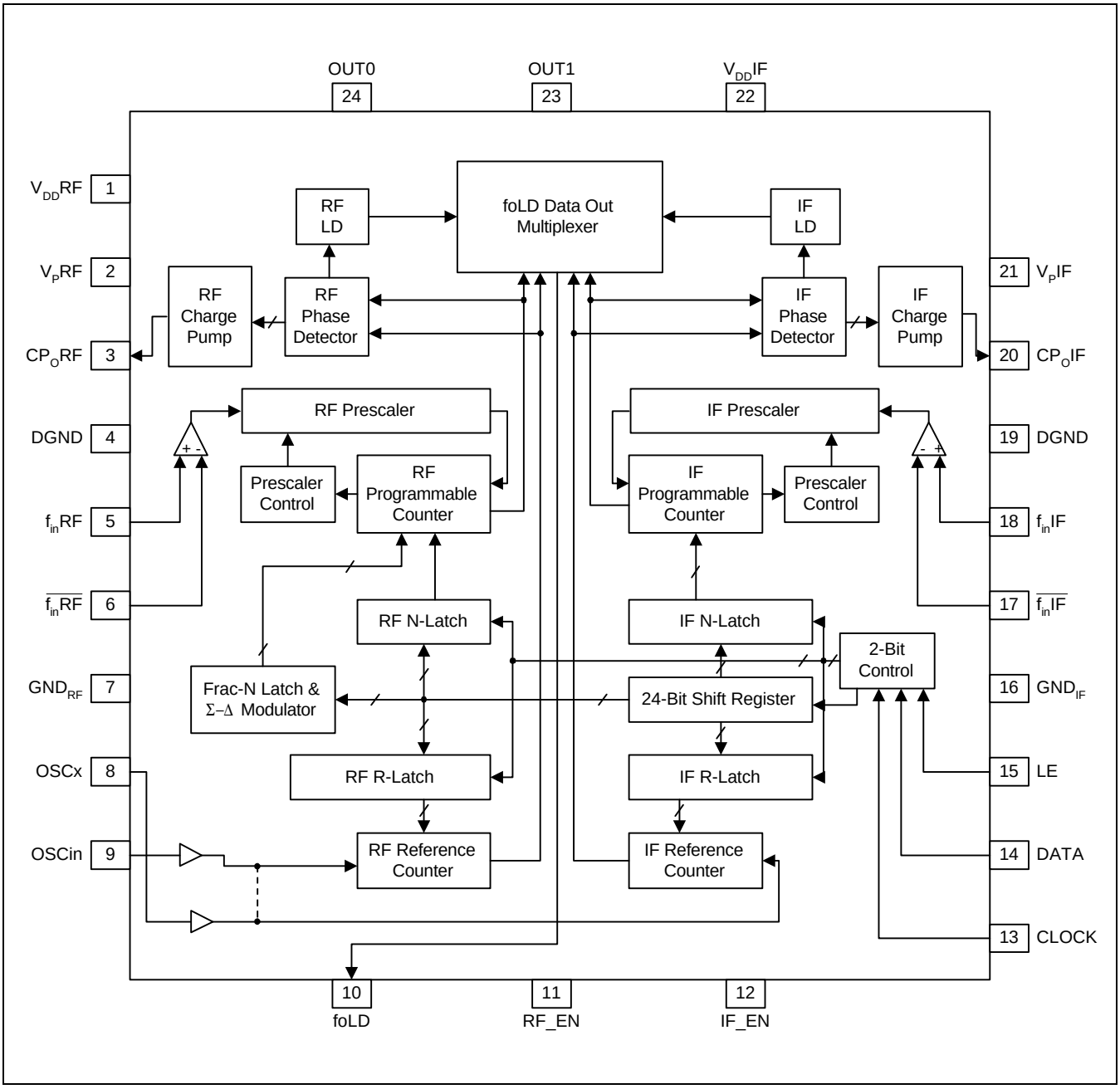
- High-rate data-service cellular telephones (for CDMA): S1M8831A, S1M8833
- High-rate data-service portable wireless communications (for Korean-PCS): S1M8833
- Other wireless communications systems

ORDERING INFORMATION

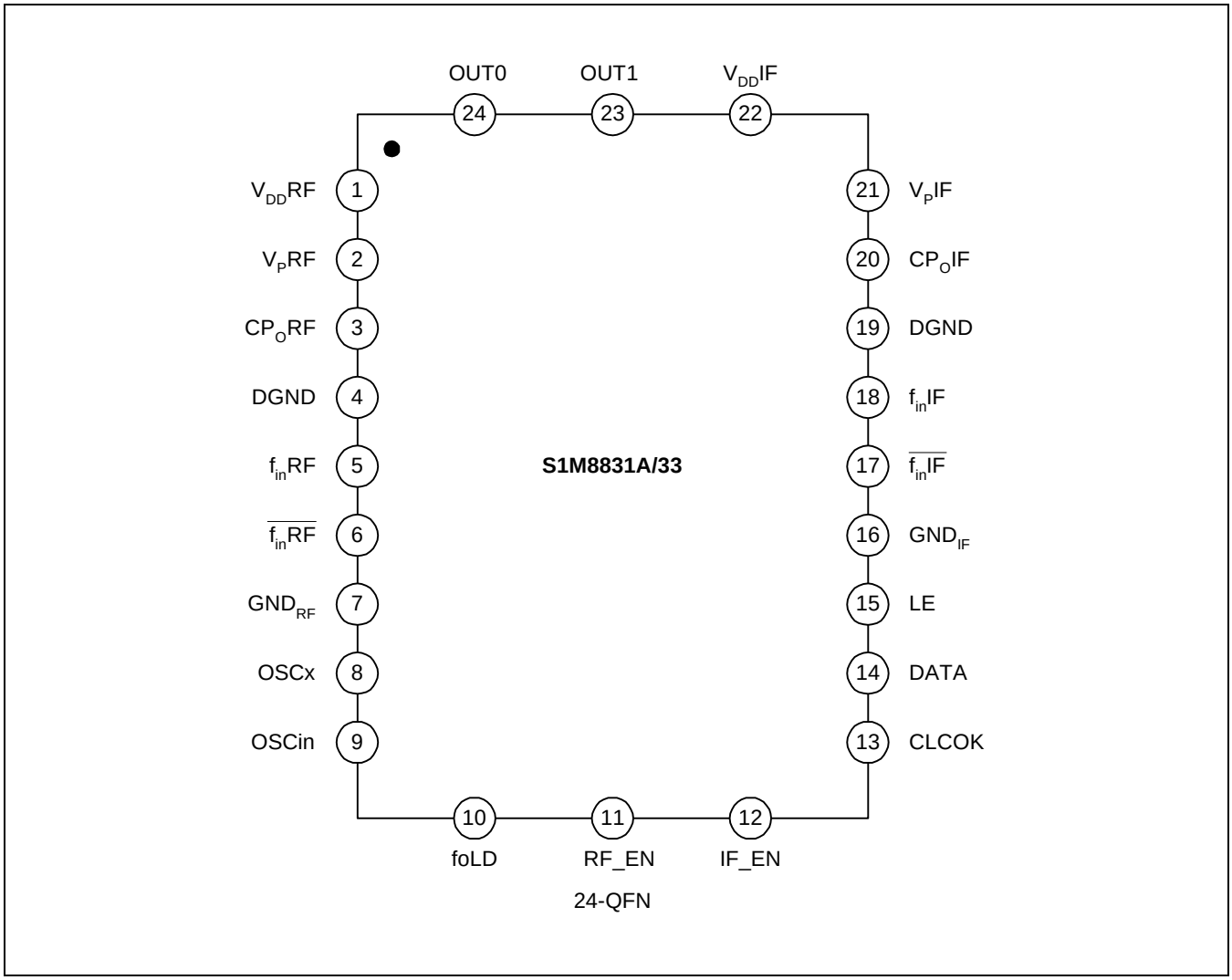
Device	Package	Operating Temperature
+S1M8831A01-G0T0	24-QFN-3.5×4.5	-40 to +85C
+S1M8833X01-G0T0		

+ : New Product

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

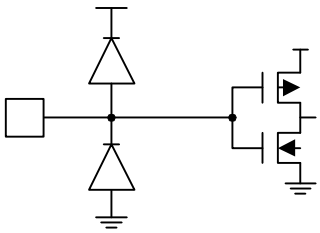
Pin No.	Symbol	I/O	Description
1	V_{DD}RF	–	RF PLL power supply(2.7V to 4.0V). Must be equal to V_{DD}IF.
2	V_PRF	–	Power supply for RF charge pump. Must be ≥ V_{DD}RF and V_{DD}IF.
3	CP_oRF	O	RF charge pump output. Connected to an external loop filter.
4	DGND	–	Ground for RF PLL digital circuitry.
5	f_{in}RF	I	RF prescaler input. Small signal input from the external VCO.
6	$\overline{f_{in}RF}$	I	RF prescaler complementary input. For a single-ended output RF VCO, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
7	GND_{RF}	–	Ground for RF PLL analog circuitry.
8	OSCx	I	RF R counter input (IF_N[22]=0) or not-use (IF_N[22]=1) which can be configured depending on the state of the program bit IF_N[22].
9	OSCin	I	Oscillator input to drive both the IF and RF R counter inputs (IF_N[22]=1) or only the IF R counter (IF_N[22]=0) which can be configured depending on the state of the program bit IF_N[22].
10	foLD	O	Multiplexed output of N or R divider and RF/IF lock detect.
11	RF_EN	I	RF PLL Enable (enable when high, power down when low). Controls the RF PLL to power down directly, not depending on a program control. Also sets the charge pump output to be in TRI-STATE when LOW. Powers up when HIGH depends on the state of RF_CTL_WORD.
12	IF_EN	I	IF PLL Enable(enable when high, power-down when low). Controls the IF PLL to power down directly. The same as RF_EN except that power-up depends on the state of IF_CTL_WORD.
13	CLOCK	I	CMOS clock input. Data for the various counters is clocked into the 24-bit shift register on the rising edge.
14	DATA	I	Binary serial data input. Data entered MSB (Most Significant Bit) first.
15	LE	I	Load enable when LE goes HIGH. High impedance CMOS input.
16	GND_{IF}	–	Ground for IF analog circuitry.
17	f_{in}IF	I	IF Prescaler complementary input. For a single-ended output IF VCO, a bypass capacitor should be placed as close as possible to this pin.
18	$\overline{f_{in}IF}$	I	IF prescaler input. Small signal input from the VCO.
19	DGND	–	Ground for IF PLL digital circuitry.
20	CPoIF	O	IF charge pump output. Connected to an external loop filter.

PIN DESCRIPTION (Continued)

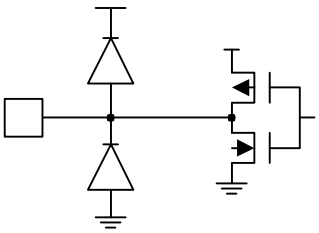
Pin No.	Pin Name	I/O	Descriptions
21	V_PIF	–	Power supply for IF charge pump. Must be ≥ V_{DD}RF and V_{DD}IF.
22	V_{DD}IF	–	IF PLL power supply (2.7V to 4.0V). Must be equal to V_{DD}RF.
23	OUT1	O	Programmable CMOS output. Level of the output is controlled by RF_N[19] bit.
24	OUT0	O	Programmable CMOS output. Level of the output is controlled by RF_N[18] bit. In the speedy lock mode, the OUT0 and OUT1 pins can be utilized as synchronous switches between active low and tri-state.

EQUIVALENT CIRCUIT DIAGRAM

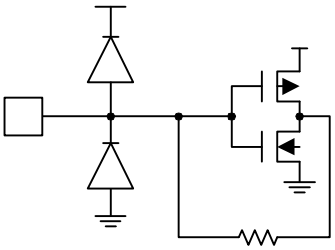
CLOCK, DATA, LE



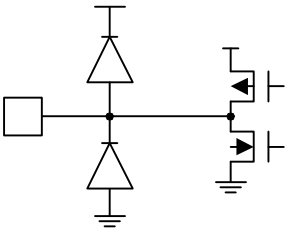
foLD



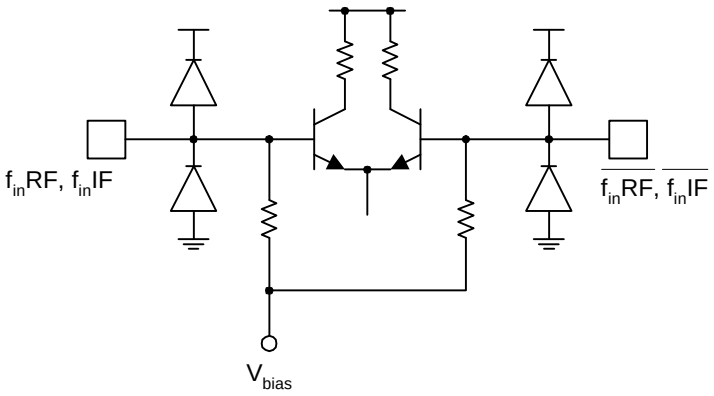
OSCin, OSCx



CP_ORF, CP_OIF



f_{in}RF, $\overline{f_{in}RF}$, f_{in}IF, $\overline{f_{in}IF}$



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power supply voltage	V_{DD}	0.0 to 4.0	V
Voltage on any pin with GND = 0 volts	V_I	-0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	600	mW
Operating temperature	T_a	-40 to +85	°C
Storage temperature	T_{STG}	-65 to +150	°C

ELECTROSTATIC CHARACTERISTICS

Characteristics	Pin No.	ESD Level	Unit
Human body model	All	< ± 2000	V
Machine model	All	< ± 300	V
Charge device model	All	< ± 800	V

NOTE: These devices are ESD sensitive. These devices must be handled in an ESD protected environment.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_P = 3.0V, T_a = 25°C, unless otherwise specified.)

Characteristic		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		2.7	3.0	4.0	V
		V_P		V_{DD}	3.0	4.0	
Power supply current	S1M8831A RF+IF	I_{DD}	Fractional-N mode (f_{osc} = 19.68MHz, RF R = 2)		5.0		mA
	S1M8833 RF+IF				7.0		
	S1M8831A RF+IF		Quiescent State		3.5		
	S1M8833 RF+IF				5.5		
	IF only				1.5		
Power down current		I_{PWDN}	V_{DD} = 3.0V		1	10	µA
Digital Inputs: CLOCK, DATA and LE							
High level input voltage		V_{IH}	V_{DD} = 2.7V to 4.0V	$0.7V_{DD}$			V
Low level input voltage		V_{IL}	V_{DD} = 2.7V to 4.0V			$0.3V_{DD}$	V
High level input current		I_{IH}	V_{IH} = V_{DD} = 4.0V	-1.0		+1.0	µA
Low level input current		I_{IL}	V_{IL} = 0V, V_{DD} = 4.0V	-1.0		+1.0	µA
Reference Oscillator Input: OSCin							
Input current		I_{IHR}	V_{IH} = V_{DD} = 4.0V			+100	µA
		I_{ILR}	V_{IL} = 0V, V_{DD} = 4.0V	-100			µA
Digital Output: foLD							
High level output voltage		V_{OH}	I_{out} = -500µA	V_{DD}-0.4			V
Low level output voltage		V_{OL}	I_{out} = +500µA			0.4	V

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = 3.0V, V_P = 3.0V, T_a = 25°C, unless otherwise specified.)

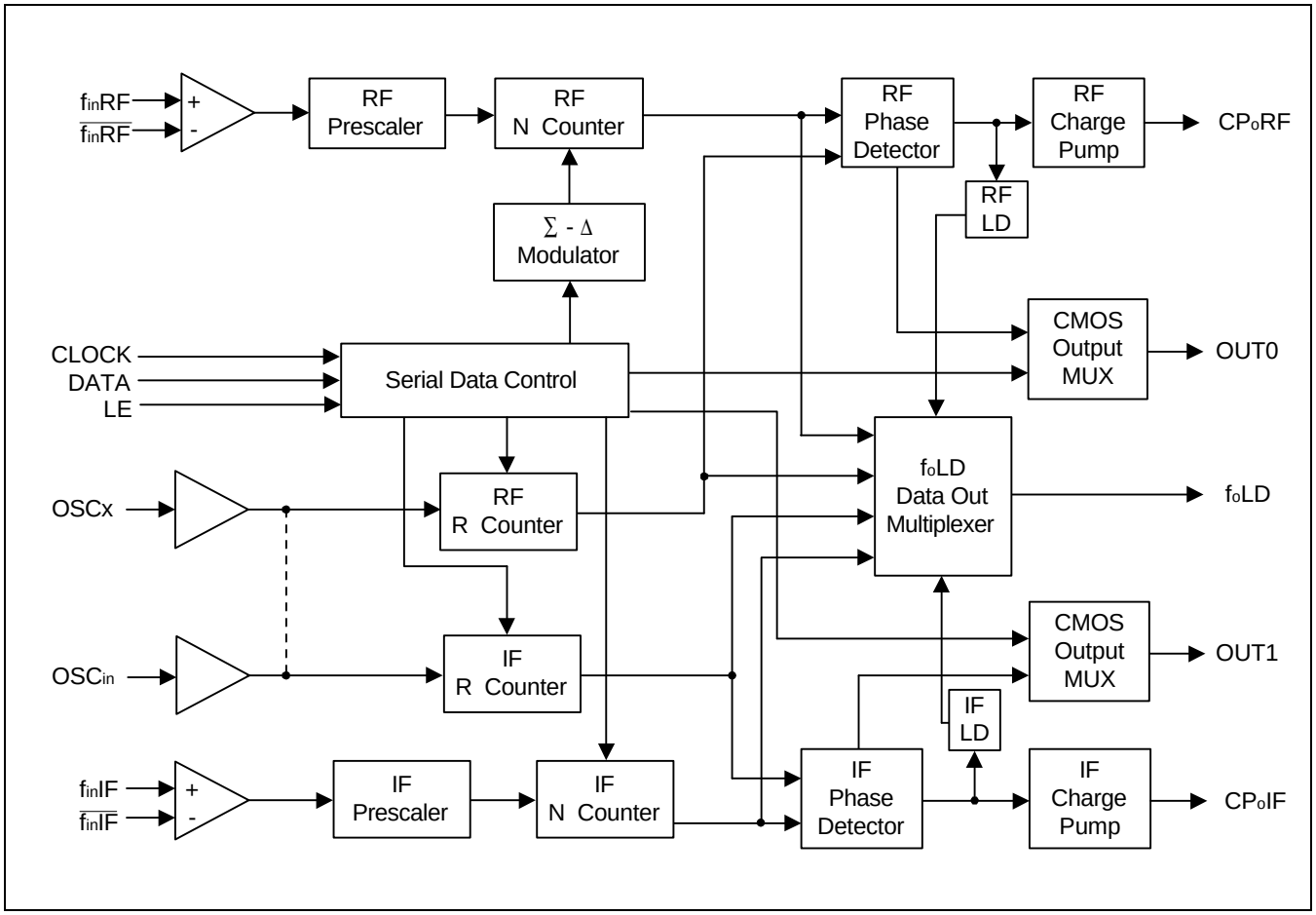
Characteristic		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Frequency, Input Sensitivity (Programmable Divider, PFD)							
RF operating frequency	S1M8833	f_{in}RF	Fractional-N mode (f_{osc} = 19.68MHz, RF R = 2)	1.6		1.65	GHz
	S1M8831A		Fractional-N mode (f_{osc} = 19.68MHz, RF R = 2)	0.71		1.2	GHz
IF operating frequency		f_{in}IF	V_{DD} = 3.0	45		520	MHz
Reference oscillator input frequency		OSC_{in}		2		40	MHz
Phase detector operating frequency		f_{PD}				10	MHz
RF input sensitivity		P_{fin}RF	V_{DD} = 3.0V	-15		0	dBm
			V_{DD} = 4.0V	-10		0	dBm
IF input sensitivity		P_{fin}IF	V_{DD} = 2.7V to 4.0V	-10		0	dBm
Reference oscillator input sensitivity		V_{OSCin}		0.5		V_{DD}	V_{PP}
Charge Pump Outputs: CPoRF, CPoIF							
RF charge pump output current		$I_{CPRF-SOURCE\_min}$	V_{CP} = V_P/2, RF_CP_WORD=0000		-50		uA
		$I_{CPRF-SIINK\_min}$	V_{CP} = V_P/2, RF_CP_WORD=0000		+50		uA
		$I_{CPRF-SOURCE\_max}$	V_{CP} = V_P/2, RF_CP_WORD=1111		-800		uA
		$I_{CPRF-SIINK\_max}$	V_{CP} = V_P/2, RF_CP_WORD=1111		+800		uA
IF charge pump output current		$I_{CPRF-SOURCE\_min}$	V_{CP} = V_P/2, CP_GAIN_8=0		-100		uA
		$I_{CPRF-SIINK\_min}$	V_{CP} = V_P/2, CP_GAIN_8=0		+100		uA
		$I_{CPRF-SOURCE\_max}$	V_{CP} = V_P/2, CP_GAIN_8=1		-800		uA
		$I_{CPRF-SIINK\_max}$	V_{CP} = V_P/2, CP_GAIN_8=1		+800		uA

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = 3.0V, V_P = 3.0V, T_a = 25°C, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Charge pump leakage current	I_{CPL}	$0.5V \le V_{CP} \le V_P$-0.5V	-2.5		+2.5	nA
Sink vs. Source mismatch	$I_{CP-SIINK}$ vs $I_{CP-SOURCE}$	$V_{CP} = V_P/2$		3	10	%
Output current magnitude variation vs. Voltage	I_{CP} vs V_{CP}	$0.5V \le V_{CP} \le V_P$-0.5V		10	15	%
Output current vs. Temperature	I_{CP} vs T_A	$V_{CP} = V_P/2$		10		%
Serial Data Control						
CLOCK frequency	f_{CLOCK}				10	MHz
CLOCK pulse width high	t_{CWH}		50			ns
CLOCK pulse width low	t_{CWL}		50			ns
DATA set up time to CLOCK rising edge	t_{DS}		50			ns
DATA hold time after CLOCK rising edge	t_{DH}		10			ns
LE pulse width	t_{LEW}		50			ns
CLOCK rising edge to LE rising edge	t_{CLE}		50			ns

FUNCTIONAL DESCRIPTION



The Samsung S1M8831A/33 is RF/IF dual frequency synthesizer IC which supports Fractional-N mode for RF PLL and Integer-N mode for IF PLL depending on a program control. S1M8831A/33 combined with external LPFs and external VCOs forms PLL frequency synthesizer. The frequency synthesizer consists of prescalers, pulse-swallowed programmable N counters, programmable reference R counters, phase detectors, programmable charge pumps, analog LD (Lock Detector), serial data control, etc.

An input buffer in the prescalers amplifies an RF input power of -10dBm from external RF/IF VCOs to a sufficient ECL switching level to drive the following ECL divider so that it can normally operate even in a smaller input power less than -10dBm. The amplified VCO output signal is divided by the prescaler with a pre-determined divide ratio (div. 8/9 in S1M8831A, div. 16/17 in S1M8833, div. 8/9 in IF), the N counter, or the Fractional-N circuitry (Σ - Δ modulator). External reference signal is divided by the R counter to set the comparison frequency of the PFD. The divide ratios of the programmable counters can be programmed via the serial bus interface. These two signals drive the both inputs of the phase detector. The phase detector drives the charge pump by comparing frequencies and phases of the above two signals. The charge pump and the external LPF make the control voltage for the external VCO and finally the VCO generates the appropriate frequency signal.

When the PLL is in the locked state, the RF VCO's frequency will be N_{INT} + N_{FRAC} times the comparison frequency, where N_{INT} is the integer divide ratio and N_{FRAC} is the fractional component.

The S1M8831A/33 has new improved features compared to conventional Integer-N PLLs.
The Fractional-N PLL is available for the RF. The fractional synthesis allows the PFD comparison frequency to be increased while maintaining the same channel frequency as in AMPS and IS-95A/B/C. It makes possible to widen a loop bandwidth as wide as 20kHz or more for a faster lock-up time and to improve in-band phase noise performance due to a reduced divide ratio N. Such S1M8831A/33 in the Fractional-N mode is suitable for CDMA, GSM and Korean PCS band applications.
Also, from the programmability of the charge pump, the user can easily design a stable loop due to free selection of loop components and reach to a low spurs, a low power PLLs due to an optimized current selection.

Prescaler

The RF/IF prescaler consists of a differential input buffer and ECL frequency dividers. The input buffer amplifies an input signal from an external VCO to the required level set by sensitivity requirements. The output of the amplifier delivers a differential signal to the divider with the correct DC level. The buffer may be either single-ended or differentially driven. The single-ended operation is preferred in typical applications due to external VCO. In this case, we recommend that the complementary input $\overline{fin}$ of the input buffer be AC coupled to ground through external capacitors, even though it is internally coupled to ground via an internal 10pF capacitor. The other input pin fin of the buffer also needs external capacitor for decoupling the DC component and controlling the input power level.

The RF prescalers of S1M8831A and S1M8833 provide 8/9 and 16/17 prescaler ratio, respectively. The IF prescaler of S1M8831A/33 contains 8/9 dual modulus prescaler.

Reference Oscillator Inputs

The reference oscillator frequency is provided by an external reference such as TCXO the OSCin and OSCx pins. When the OSC bit is LOW, the oscillator input pins (OSCin and OSCx) drive the IF R and R counters separately. When the OSC bit is HIGH, on the other hand, the oscillator input pin OSCin drives both IF R and RF R counters.

Programmable Dividers (RF/IF N Counters)

The RF N counter can be configured as a fractional counter. The fractional-N counter is selected when the Frac-N_SEL bit becomes HIGH.

In the fractional mode, the S1M8831A is capable of offering a continuous integer divide range from 72 to 1008 and the S1M8833 offering a continuous integer divide range from 161 to 168.

The S1M8831A/33 IF N counter supports an integer counter mode only, not including fractional counter, and is capable of operating from 45MHz to 520MHz offering a continuous integer divide range from 72 to 32767.

∑ - Δ Modulator

The RF part of S1M8831A/33 adopts the Σ -Δ modulator as a core of the fractional counter that makes it possible to obtain divide ratio N to be a fractional number between two contiguous integers. The Σ -Δ modulator effectively randomizes the quantization noise generated from digitizing process and results in extreme suppression of in-band noise power by pushing it out to out-of-band as in conventional Σ -Δ data converter. This technique eliminates the need for compensation current injection into the loop filter and improves fractional spurious performance, suitable for high-tier applications.
The ∑-Δ modulator operates only for fractional-N mode, when the Frac-N_SEL is HIGH.

For proper use of the fractional mode, the user should be kept in mind that

1. A fractional number should be set in the range from -0.5 to 0.5 in step of 1/62976.
2. The clock frequency fixed at 9.84MHz (= 19.68MHz/2) is recommended for the ∑-Δ modulator which is an optimum condition for achieving better electrical performances related to the fractional noise and power consumption. Only when using the clock frequency, the S1M8831A/33 guarantees the exact frequency resolutions: 10kHz for CDMA PCS and 30kHz for CDMA cellular.
   Note that the clock frequency much lower than 9.84MHz can deteriorate the fractional noise performance.

Phase-Frequency Detector (PFD) and Charge Pump (CP)

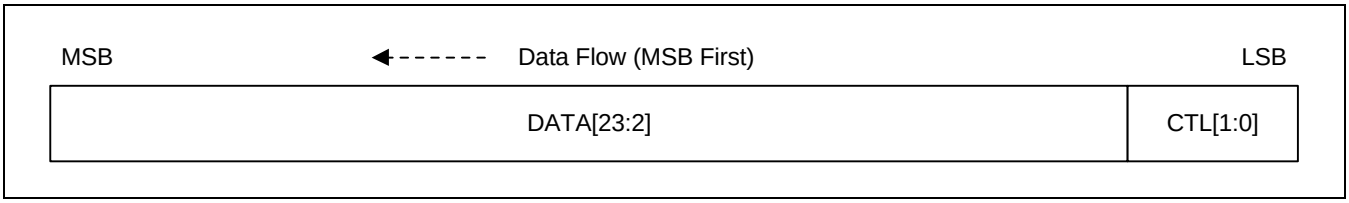
The RF/IF phase detector composed of PFD and CP outputs pump current into an external loop filter in proportional to the phase difference between outputs of N and R counter . The phase detector has a better linear transfer characteristic due to a feedback loop to eliminate dead zone. The polarity of the PFD can be programmed using RF_PFD_POL/IF_PFD_POL depending on whether RF/IF VCO characteristics are positive or negative. (programming descriptions for phase detector polarity)

Power-Down (or Power-Save) Control

Each PLL is individually power controlled by the enable pins (RF_EN and IF_EN pins) or program control bits (PWDN, PWDN_RF/IF). The enable pins override the program control bits. When both enable pins are HIGH, the program control bits determine the state of power control. Power down forces all the internal blocks to be deactivated and the charge pump output to be in the TRISTATE. The control register, however, remains active for serial programming and is capable of loading and latching in data during the power down.

PROGRAMMING DESCRIPTION

The S1M8831A/33 can be programmed via the serial bus interface. The interface is made of 3 functional signals: clock, data, and latch enable(LE). Serial data is moved into the 24-bit shift register on the rising edge of the clock. These data enters MSB first. When LE goes HIGH, data in the shift register is moved into one of the 4 latches (by the 2-bit control).



Control Bit Map (CTL[1:0])

Control Bits		Data Location
CTL2(CTL[1])	CTL1(CTL[0]	
0	0	RF/IF R counter
0	1	IF N counter
1	0	RF N counter
1	1	RF Frac counter

Data Bit Map (DATA[23:2])

	First Bit							Register Bit Location														Last Bit	
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RIF_R	TEST							IF_R_CNTR(15 bits)															0	0
IF_N	TEST	OSC	IF_CTL_ WORD			IF_CP_ WORD		IF_NB_CNTR(3 bits)												IF_NA_CNT R(3 bits)			0	1
RF_N	RF_CTL_WORD			CMOS				RF_CP_WORD						RF_NB_CNTR(7 bits)						FoLD(4 bits)			1	0
RF_Frac	RF_NA_CNTR(4 bits)				TEST			FRAC_CNTR(17 bits)															1	1

NOTE: Test bits are reserved and should be set to be zero(Low) for normal usage.

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
OSC	IF_N[22]	OSC	Separate inputs; OSCin: for IF, OSCx: for RF	Common input through OSCin for both RF and IF	Reference oscillator input control
IF_CTL_WORD	IF_N[21]	IF_CNT_RST	Normal operation	IF counter reset	IF
	IF_N[20]	PWDN_IF	Power up	Power down	IF
	IF_N[19]	PWDN	Asynchronous power down	Synchronous power down	RF and IF
IF_CP_WORD	IF_N[18]	IF_CP_GAIN	1X	8X	IF charge pump
	IF_N[17]	IF_PFD_POL	Negative slope	Positive slope	IF PFD
RF_CTL_WORD	RF_N[23]	RF_CNT_RST	Normal operation	RF counter reset	RF
	RF_N[22]	PWDN_RF	Power up	Power down	RF
	RF_N[21]	Frac-N_SEL	Integer-N mode	Fractional-N mode	RF; PLL mode selection
CMOS	RF_N[20]	Speedy_Lock	CMOS output	Speedy Lock mode	
	RF_N[19]	OUT1	Voltage LOW	Voltage HIGH	pin #23
	RF_N[18]	OUT0	Voltage LOW	Voltage HIGH	pin #24
RF_CP_WORD	RF_N[17:14]	RF_CP_LVL	Select 16-level charge pump current (RF charge pump gain for control codes in detail)		RF charge pump
	RF_N[13]	RF_PFD_POL	Negative slope	Positive slope	RF PFD
foLD	RF_N[5:2]	foLD	Select LDs and monitoring mode of internal counters. (foLD control for control codes in detail)		Lock Detector (LD), test mode

— Counter reset mode resets R & N counters.

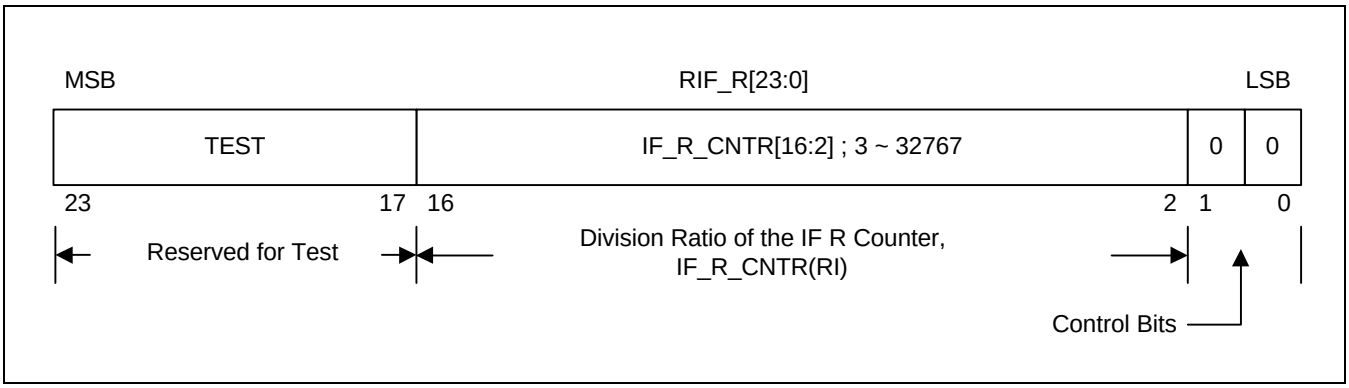
— IF charge pump current can be selected to high current (8X) or low current (1X) mode.

— In the Speedy Lock mode, the OUT0 and OUT1 pins can be utilized as synchronous switches between active low and tri-state. The Speedy Lock mode activates the OUT0 and OUT1 pins to be connected to GROUND with a low impedance (< 150Ω) while a high charge pump gain (≥ S 8X) is selected and otherwise to the TRISTATE.

— For using a programmable CMOS output, the CMOS output bit(RF_N[20]=L) should be activated and then the desired logic level should be programmed with the control bits RF_N[18] for OUT0 and RF_N[19] for OUT1.

Programmable Reference Counter (IF_R_CNTR[16:2])

If the control bit is 00, data is moved from the 24-bit shift register into the R-latch which sets the IF reference counter. Serial data format is shown in the table below.



- **15-Bit IF R Counter Division Ratio**

  Division ratio: 3 to 32767 (The divide ratios less than 3 are prohibited)
  Data are shifted in MSB first

Division Ratio	RI 14	RI 13	RI 12	RI 11	RI 10	RI 9	RI 8	RI 7	RI 6	RI 5	RI 4	RI 3	RI 2	RI 1	RI 0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

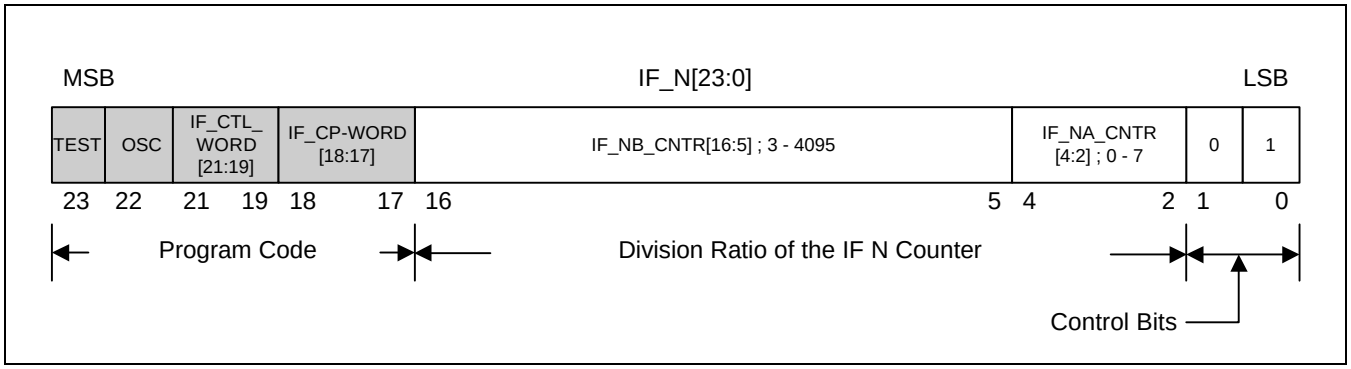
- **RF R Counter Division Ratio**

  Division Ratio: 2 (fixed value. Note it is not programmable.)

Programmable Counter (N CoUnter)

If the control bits are 01(IF), 10, and 11(RF), data is transferred from the 24-bit shift register into the N/Frac-latch. N Counter consists of swallow counter (A counter; 3-bit for IF & S1M8831A RF and 4-bit for S1M8833), main counter (B counter; 7-bit for S1M8831A/33 RF and 12-bit for IF), and fractional counter (F counter; 17-bit for S1M8831A/33 RF). Serial data format is shown below.

IF N Counter



- **IF Main Counter Division Ratio (B Counter)**

  IF_NB_ CNTR[16:5] ; for S1M8831A/33

Division Ratio(B)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1	N 0
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Division Ratio: 3 to 4095 (The division ratios less than 3 are prohibited)

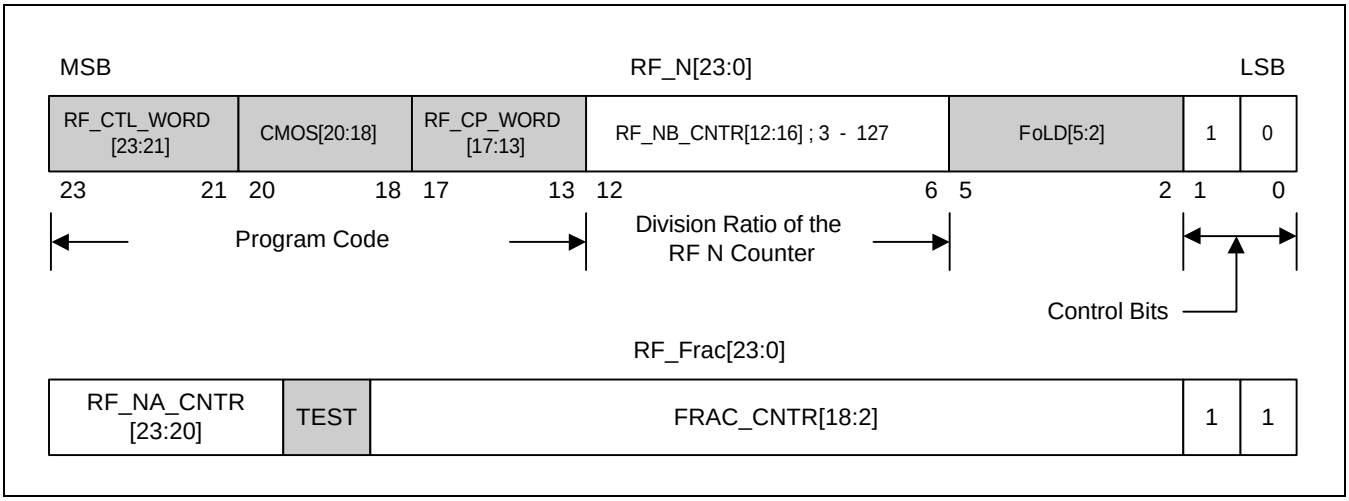
- **Swallow Counter Division Ratio (A Counter)**

  IF_NA_CNTR[4:2] ; for S1M8831A/33

Division Ratio(A)	N 2	N 1	N 0
0	0	0	0
1	0	0	1
•	•	•	•
7	1	1	1

Division Ratio: 0 to 7 (B > A)

RF N Counter



- **RF Main Counter Division Ratio (B Counter)**

RF_NB_ CNTR[12:6] ; for S1M8831A/33

Division Ratio(B)	N 6	N 5	N 4	N 3	N 2	N 1	N 0
3	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Division Ratio: 3 to 127 (The division ratios less than 3 are prohibited)

- **RF Swallow Counter Division Ratio (A Counter)**

RF_NA_CNTR[23:20] ; for S1M8831A

Division Ratio(A)	N 3	N 2	N 1	N 0
0	x	0	0	0
1	x	0	0	1
•	•	•	•	•
7	x	1	1	1

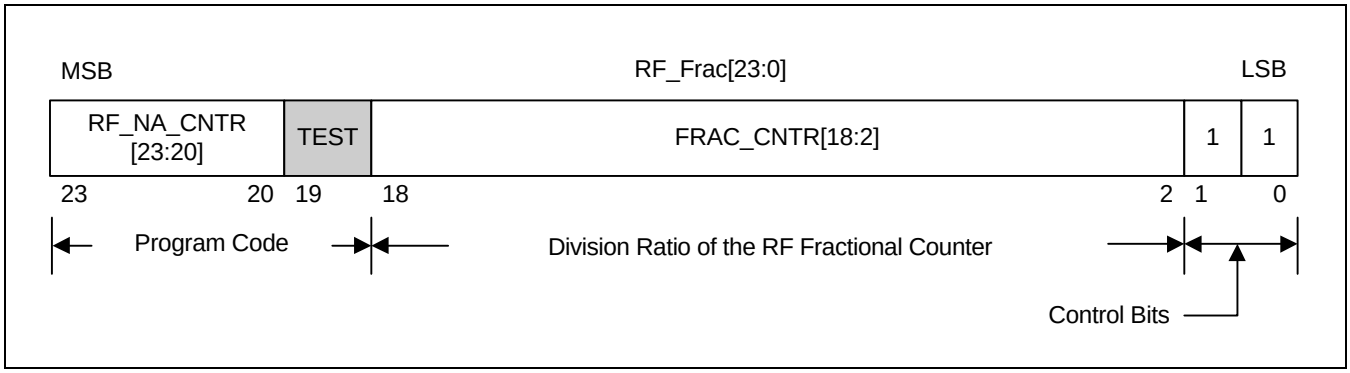
Division Ratio: 0 to 7 (B > A)
x = Don' t care condition

RF_NA_CNTR[23:20] ; for S1M8833

Division Ration(A)	N 3	N 2	N 1	N 0
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

Division Ratio: 0 to 15 (B > A)

RF Fractional Counter



- **RF Fractional Counter Value (F Counter)**

FRAC_ CNTR[18:2] ; for S1M8831A/33 RF

Counter Value(F)	F 16	F 15	F 14	F 13	F 12	F 11	F 10	F 9	F 8	F 7	F 6	F 5	F 4	F 3	F 2	F 1	F 0
31488	0	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
-31488	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

F Counter Value: -31488(2's complementary) to 31488

NOTE: For a negative integer, the counter value should be inputted as the corresponding 2's complementary binary code. For instance, the 2's complementary binary code of -2 is
1 1111 1111 1111 1110.

Programmable PFD and Charge Pump

IF Charge Pump Gain (IF_CP_WORD; IF_N[18])

Control Words	Control Bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CP_WORD	IF_N[18]	IF_CP_GAIN	1X (100uA)	8X (800uA)	IF charge pump

RF Charge Pump Gain (RF_CP_WORD; RF_N[17:14])

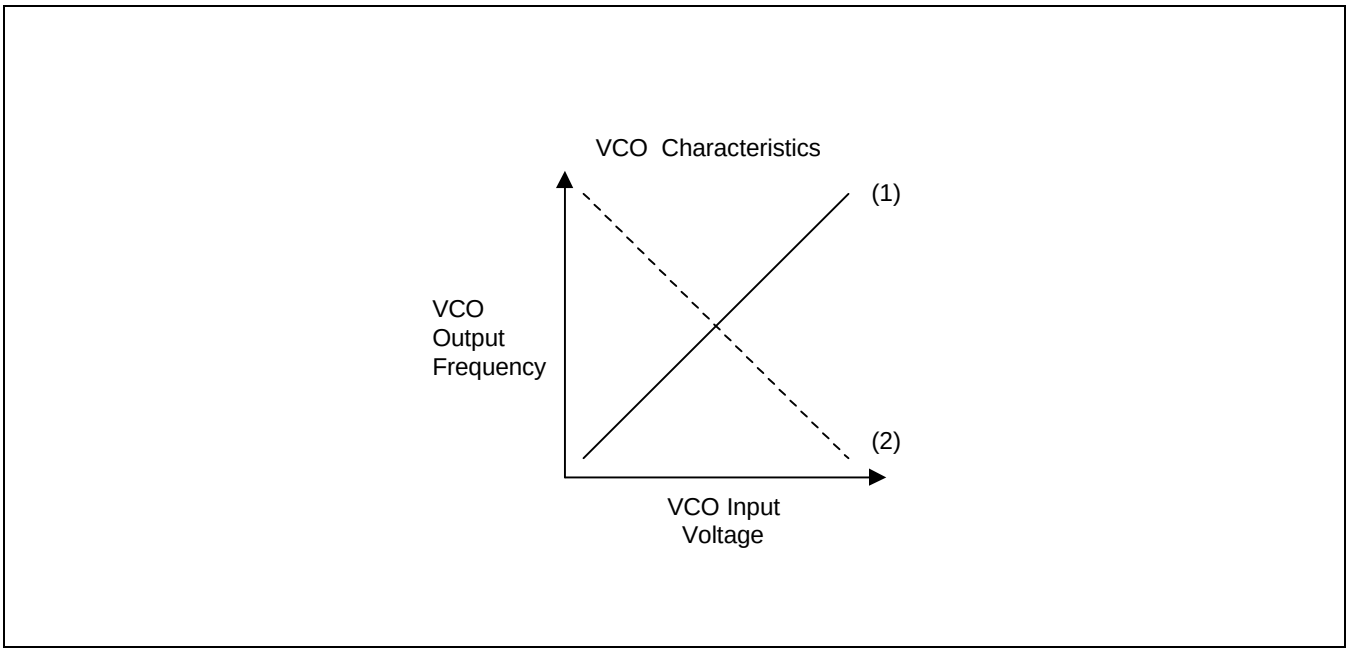
Control Words	Control Bits	Acronym	LOW (0)	HIGH (1)	Comments
RF_CP_WORD	RF_N[17:14]	RF_CP_LVL	Select 16-level charge pump current		RF charge pump

Icpo (uA)	8X	4X	2X	1X
	RF_N[17]	RF_N[16]	RF_N[15]	RF_N[14]
50	0	0	0	0
100	0	0	0	1
•	•	•	•	•
200	0	0	1	1
250	0	1	0	0
•	•	•	•	•
400	0	1	1	1
450	1	0	0	0
•	•	•	•	•
800	1	1	1	1

Phase Detector Polarity (RF_CP_WORD/IF_CP_WORD; RF_N[13]/IF_N[17])

Depending on VCO characteristics, IF_N[17] and RF_N[13] bits should be set as follows:

Control Bits	LOW (0)	HIGH (1)	Comments
IF_N[17]	Negative Slope	Positive Slope	IF PFD
RF_N[13]	Negative Slope	Positive Slope	RF PFD



Program Mode Control

Power Down Mode Operation

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CTL_WORD	IF_N[20]	PWDN_IF	Power Up	Power Down	IF
	IF_N[19]	PWDN	Asynchronous Power Down	Synchronous Power Down	RF and IF
RF_CTL_WORD	RF_N[22]	PWDN_RF	Power Up	Power Down	RF

Each PLL is individually power controlled by the enable pins (RF_EN and IF_EN pins) or program control bits (PWDN, PWDN_RF/IF). The enable pins override the program control bits. When both enable pins are HIGH, the program control bits determine the state of power control. Power down forces all the internal analog blocks to be deactivated and the charge pump output to be in a TRISTATE. The oscillator circuitry function becomes disabled dependent on the state of IF and RF power-down bits, IF_N[20] and RF_N[22]. The RF(or IF) oscillator buffer is powered down when the power down bit (RF_N[22] or IF_N[20]) becomes HIGH. The control register and R/N counters, however, remains active for permitting serial programming and is capable of loading and latching in data during the power down. The PLL returns to the active power-up mode when IF_N[20] and RF_N[22] become LOW.

There are synchronous and asynchronous power-down modes for S1M8831A/33. The power-down bit IF_N[19] is used to select between synchronous and asynchronous power down. Synchronous power down mode occurs if IF_N[19] bit is HIGH and then the power down bit (RF_N[22] or IF_N[20]) becomes HIGH. In the synchronous power down mode, the power-down function will go into power down mode upon the completion of a charge pump pulse event because it is synchronized with the charge pump and thus can diminish undesired frequency jumps. Asynchronous power down mode occurs if IF_N[19] bit is LOW and then the power down bit (RF_N[22] or IF_N[20]) becomes HIGH. Activation of the asynchronous function will go into power-down mode immediately.

RF Power Down Mode Table

RF_N[22]	IF_N[19]	Power Down Mode Status
0	0	RF PLL active
0	1	RF PLL active, only charge pump to TRISTATE
1	0	Asynchronous power down
1	1	Synchronous power down

IF Power Down Mode Table

IF_N[20]	IF_N[19]	Power Down Mode Status
0	0	IF PLL active
0	1	IF PLL active, only charge pump to TRISTATE
1	0	Asynchronous power down
1	1	Synchronous power down

Reference Oscillator Input Control

Control Words	Control bits	Acronym	LOW (0)	HIGH (1)	Comments
OSC	IF_N[22]	OSC	separate inputs; OSCin: for IF, OSCx: for RF	common input through OSCin for both RF and IF	reference oscillator input control

The reference oscillator frequency is provided from an external reference such as TCXO through the OSCin and OSCx pins. When the OSC bit is LOW, the oscillator input pins(OSCin and OSCx) drive the IF R and RF R counters separately. When the OSC bit is HIGH, on the other hand, the oscillator input pin OSCin drives the IF R and RF R counters commonly.

IF_N[22] = LOW

PWDN_IF	PWDN_RF	IF	RF
IF_N[20]	RF_N[22]		
0	0	OSC_{in}	OSC_x
0	1	OSC_{in}	LOW(powerdown)
1	0	LOW(powerdown)	OSC_x
1	1	LOW(powerdown)	LOW(powerdown)

IF_N[22] = HIGH

PWDN_IF	PWDN_RF	IF	RF
IF_N[20]	RF_N[22]		
0	0	OSC_{in}	OSC_{in}
0	1	OSC_{in}	LOW(powerdown)
1	0	LOW(powerdown)	OSC_{in}
1	1	LOW(powerdown)	LOW(powerdown)

Programmable Counter Reset Control

Control Words	Control Bits	Acronym	LOW (0)	HIGH (1)	Comments
IF_CTL_WORD	IF_N[21]	IF_CNT_RST	Normal Operation	IF Counter Reset	IF
RF_CTL_WORD	RF_N[23]	RF_CNT_RST	Normal Operation	RF Counter Reset	RF

Counter Reset Mode Resets R & N Counters.

RF Fractional-N Selection

Control Words	Control Bits	Acronym	LOW (0)	HIGH (1)	Comments
RF_CTL_WORD	RF_N[21]	Frac-N_SEL	Reserved	Fractional-N Mode	RF; PLL Mode Selection

CMOS Output Control

Control Words	Control Bits	Acronym	LOW (0)	HIGH (1)	Comments
CMOS	RF_N[20]	Speedy Lock	CMOS Output	Speedy Lock Mode	
	RF_N[19]	OUT1	Voltage LOW	Voltage HIGH	Pin #23
	RF_N[18]	OUT0	Voltage LOW	Voltage HIGH	Pin #24

In the Speedy Lock mode, the OUT0 and OUT1 pins can be utilized as synchronous switches between active low and a tri-state. The Speedy Lock mode activates the OUT0 and OUT1 pins to be connected to GROUND with a low impedance (< 150Ω) while a high charge pump gain (≥ 8X) is selected and otherwise to a tri-state. For using a programmable CMOS output, the CMOS output bit(RF_N[20] = LOW) should be activated and then the desired logic level should be programmed with the control bits RF_N[18] for OUT0 and RF_N[19] for OUT1.

foLD Control

Control Words	Control Bits	Acronym	LOW (0)	HIGH (1)	Comments
foLD	RF_N[5:2]	foLD	Select LDs and monitoring mode of internal counters.		Lock Detector(LD), Test Mode

foLD[3]	foLD[2]	foLD[1]	foLD[0]	foLD Output State
0	0	0	0	Disabled (default LOW)
0	0	0	1	RF and IF analog lock detect
0	0	1	0	Reserved test mode
0	0	1	1	Reserved test mode
X	1	0	0	Reserved test mode
X	1	0	1	IF R counter output
X	1	1	0	IF N counter output
X	1	1	1	RF R counter output
1	0	0	0	RF N counter output
1	0	0	1	Reserved test mode
1	0	1	0	Reserved test mode
1	0	1	1	Reserved test mode

— When the PLL is locked and the analog lock detect mode is selected, the foLD output is HIGH, with narrow pulses LOW.

Lock Detector (LD)

There is analog mode for S1M8831A/33. The foLD bits, RF_N[5:2], are used to select the lock detection mode and to output the selected lock signal through the foLD pin.

The foLD output becomes HIGH with narrow pulsed LOW while both RF and IF PLLs are locked and thereby the output should be low-pass filtered for a DC locked voltage HIGH.

Pulse Swallow Function

The RF VCO's frequency f_{VCO} becomes $N_{INT} + N_{FRAC}$ times the comparison frequency (f_{OSC}/R) where NINT is the integer divide ratio and NFRAC is the fractional component;

$f_{VCO} = (N_{INT} + N_{FRAC}) \times f_{OSC}/R = N \times f_{OSC}/R$

where $N_{INT} = (P \times B) + A$,

RF PLL: $N_{FRAC} = F/62976$, $-31488 \leq F \leq 31488$, $B > P$, and $R = 2$

IF PLL: $N_{FRAC} = 0$, $B > A$, and $3 \leq R \leq 32767$

f_{VCO} : External VCO output frequency
f_{OSC} : External reference frequency (From external oscillator)
R : Preset divide ratio of programmable R counter (RF: 2, IF: 3 to 32767);
P : Preset modulus of dual modulus prescaler (S1M8831 RF: P=8, S1M8833 RF: P=16, IF: P=8)
B : Preset value of main counter (S1M8831A/33 RF: 3 to 126, IF: 3 to 4095)
A : Preset value of swallow counter division ratio
(S1M8831 RF: $0 \leq A \leq 7$, S1M8833 RF: $0 \leq A \leq 15$, IF: $0 \leq A \leq 7$, $A < B$)
N_{FRAC} : Fractional component of Pulse-swallowed division ratio N (for IF: $N_{FRAC} = 0$)
F : Preset value of fractional register ($-31488 \leq F \leq 31488$);
For a negative integer, F should be inputted as its 2's complementary binary code.

For examples in S1M8831 fractional-N mode (f_{OSC} = 19.68MHz, R=2, P=8)

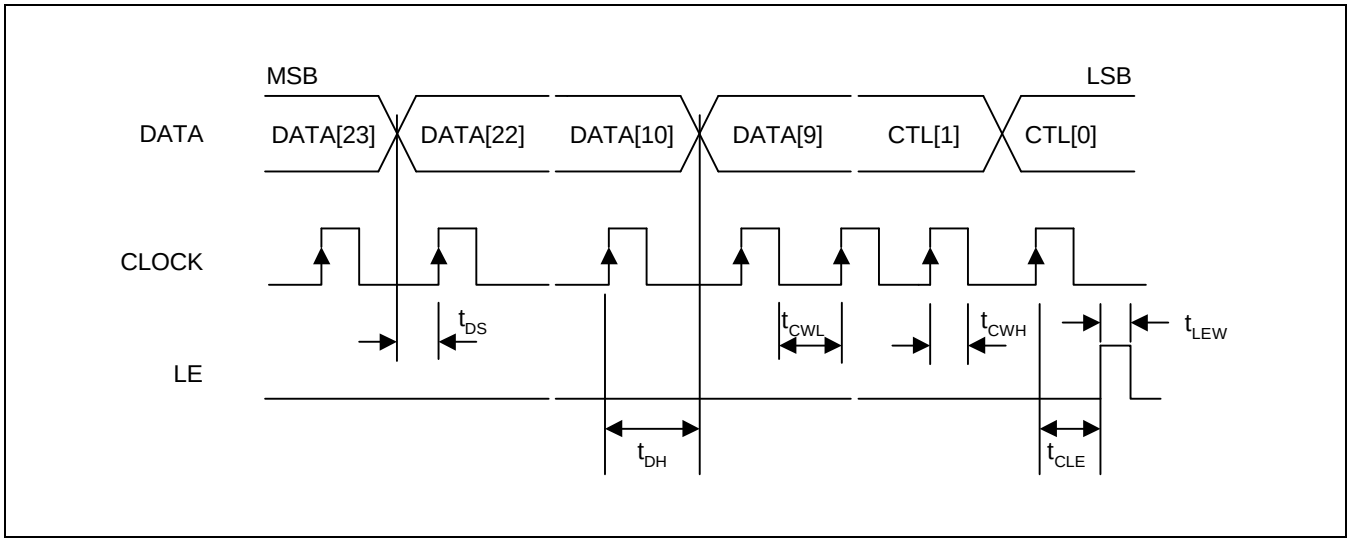
1) for fvco = 955.02MHz ; N = 97.05487805, B=12, A=1, F=3456 (= 0 0000 1101 1000 0000)
2) for fvco = 955.03MHz ; N = 97.05589431, B=12, A=1, F=3520
3) for fvco = 956.25MHz ; N = 97.17987805, B=12, A=1, F=11328
4) for fvco = 979.35MHz ; N = 99.52743902, B=12, A=4, F=-29760

∴ F= 0.52743903 X 62976 = 33125 → 33125 > 31488 (A=3+1=4)
= 33215 – 62976 = -29760 (1 1000 1011 1100 0000)

For examples in S1M8833 fractional-N mode (f_{OSC} = 19.68MHz, R=2, P=16)

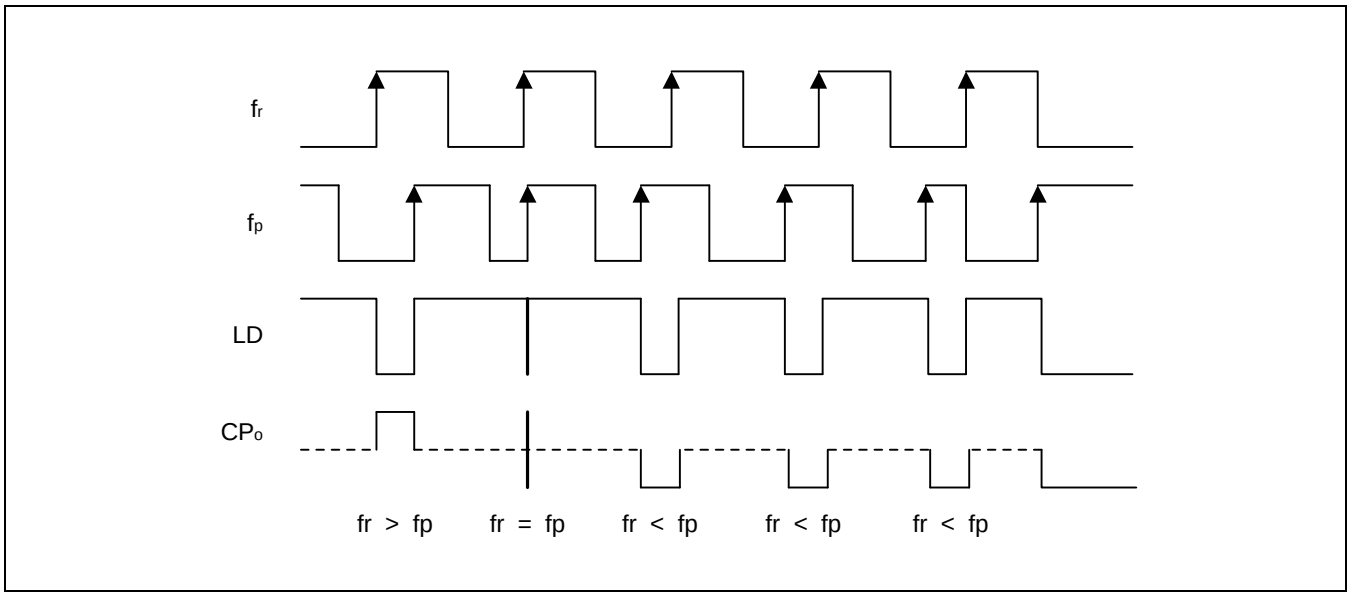
1) for fvco = 1620.87MHz(CH25) ; N = 164.722561, B=10, A=5, F=-17472 (= 1 1011 1011 1100 0000)
2) for fvco = 1620.88MHz ; N = 164.7235772, B=10, A=5, F=-17408
3) for fvco = 1622.12MHz(CH50) ; N = 164.8495935, B=10, A=5, F=-9472
4) for fvco = 1632.12MHz(CH250) ; N = 165.8658537, B=10, A=6, F=-8448
5) for fvco = 1648.37MHz(CH575) ; N = 167.5172764, B=10, A=8, F=-30400

Serial Data Input Timing

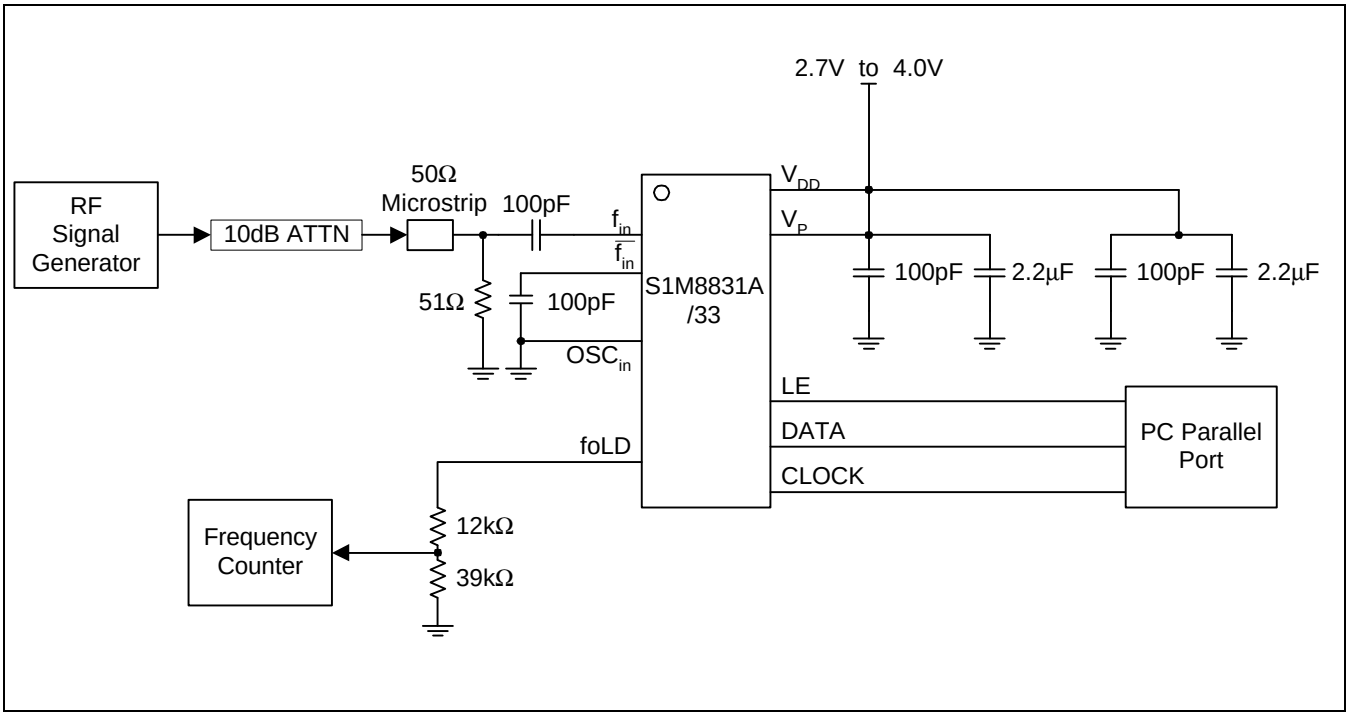


Phase Detector and Charge Pump Characteristics

Phase difference detection range: -2π to +2π
When the positive-slope polarity of PFD is selected, IF_N[17] = HIGH or RF_N[13] = HIGH;



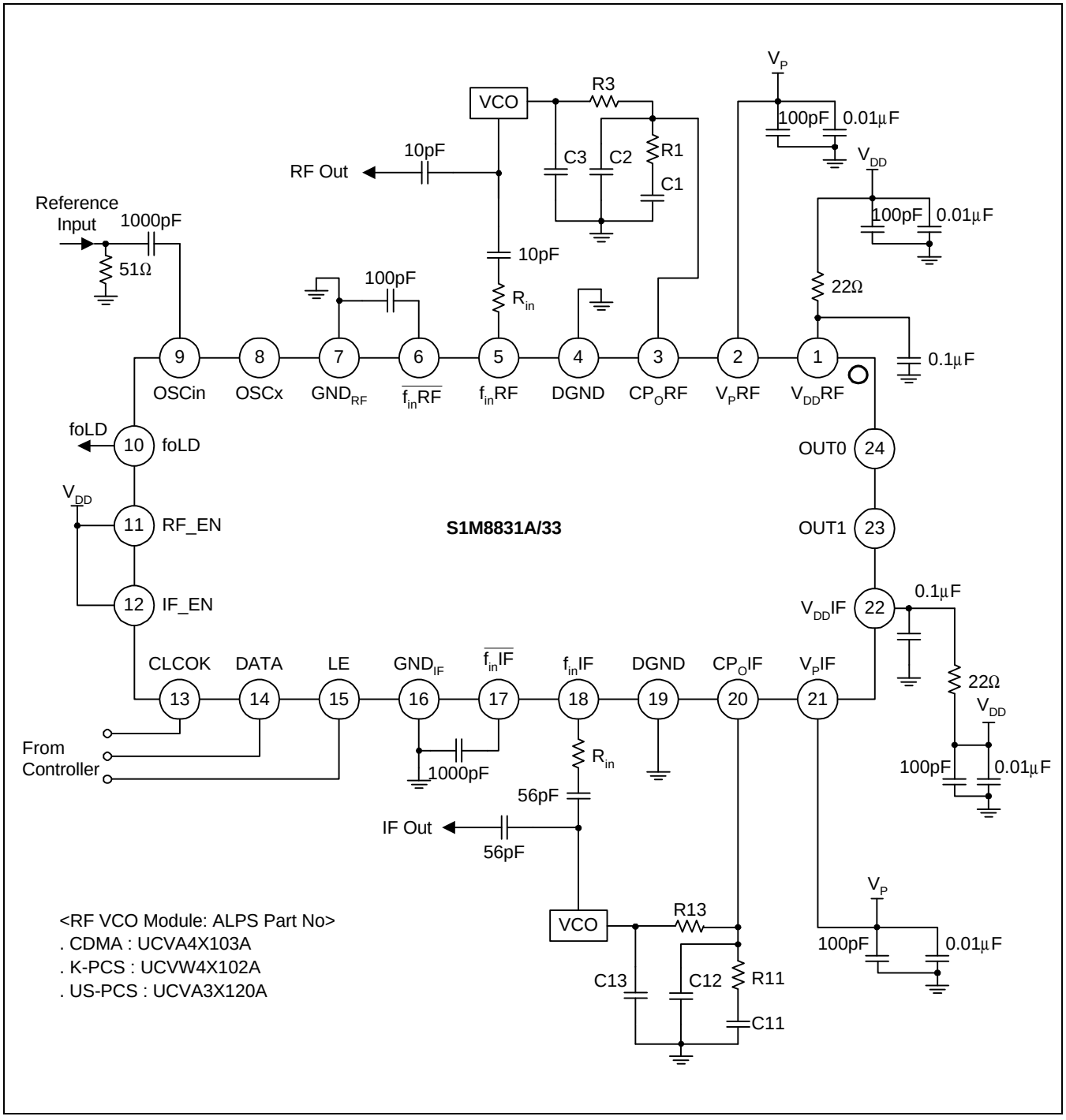
SIMPLIFIED SCHEMATIC DIAGRAM FOR RF SENSITIVITY TEST



NOTES:

1. Sensitivity limit is determined when the error of the divided RF output (fOLD) becomes 10Hz.
2. f_{VCO} = 1.0GHz, N = 1000, P = 8, R = 2 in S1M8831 Integer-N test mode
   f_{VCO} = 1.6GHz, N = 1600, P = 16, R = 2 in 1M8833 Integer-N test mode

TYPICAL APPLICATION CIRCUIT



NOTE: The role of Rin: Rin makes a large portion of VCO output power go to the load rather than the PLL. The value of Rin depends on the VCO power level.

PCB LAYOUT GUIDE

In doing PCB layouts for S1M8831A/33, we recommend that you apply the following design guide to your handsets, thus improving the phase noise and reference spurious performances of the phones.

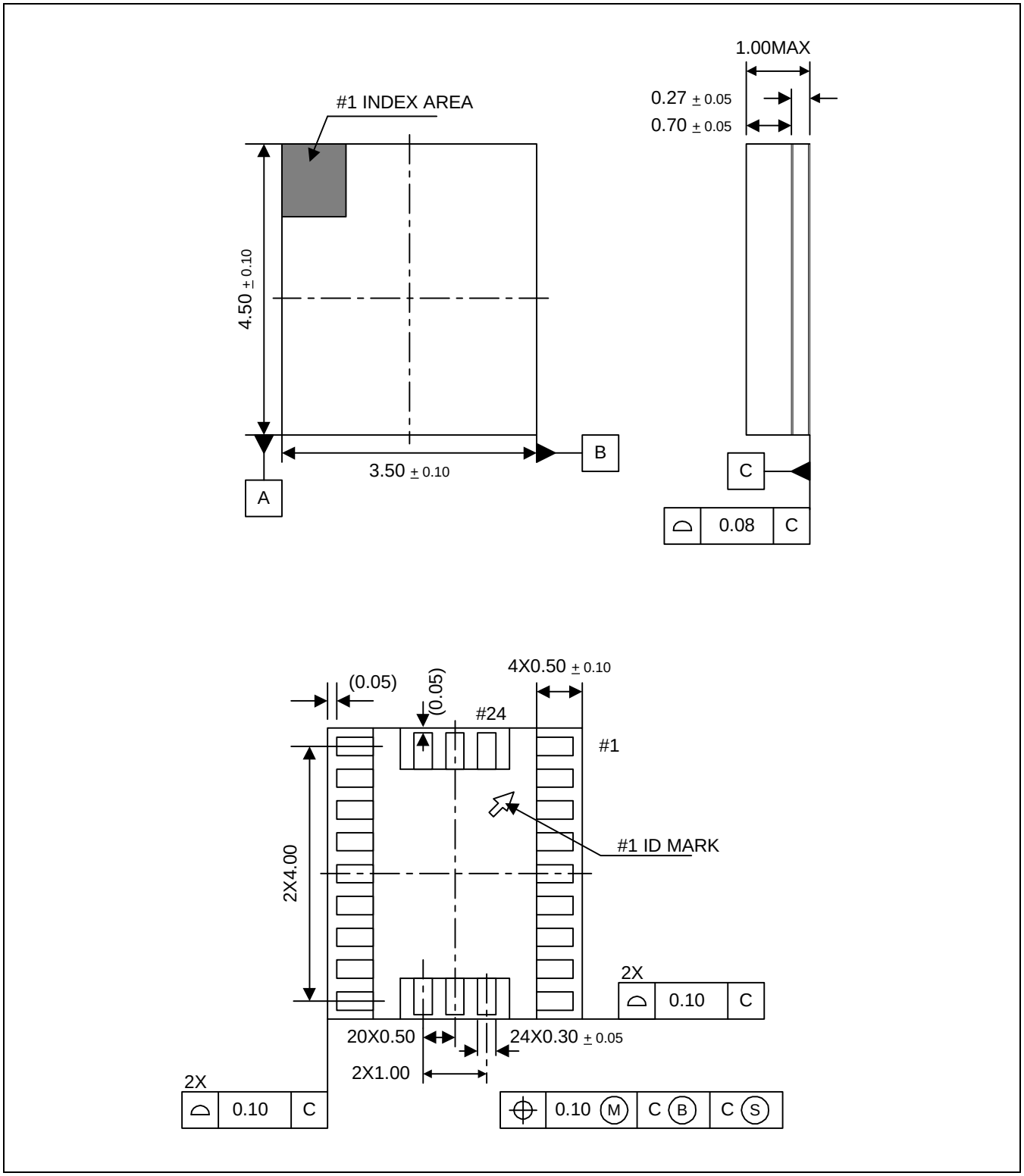
1. The S1M8831A/33 has external four power supply pins to supply on-chip bias, each for analog and digital blocks of RF and IF PLLs. Basically in doing PCB layout, it is important that power supply lines should be separated from one another and thus coupling noises through the voltage supply lines can be minimized. If you have some troubles with the direction to separate, you can choose the following recommendations for your convenience;
   - Tying analog power lines, V_{CC}RF and V_{CC}IF, is possible.
   - Tying digital power lines, V_{P1} and V_{P2}, is possible.
   - A point connecting the analog and digital power lines should be near to battery line as close as possible.

   It minimizes coupling noise effects from a digital switching noise into analog blocks. We also recommend that a passive RC low pass filter (R(22Ω), C(100nF)) be utilized for suppressing high frequency noise on the analog power supply line and reducing any digital noise couplings.

2. VCO power lines should be well separated from those of PLL because VCO is generally a very sensitive device from power line noises and PLL is a digital noise generator.

3. For more improvement of reference spurious performance, it is recommended that the LPF ground be tied to the PLL ground, not the VCO ground.

PACKAGE DIMENSIONS



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