MH88632B

Central Office Interface Circuit

Preliminary Information

DS5574 ISSUE 4 October 2001

Features

- Supports Loop Start and Ground Start protocols
- 2-4 Wire conversion
- Programmable Input Impedance, Network Balance Impedance and gains
- Three relay drivers
- Line state detection outputs
- 15mA operation allowing long line length capability
- On-hook reception for Caller Line Identification
- Meets FCC Part 68 Leakage Current Requirements

Applications

Interface to Central Office telephone line for

- PBX
- Key Telephone System
- Terminal Equipment
- Digital Loop Carrier
- Wireless Local Loop

Ordering Information

MH88632B 40 Pin SIL Package

0°C to 70°C

Description

The Zarlink MH88632B Central Office Interface Circuit provides a complete analog and signalling link between audio switching equipment and a subscriber line. The device is available in a single in line package for high packing densities or in a 90° package for reduced card clearance.

The device is fabricated using thick film hybrid technology for optimum circuit design and very high reliability.

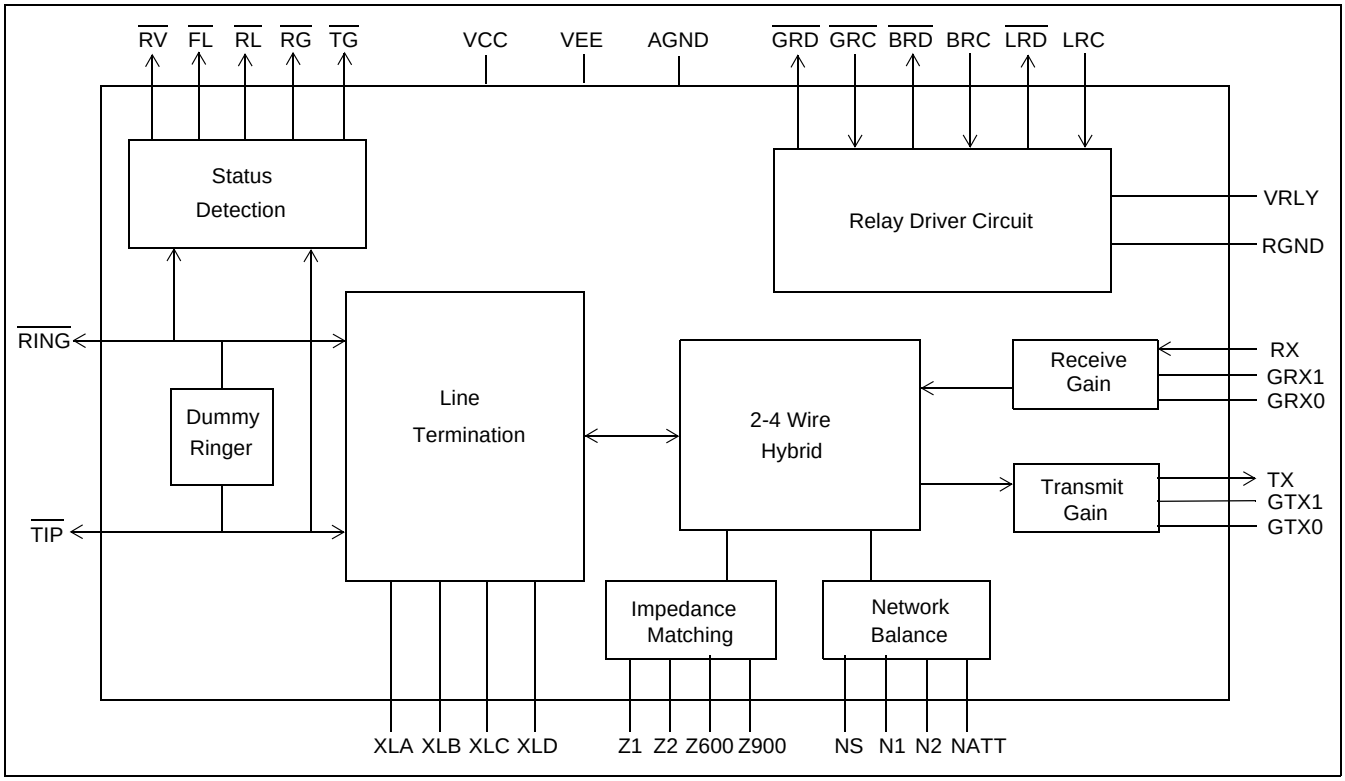


Figure 1 - Functional Block Diagram

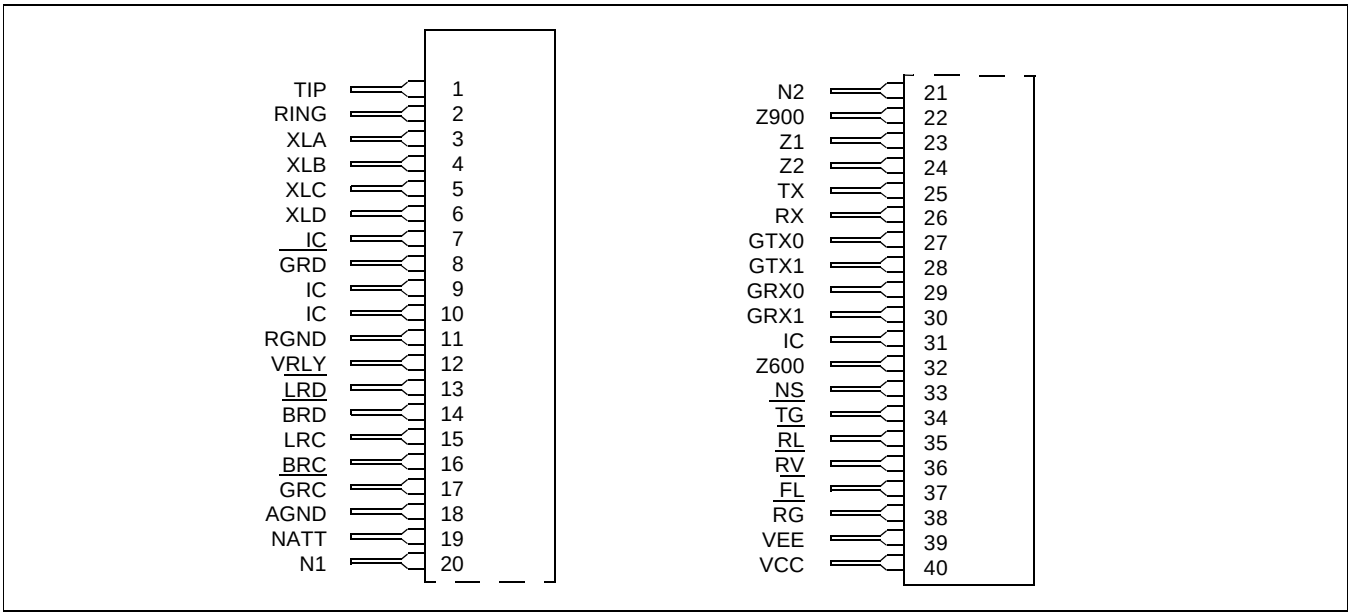


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	TIP	**Tip Lead.** Connects to the Tip lead of a telephone line usually via an external protection circuit.
2	RING	**Ring Lead.** Connects to the Ring lead of a telephone line usually via an external protection circuit.
3	XLA	**Loop Relay Contact A.** Connects to XLB through relay contacts (K1A) when the relay is energized.
4	XLB	**Loop Relay Contact B.** Connects to XLA through relay contacts (K1A) when the relay is energized.
5	XLC	**Loop Relay Contact C.** Connects to XLD through relay contacts (K1B) when the relay is energized.
6	XLD	**Loop Relay Contact D.** Connects to XLC through relay contacts (K1B) when the relay is energized.
7	IC	**Internal Connection.** No connection should be made to this pin.
8	$\overline{\text{GRD}}$	**Ground Ring Lead Relay Drive (Output).** Connects to the Ground Ring Lead Relay coil (K3) and is controlled by GRC.
9	IC	**Internal Connection.** No connection should be made to this pin.
10	IC	**Internal Connection.** No connection should be made to this pin.
11	RGND	**Relay Ground.** Return path for relay supply voltage.
12	VRLY	**Relay Positive Supply Voltage.** Normally +5V. Connects to all relay coils and the relay supply voltage.
13	$\overline{\text{LRD}}$	**Loop Relay Drive (Output).** Connects to the Loop Relay coil (K1) and is controlled by LRC.
14	$\overline{\text{BRD}}$	**Bias Relay Drive (Output).** Connects to the Bias Relay coil (K2) and is controlled by $\overline{\text{BRC}}$.
15	LRC	**Loop Relay Control (Input).** A logic 1 activates $\overline{\text{LRD}}$. The Loop Relay (K1) is used for placing the Line Termination across Tip and Ring.

Pin Description (continued)

16	BRC	**Bias Relay Control (Input).** A logic 1 activates $\overline{\text{BRD}}$. The Bias Relay (K2) is used to connect Tip and Ring to -48V via bias resistors. This input should be connected to logic 0 when not used.
17	$\overline{\text{GRC}}$	**Ground Ring Relay Control (Input).** A logic 0 activates $\overline{\text{GRD}}$. The Ground Ring Lead Relay (K3) is used to connect Ring to AGND via a bias resistor. This input should be connected to logic 1 when not used.
18	AGND	**Analog Ground.** 4-Wire Ground. Normally connects to system ground. This pin must be connected to the system ground in Ground Start applications.
19	NATT	**Network Balance AT&T Node.** Used when setting the Network Balance Impedance to AT&T compromise network.
20	N1	**Network Balance Node 1.** Used when a Network Balance Impedance which differs from the Input Impedance is required or when NATT is used.
21	N2	**Network Balance Node 2.** Used when a Network Balance Impedance which differs from the Input Impedance is required.
22	Z900	**Input Impedance 900Ω Node.** Connects to Z1 when selecting an Input Impedance of 900Ω.
23	Z1	**Input Impedance Node 1.** Used when setting the Input Impedance.
24	Z2	**Input Impedance Node 2.** Used when a user defined Input Impedance is required.
25	TX	**Transmit (Output).** 4-Wire ground (AGND) referenced analog output.
26	RX	**Receive (Input).** 4-Wire ground (AGND) referenced analog input.
27	GTX0	**Transmit Gain Node 0.** Connects to GTX1 for 0dB transmit gain.
28	GTX1	**Transmit Gain Node 1.** Connects to GTX0 for 0dB transmit gain or via a resistor to AGND for transmit gain programming.
29	GRX0	**Receive Gain Node 0.** Connects to GRX1 for 0dB receive gain.
30	GRX1	**Receive Gain Node 1.** Connects to GRX0 for 0dB receive gain or via a resistor to AGND for receive gain programming.
31	IC	**Internal Connection.** No connection should be made to this pin.
32	Z600	**Loop Impedance 600Ω Node.** Connects to Z1 when selecting an Input Impedance of 600Ω.
33	NS	**Network Balance Setting (Input).** Used to select the Network Balance impedance.
34	$\overline{\text{TG}}$	**Tip Lead Ground Detect (Output).** A logic 0 output indicates that the Tip lead is at ground (AGND) potential.
35	$\overline{\text{RL}}$	**Reverse Loop Detect (Output).** In the on-hook state, a logic 0 output indicates that reverse loop battery is present. In the off-hook state, a logic 0 output indicates that reverse loop current is present.
36	$\overline{\text{RV}}$	**Ringing Voltage Detect (Output).** A logic low indicates that ringing voltage is across the Tip and Ring leads.
37	$\overline{\text{FL}}$	**Forward Loop Detect (Output).** In the on-hook state, a logic 0 output indicates that forward loop battery is present. In the off-hook state, a logic 0 output indicates that forward loop current is present.
38	$\overline{\text{RG}}$	**Ring Lead Ground Detect (Output).** A logic 0 output indicates that the Ring lead is at ground (AGND) potential.
39	VEE	**Negative Supply Voltage.** -5V DC
40	VCC	**Positive Supply Voltage.** +5V DC

Functional Description

The MH88632B is a Central Office Interface Circuit (COIC). It is used to correctly terminate a Central Office 2-Wire telephone line. The device provides a signalling link and a 2-4 Wire line interface between the telephone line and subscriber equipment. The subscriber equipment can include Private Branch Exchanges (PBX's), Key Telephone Systems, Terminal Equipment, Digital Loop Carriers and Wireless Local Loops.

All descriptions assume that the device is connected as in the application circuit shown in Figure 3.

Isolation Barrier

The MH88632B provides an isolation barrier which is designed to meet FCC Part 68 (November 1987) Leakage Current Requirements.

External Protection

An external protection circuit may be required to assist in preventing overvoltage damage to the device and the subscriber equipment in which it is incorporated. The type of protection required is dependant on the application and the regulatory standards. Please contact the governing regulatory body and local approvals testing houses for more assistance.

This protection is shown in block form in Figure 3.

Suitable Markets

The programmability offered by the MH88632B enhances its suitability for use throughout the world. However, care should be taken that all regulatory requirements, e.g. isolation and DC termination, are being fulfilled for the particular application in which the device is intended to be used.

Line Termination

When LRC is at a logic 1, $\overline{\text{LRD}}$ is taken to a logic 0 which energizes the Loop Relay (K1), connecting XLA to XLB and XLC to XLD. This places a line termination across Tip and Ring. The device can be considered to be in an off-hook state and DC loop current will flow. The line termination consists of a DC resistance and an AC impedance. When LRC is at a logic 0, the Line Termination is removed from across Tip and Ring.

An internal Dummy Ringer is permanently connected across Tip and Ring which is a series AC load of (17kΩ+330nF). This represents a mechanical telephone ringer and allows ringing voltages to be sensed. This load can be considered negligible when the line has been terminated.

Depending on the Network Protocol being used the line termination can seize the line for an outgoing call, terminate an incoming call, or if applied and disconnected at the correct rate can be used to generate dial pulse signals.

The DC line termination circuitry provides the line with an active DC load which is equivalent to a DC resistance of between 190Ω and 290Ω dependant on the loop current.

AC Input Impedance

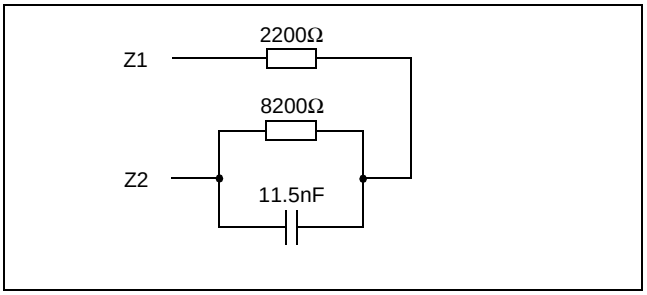
The Input Impedance (Zin) is the AC impedance that the MH88632B places across Tip and Ring in order to terminate the telephone line. It can be user defined, set to 600Ω or set to 900Ω.

To select a 600Ω Input Impedance, Z1 should be connected directly to Z600. No connection should be made to Z2 or Z900.

To select a 900Ω Input Impedance, Z1 should be connected directly to Z900. No connection should be made to Z2 or Z600.

In order to user define the Input Impedance an impedance network should be placed between Z1 and Z2. This should be equivalent to 10 times the required Input Impedance and must be greater than 100Ω at 3.4kHz. No connection should be made to Z600 or Z900.

For example, to implement an Input Impedance of 220Ω+(820Ω//115nF) an impedance network of 2200Ω+(8200Ω//11.5nF) should be connected between Z1 and Z2 as shown below.



User defined Input Impedances can be used to satisfy most national requirements. See Table 1.

All connections should be kept as short as possible.

Network Balance Impedance

The MH88632B's Network Balance Impedance can be selected to mirror the Input Impedance, to be AT&T compromise or set to a user defined value. Thus, the Network Balance Impedance can comply with most national requirements.

With NS at logic 0, the Network Balance Impedance is selected to mirror the Input Impedance of the device. No connection should be made to NATT, N1 and N2.

To select a Network Balance Impedance equal to AT&T Compromise (i.e. 350Ω+(1kΩ//210nF)), NS should be set to a logic 1 and a direct connection made between NATT and N1. No connection should be made to N2.

To set a user defined Network Balance Impedance NS is set to a logic 1. An impedance network which is 10 times the required Network Balance Impedance must be placed between N1 and AGND. Another impedance network must be placed between N1 and N2 which is 10 times the selected input impedance of the device.

For example, to implement a Network Balance Impedance of 220Ω+(820Ω//115nF), an impedance network of 2200Ω+(8200Ω//11.5nF) must be connected between N1 and AGND. An impedance network equal to 10 times the selected Input Impedance must be connected between N1 and N2. See Table 2.

All connections should be kept as short as possible.

2-4 Wire Conversion

The device converts the balanced 2-Wire input, presented by the line at Tip and Ring, to a ground referenced signal at TX. This circuit operates with or without loop current; signal reception with no loop current is required for on-hook reception enabling the detection of Caller Line Identification signals.

Conversely the device converts the ground referenced signal input at RX, to a balanced 2-Wire signal across Tip and Ring.

The 4-Wire side (TX and RX) can be interfaced to a filter/codec, such as the Zarlink MT896X, for use in digital voice switched systems.

During full duplex transmission, the signal at Tip and Ring consists of both the signal from the device to the line and the signal from the line to the device. The signal input at RX, being sent to the line, must not appear at the output TX. In order to prevent this, the device has an internal cancellation circuit. The measure of attenuation is Transhybrid Loss (THL).

Programmable Transmit and Receive Gain

The Transmit Gain (GTX) of the MH88632B is the gain from the balanced signal across Tip and Ring to the ground referenced signal at TX. It is programmed by making a connection to GTX1. A direct connection from GTX1 to GTX0 selects a gain of 0dB. A direct connection from GTX1 to AGND selects a gain of +6dB. Other gains can be programmed by connecting a resistor (R_{TX}) between GTX1 and AGND. The value of resistor is selected using the following formulae.

$$R_{TX} = \frac{5000}{10^{(-GTX/20)} - 0.5}$$

$$GTX = -20 \log\left(0.5 + \frac{5000}{R_{TX}}\right)$$

The Receive Gain (GRX) of the MH88632B is the gain from the ground referenced signal at RX to the balanced signal across Tip and Ring. It is programmed by making a connection to GRX1. A direct connection from GRX1 to GRX0 selects a gain of 0dB. A direct connection from GRX1 to AGND selects a gain of +6dB. Other gains can be programmed by connecting a resistor (R_{RX}) between GRX1 and AGND. The value of resistor is selected using the following formulae.

$$R_{RX} = \frac{5000}{10^{(-GRX/20)} - 0.5}$$

$$GRX = -20 \log\left(0.5 + \frac{5000}{R_{RX}}\right)$$

For the correct programming of Transmit and Receive Gains the selected Input Impedance must match the specified telephone line characteristic impedance.

Both Gains are programmable in the range -12dB to +6dB. This wide range is capable of accommodating most system loss plans. See Tables 3 and 4.

Caller Line Identification

Caller Line Identification (CLI) provides the called party with the calling party telephone number. The Central Office will utilise the voice path of a regular loop-start telephone line when the MH88632B is in the on-hook state. The CLI information is typically a Frequency Shift Keyed (FSK) data signal which is output at TX.

Supervisory Features

Line Status Detection Outputs

The MH88632B supervisory circuitry provides the signalling status outputs which are monitored by the system controller. The supervisory circuitry is capable of detecting: ringing voltage; forward and reverse loop battery; forward and reverse loop current; grounded tip lead; and grounded ring lead.

If these Supervisory Features and the Control Features are used as indicated in Figure 3 they can implement common Network Protocols such as Loop-Start Signalling and Ground-Start Signalling.

1. Ringing Voltage Detect Output ($\overline{RV}$)

The $\overline{RV}$ output provides a logic 0 when ringing voltage is detected across Tip and Ring. This detector includes a filter which ensures that the output toggles at the ringing cadence and not at the ringing frequency. Typically this output switches to a logic 0 after 50ms of applied ringing voltage and remains at a logic 0 for 50ms after ringing voltage is removed.

2. Forward Loop and Reverse Loop Detect Outputs (FL & RL)

The $\overline{FL}$ output provides a logic 0 when either forward loop battery or forward loop current is detected, that is the Ring pin voltage is negative with respect to Tip pin voltage.

The $\overline{RL}$ output provides a logic 0 when either reverse loop battery or reverse loop current is detected, that is the Tip pin voltage is negative with respect to Ring pin voltage.

3. Tip Ground and Ring Ground Detect Outputs (TG & RG)

The $\overline{TG}$ output provides a logic 0 when the Tip pin is at ground (AGND) potential.

The $\overline{RG}$ output provides a logic 0 when the Ring pin is at ground (AGND) potential.

Control Inputs

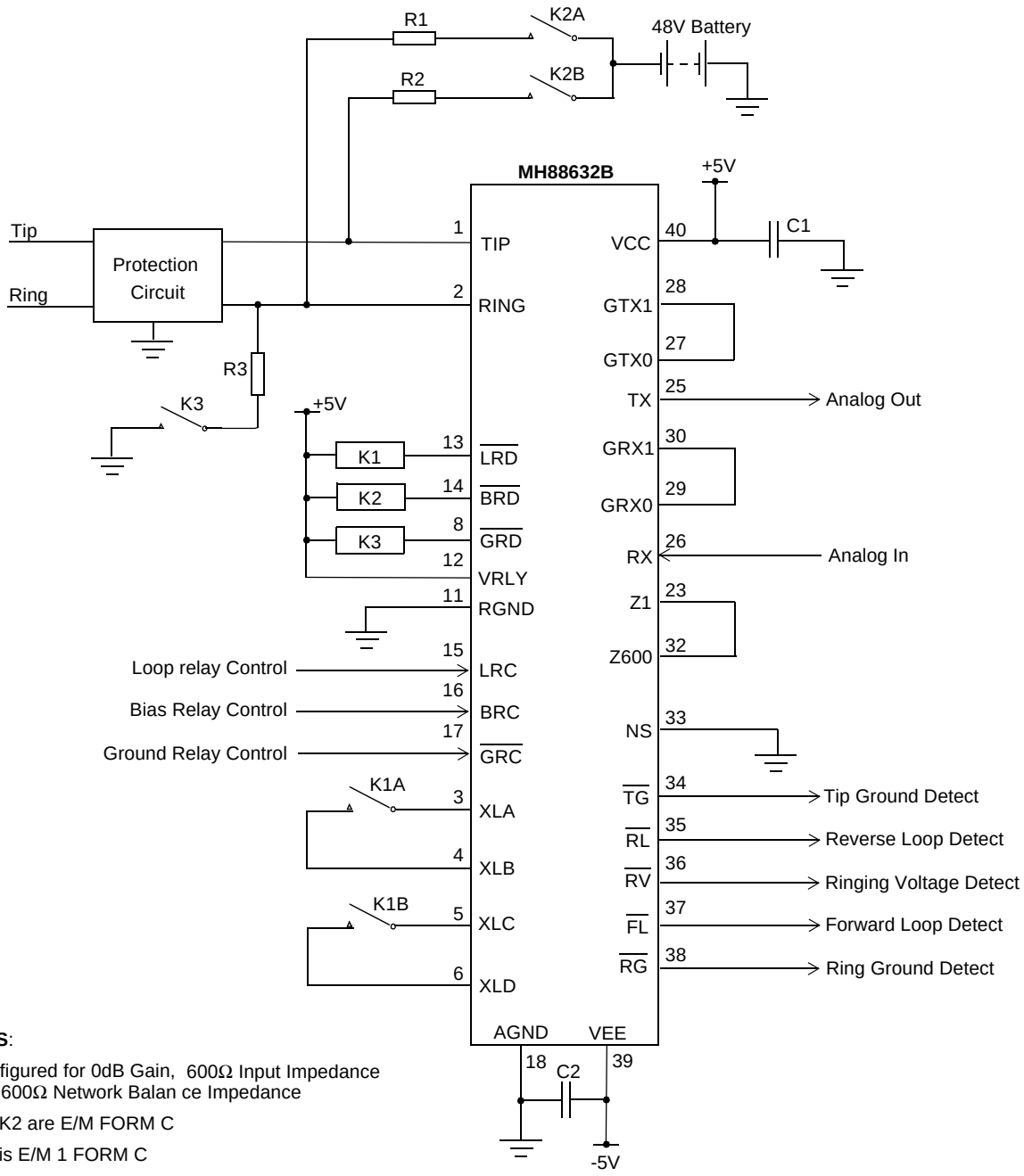
The MH88632B accepts control signals from the system controller at the inputs Loop Relay Control (LRC), Bias Relay Control (BRC) and Ground Ring Relay Control ($\overline{GRC}$). These energize the relay drive outputs Loop Relay Drive (LRD), Bias Relay Drive ($\overline{BRD}$) and Ground Ring Relay Drive ($\overline{GRD}$) respectively. Each output is active low and has an internal clamp diode to VRLY.

The intended use of each of these relay drivers is shown in Figure 3. LRC is being used to add and remove the Line Termination from across Tip and Ring. BRC is used to connect Tip and Ring to -48V via external bias resistors. $\overline{GRC}$ is controlling the connection of Ring to AGND via an external bias resistor.

If these Control Features and the Supervisory Features are used as intended they can be used to implement common Network Protocols such as Loop-Start Signalling and Ground-Start Signalling.

Mechanical Information

See Figure 9 for mechanical specifications for the MH88632B.



NOTES:

1) Configured for 0dB Gain, 600Ω Input Impedance and 600Ω Network Balan ce Impedance
2) K1, K2 are E/M FORM C
3) K3 is E/M 1 FORM C
4) R1 = R2 = 30.9kΩ, 1%, 5W
5) R3 = 470Ω, 5%, 5W
6) K2, K3, R1, R2, R3 are required for Ground Start only
7) C1, C2 are decoupling capacitors

Figure 3 - Typical Combined Loop Start and Ground Start Appliation Circuit

Input Impedance Settings

Z2	Z1	Z600	Z900	Resulting input impedance (Zin)
NA	Connect Z1 to Z600		NA	600Ω
NA	Connect Z1 to Z900	NA	Connect Z1 to Z900	900Ω
Connect network from Z1 to Z2		NA	NA	0.1 x impedance between Z1 & Z2

Note: NA indicates high impedance (10kΩ) connection to this pin does not effect the resulting Input Impedance

Network Balance Settings

NS (Input)	N2	N1	NATT	Resulting input impedance (Zin)
Low	NA	NA	NA	Equivalent to Zin
High	NA	Connect N1 to NATT		AT&T compromise (350Ω + 1kΩ // 210nF) Zin must be 600Ω
High	Connect network from N1 to AGND equivalent to 10 x NETBAL. Connect network from N1 to N2 equivalent to 10 x Zin.		NA	0.1 x impedance between N1 & N2

Notes: NA indicates high impedance (10kΩ) connection to this pin does not effect the resulting Network Balance Impedance.
Low indicates Logic 0.
High indicates Logic 1.

Transmit Gain Programming

Transmit Gain (dB)	R_{TX} Resistor Value (Ω)	Notes
+6.0	No Resistor	
+4.0	38.3k	Results in 0dB overall gain when used with Zarlink A-law codec (i.e. MT8967)
+3.7	32.4k	Results in 0dB overall gain when used with Zarlink μ-law codec (i.e. MT8966)
0.0	GTX0 to GTX1	
-3.0	5.49k	
-6.0	3.32k	
-12.0	1.43k	

Note: Overall gain refers to the receive path of PCM to 2-Wire.

Receive Gain Programming

Receive Gain (dB)	R_{RX} Resistor Value (Ω)	Notes
+6.0	No Resistor	
0.0	GRX0 to GRX1	
-3.0	5.49k	
-3.7	4.87k	Results in 0dB overall gain when used with Zarlink A-law codec (i.e. MT8967)
-4.0	4.64k	Results in 0dB overall gain when used with Zarlink μ-law codec (i.e. MT8966)
-6.0	3.32k	
-12.0	1.43k	

Note: Overall gain refers to the transmit path of 2-wire to PCM.

Absolute Maximum Ratings*

	Parameter	Sym	Min	Max	Units	Comments
1	DC Supply Voltage	V_{CC} V_{EE}	-0.3 0.3	7 -7	V V	
2	DC Relay Voltage	V_{RLY}	-0.3	20	V	
3	Storage Temperature	T_S	-55	+125	°C	
4	Ring Trip Current	I_{TRIP}		180	mArms	250ms 10% duty cycle or 500ms single shot

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Sym	Min	Typ‡	Max	Units	Comments
1	DC Supply Voltage	V_{CC} V_{EE}	4.75 -4.75	5 -5	5.25 -5.25	V V	
2	DC Relay Voltage	V_{RLY}		5	15	V	
3	Operating Temperature	T_{OP}	0	25	70	°C	

‡Typical figures are at 25× C with nominal ±5V supplies and are for design aid only.

DC Electrical Characteristics†

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Current	I_{DD} I_{EE}		14 10	15 13	mA mA	
2		Power Consumption	PC		120	147	mW	
3	$\overline{FL}$ $\overline{RL}$ $\overline{RG}$ $\overline{TG}$ RV	Low Level Output Voltage High Level Output Voltage	V_{OL} V_{OH}	 2.4		0.5	V V	I_{OL} = 4mA I_{OH} = 0.4mA
4	$\overline{LRD}$ $\overline{BRD}$ GRD	Sink Current, Relay to V_{CC} Clamp Diode Current	I_{OL} I_{CD}	100 150			mA mA	V_{OL} = 0.35V
5	NS LRC $\overline{BRC}$ GRC	Low Level Input Voltage High Level Input Voltage	V_{IL} V_{IH}	 2		0.8	V V	
6	NS LRC $\overline{BRC}$ GRC	High Level Input Current Low Level Input Current	I_{IH} I_{IL}			1 1	µA µA	

† Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

Loop Electrical Characteristics†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Ringing Voltage	V_R	20	90	130	Vrms	
2	Ringing Frequency		17	20	68	Hz	
4	Operating Loop Current		15		90	mA	
5	Off-Hook DC Resistance		190	275	290	Ω	
6	Leakage Current (Tip-Ring to AGND)				7	mArms	@1000VAC
7	$\overline{FL}$ Threshold Tip-Ring Voltage Detect (On-hook) Tip-Ring Current Detect (Off-hook)		 12 6		 21 12	 V mA	 LRC = 0V LRC = 5V
8	$\overline{RL}$ Threshold Tip-Ring Voltage Detect (On-hook) Tip-Ring Current Detect (Off-hook)		 -12 -6		 -21 -12	 V mA	 LRC = 0V LRC = 5V
9	$\overline{TG}$ and $\overline{RG}$ Detect Threshold		-12		-14	V	

=Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡Typical figures are at 25°C with nominal ±5V supplies and are for design aid only.

AC Electrical Characteristics†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	2-wire Input Impedance Note 1	Zin		600 900 Ext.		Ω Ω Ω	
2	Return Loss at 2-Wire (Zin = 600Ω)	RL	 20 26 20	 40 48 46		 dB dB dB	Test Circuit Fig. 6 200-500 Hz 500-1000 Hz 1000-3400 Hz
3	Return Loss at 2-Wire (Zin = 900Ω)	RL	22 26 24			dB dB dB	200-500 Hz 500-1000 Hz 1000-3400 Hz
4	Longitudinal to Metallic Balance Note 2		 58 58 55 53 51	 64 63 61 57 54		 dB dB dB dB dB	Test Circuit Fig. 8 200 Hz 1000 Hz 2000 Hz 3000 Hz 4000 Hz
5	Metallic to Longitudinal Balance Note 2		 60 40	 62 62		 dB dB	Test Circuit Fig. 7 200-1000 Hz 1000 -4000 Hz
6	Transhybrid Loss (Zin = Net = 600Ω) Note 2 & 3	THL	18 21	25 33		dB dB	200-3400 Hz 500-2500 Hz
7	Transhybrid Loss (Zin = Net = 900Ω) Note 2 & 3	THL	18 21			dB dB	200-3400 Hz 500 -2500 Hz
8	Transhybrid Loss (Zin =600Ω, Net = AT&T) Note 2 & 3	THL	18 21	 30		dB dB	200-3400 Hz 500-2500 Hz
9	Input Impedance At RX			10		kΩ	
10	Output Impedance at TX				5	Ω	
11	Transmit Gain, (2-Wire/TX): Default Gain(0dB) Programmable Range		 -0.2 -12	 0	 0.2 6	 dB dB	Test Circuit Fig. 5 Input 0.5V 1000Hz 1000Hz

AC Electrical Characteristics† (continued)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
12	Frequency response gain (relative to gain at 1kHz) Note 2		 -1.3 -0.3 -0.3 -0.7	 0 0 0 0	 0.1 0.1 0.1 0.1	 dB dB dB dB	Test Circuit Fig. 5 Input 0.5V 200 Hz 300 Hz 3000 Hz 3400 Hz
13	Receive Gain, (RX/2-Wire): Default Gain (0dB) Programmable Range		 -0.2 -12	 0 	 0.2 6	 dB dB	Test Circuit Fig. 4 Input 0.5V 1000Hz 1000Hz
14	Frequency response gain (relative to gain at 1kHz) Note 2		 -1.3 -0.3 -0.3 -0.7	 0 0 0 0	 0.1 0.1 0.1 0.1	 dB dB dB dB	Test Circuit Fig. 4 Input 0.5V 200 Hz 300 Hz 3000 Hz 3400 Hz
15	Signal Output Overload Level at 2-wire at TX		 4 4	 	 	 dBm dBm	THD < 5% Ref. 600Ω Ref. 600Ω
16	Total Harmonic Distortion at 2-Wire at TX	THD		 0.2 0.4	 1 1	 % %	Input 0.5V, 1kHz
17	Idle Channel Noise at 2-Wire at TX	Nc		 10 11	 13 13	 dBrn C dBrn C	
18	Common Mode Rejection Ratio	CMRR	48	65		dB	540Hz Test Circuit Fig. 8
19	Power Supply Rejection Ratio at 2-Wire and TX V_{CC} V_{EE}	PSRR	 20 20	 42 28	 	 dB dB	Ripple 0.1V, 1kHz
20	On-Hook Transmit Gain (2-Wire/TX) Default Gain 0dB Programmable Range		 -1 -12	 0 	 1 6	 dB dB	 1000Hz 1000Hz
21	On-Hook frequency Response Gain (relative to off-hook gain)		-1	0	1	dB	Input 0.5V, 1kHz

=Electrical Characteristics are over recommended operating conditions unless otherwise stated
‡Typical figure are at 25°C with nominal ±5V supplies and are for design aid only
*All test conditions use a test source impedance which matches the device's input impedance
dBm is referenced to 600Ω unless otherwise stated
Notes: Impedance set by external network equal to 10 times the required input impedance
Test conditions use a transmit and receive gain set to 0dB default
"Net" indicates network balance impedance

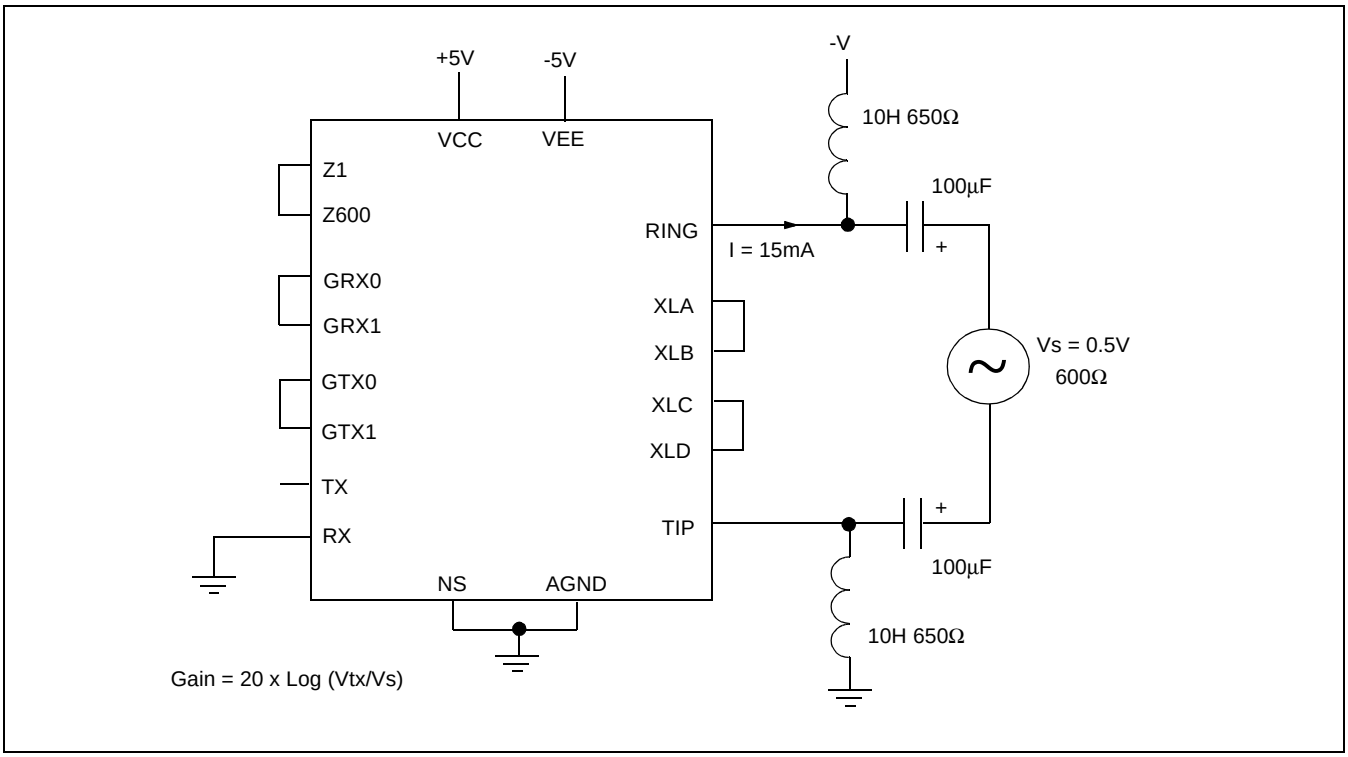


Figure 4 - 2-4 Wire Gain Test Circuit

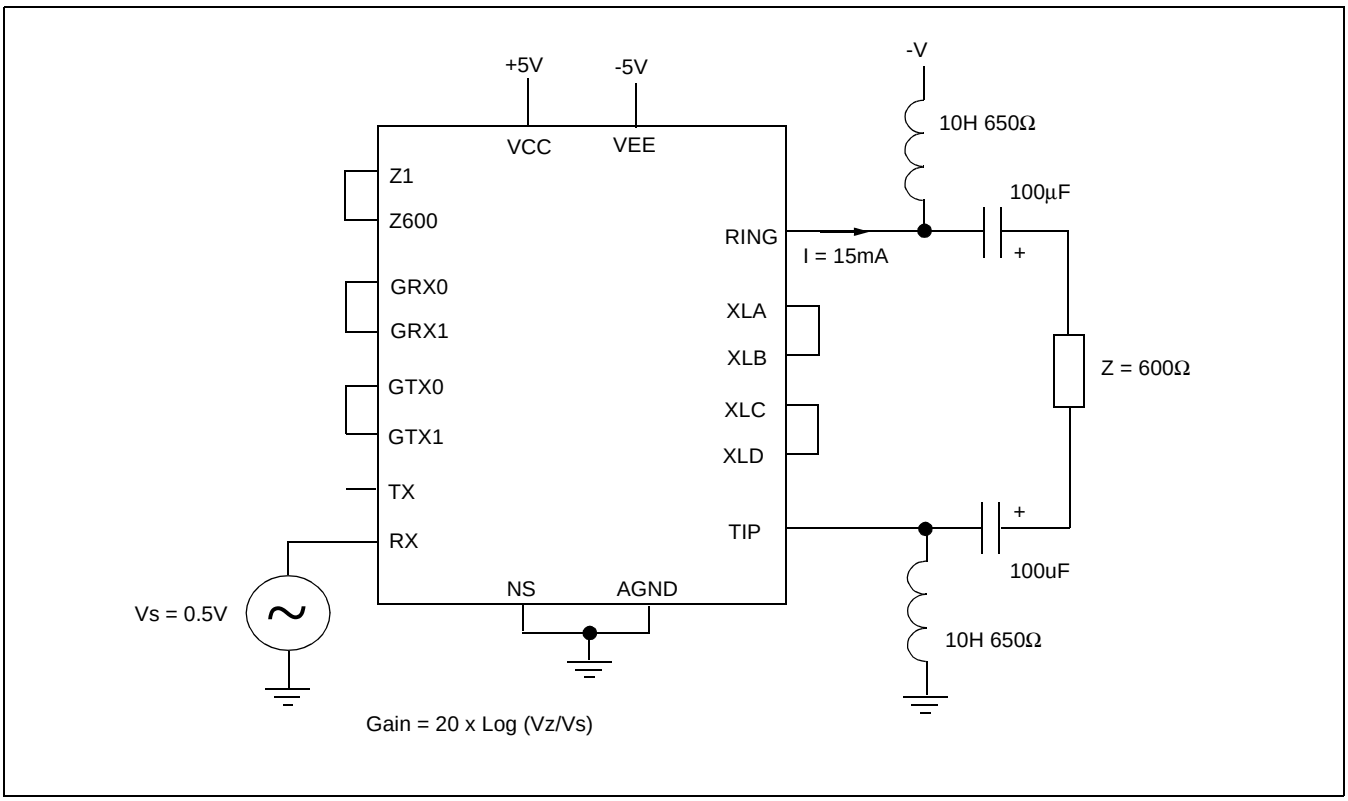


Figure 5 - 4-2 Wire Test Circuit

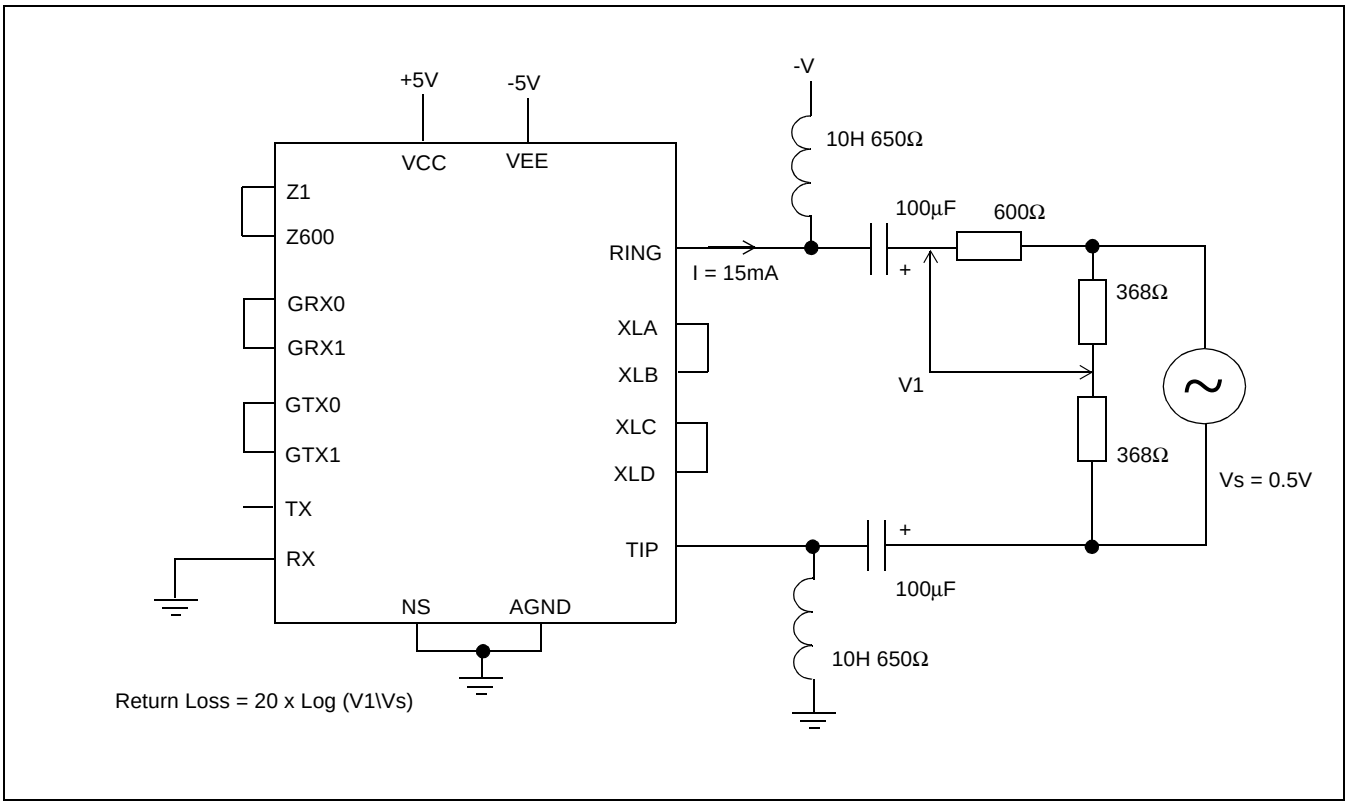


Figure 6 - Return Loss Test Circuit

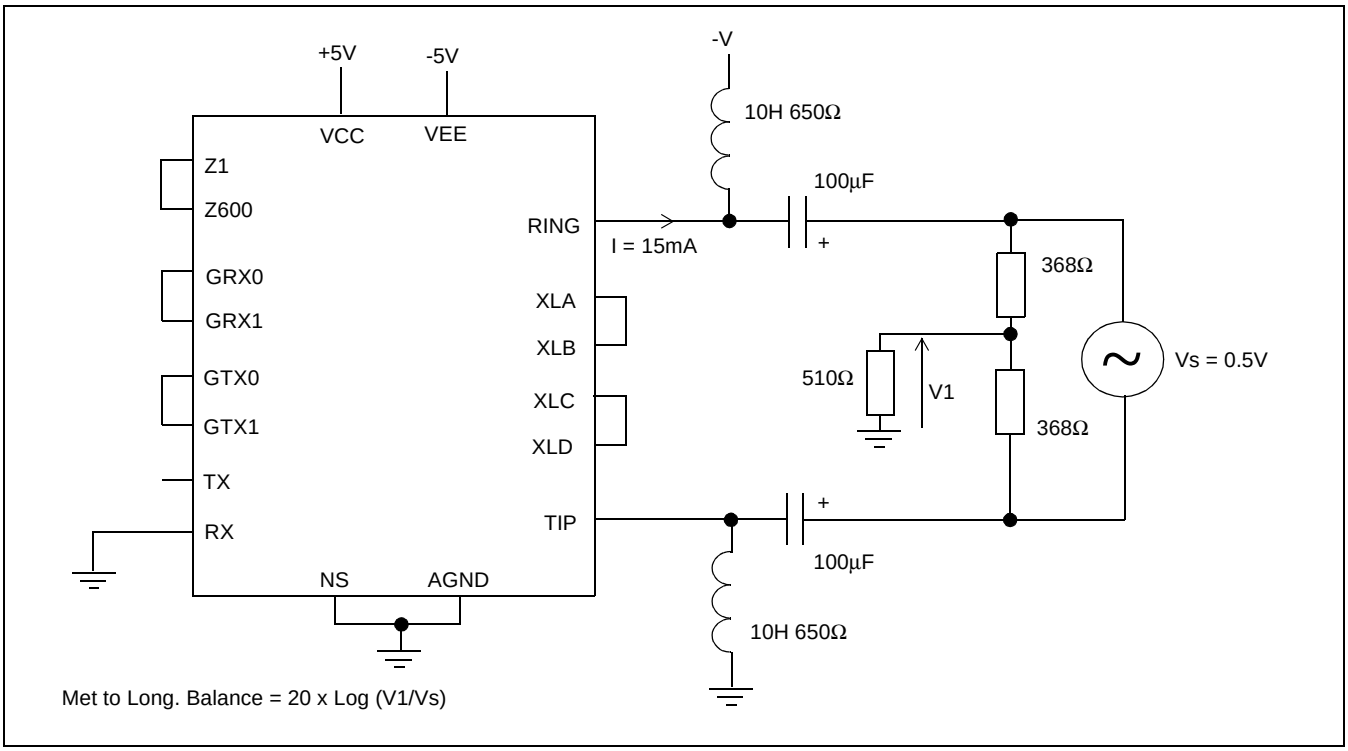


Figure 7 - Metallic to Longitudinal Balance Test Circuit

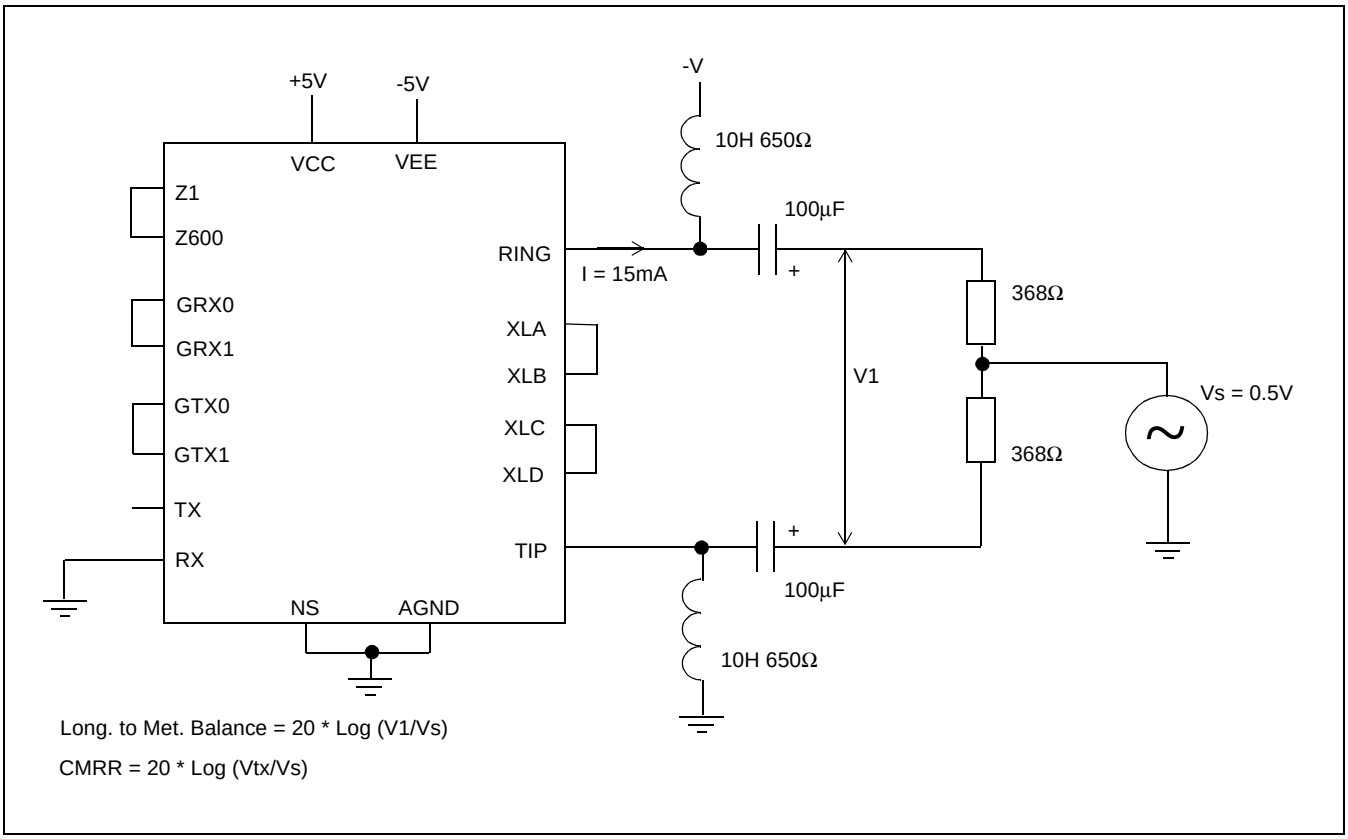


Figure 8 - Longitudinal to Metallic Balance and CMRR Test Circuit

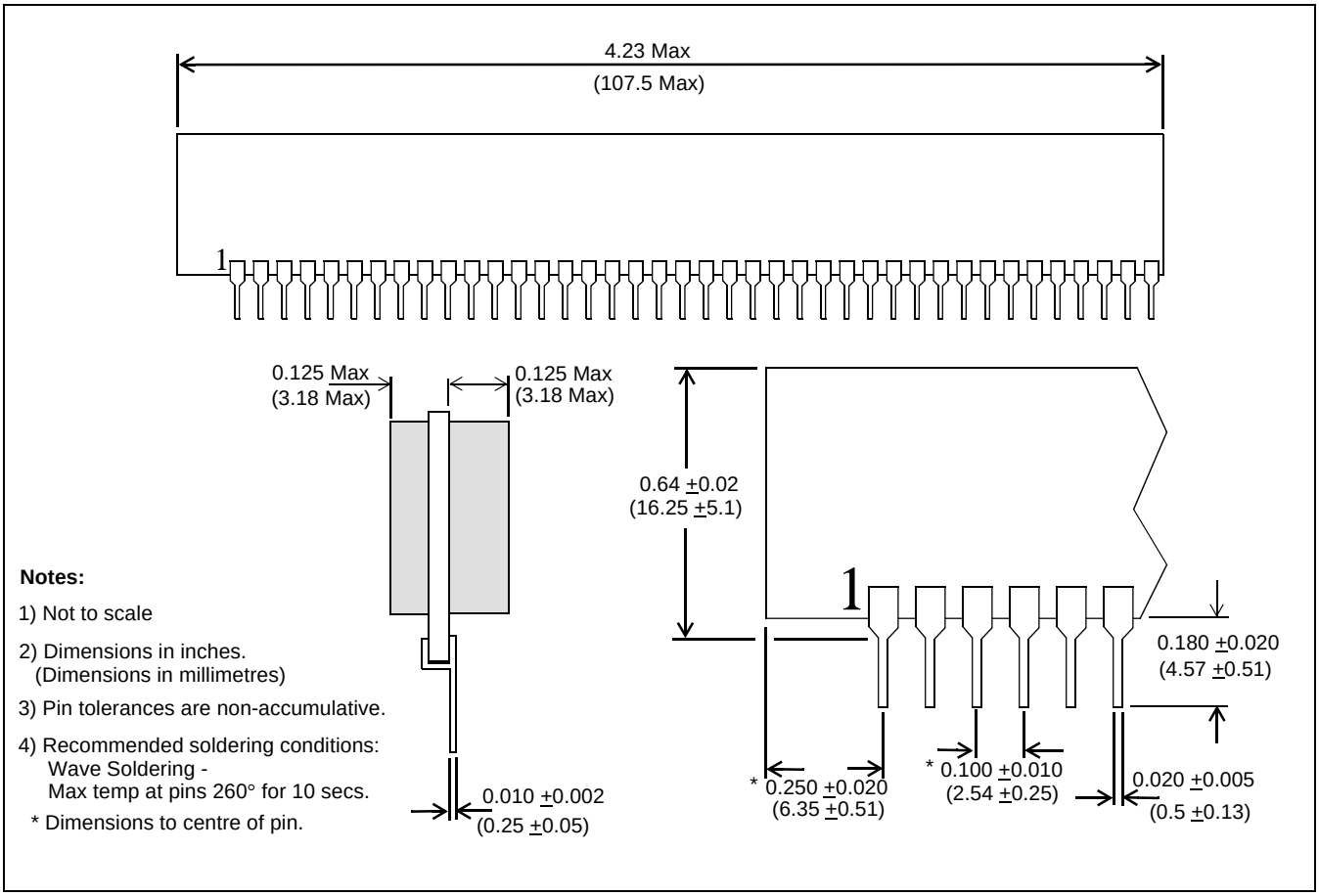


Figure 9 - MH88632B Mechanical Information

Notes:

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