HI3050

Triple 10-Bit, 50 MSPS, High Speed, 3-Channel D/A Converter

August 1997

Features

- **Resolution . . . . . .Triple 10-Bit**
- **Throughput Rate 50MHz**
- **3-Channel, RGB, I/O**
- **RS-343A/RS-170 Compatible Outputs**
- **Low Power Consumption (Typ) 500mW**
- **Differential Linearity Error . . . . . ±0.5 LSB**
- **Low Glitch Energy**
- **CMOS Compatible Inputs**
- **Direct Replacement for Sony CXD2308**

Applications

- **NTSC, PAL, SECAM Displays**
- **High Definition Television (HDTV)**
- **Presentation and Broadcast Video**
- **Image Processing**
- **Graphics Displays**

Description

The HI3050 is a triple, 10-bit D/A converter, fabricated in a silicon gate CMOS process, ideally suited for RGB video applications.

The converter incorporates three 10-bit input data registers with a common blanking capability, forcing all outputs to 0mA. The HI3050 features low glitch, high impedance current outputs and single 5V supply operation. Low current inputs accept standard TTL/CMOS levels. The architecture is a current cell arrangement providing low differential and integral linearity errors.

The HI3050 requires a 2V external reference and a set resistor to control the output current. The HI3050 also features a chip enable/disable pin for reducing power consumption (<5mW) when the part is not in use.

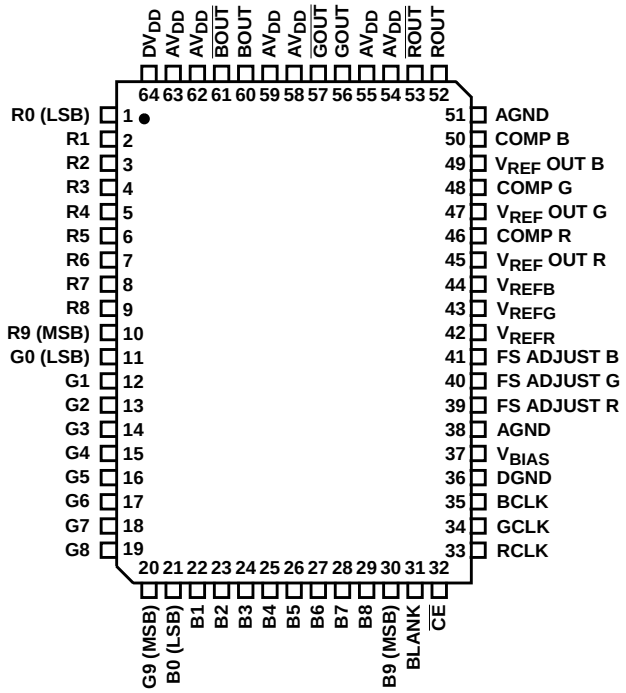
The HI3050 can generate RS-343A and RS-170 compatible video signals into doubly terminated and singly terminated 75Ω loads.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3050JCQ	-20 to 75	64 Ld MQFP	Q64.14x20-S

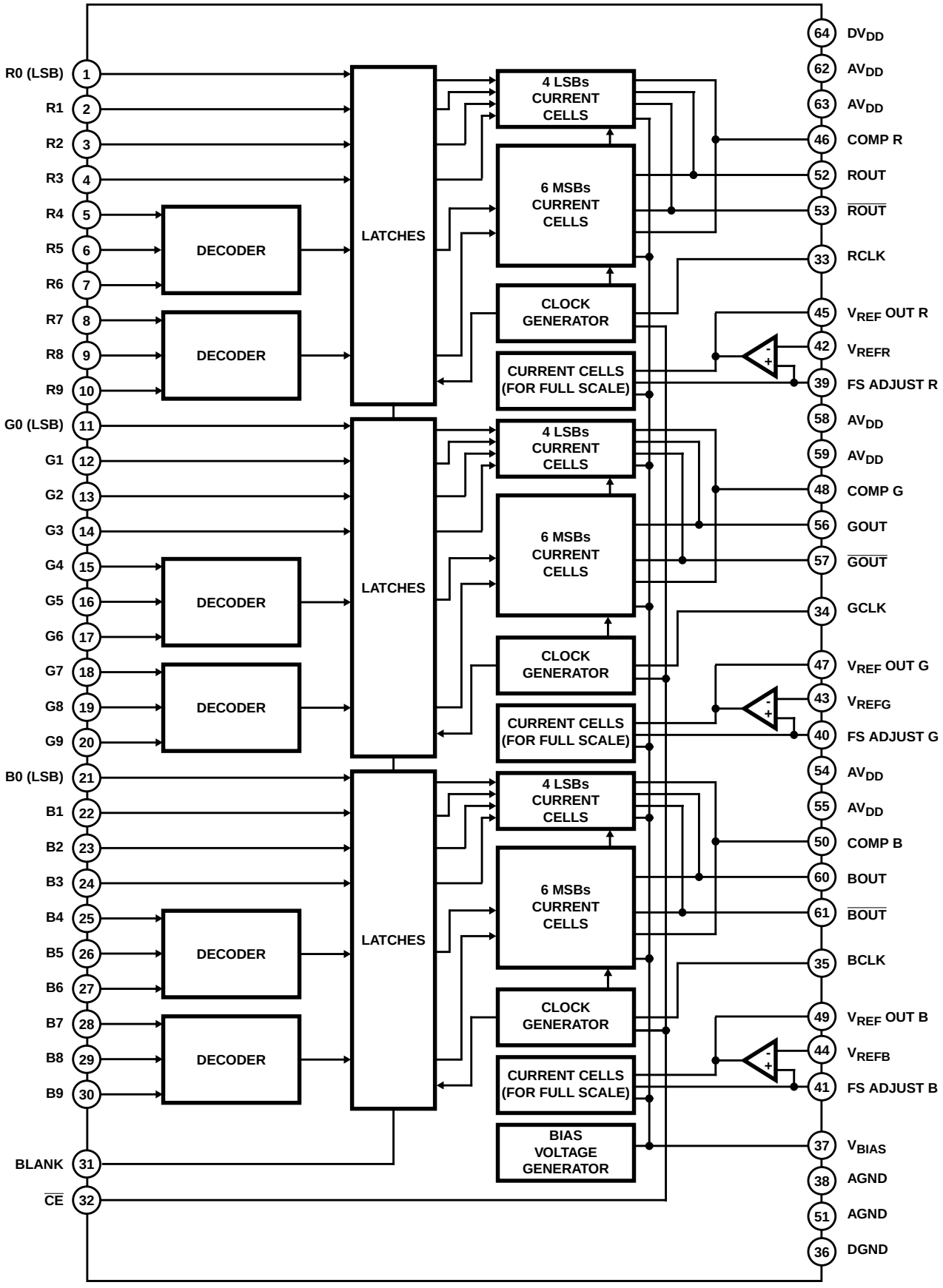
Pinout

HI3050 (MQFP)
TOP VIEW

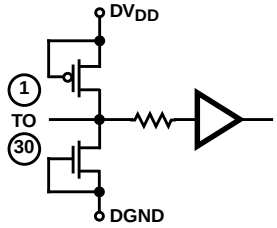
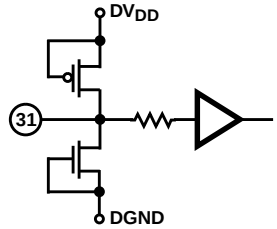
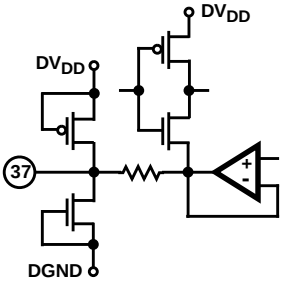
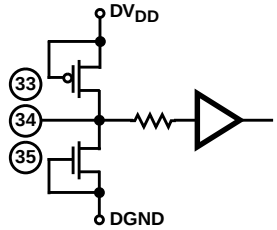
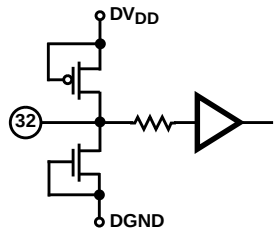


File Number **3936.2**

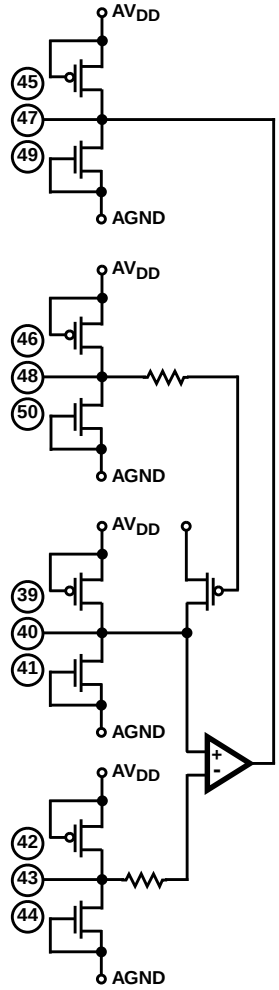
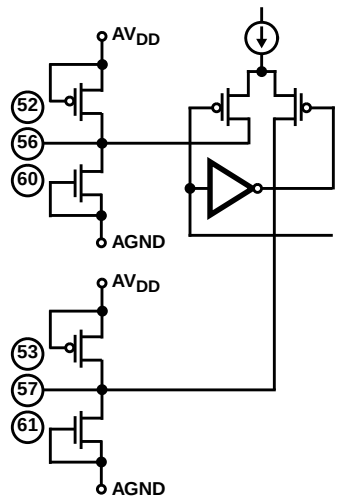
Functional Block Diagram



Pin Descriptions and Equivalent Circuits

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 - 10	R0 - R9		Digital Inputs.
11 - 20	G0 - G9		
21 - 30	B0 - B9		
31	BLANK		Output Blanking Input. High: Outputs Set to 0mA. Low: Normal Output Operation.
37	V_{BIAS}		Internal Bias Decoupling. Connect a 0.1µF decoupling capacitor to DGND.
33	RCLK		Clock Inputs. All input pins are TTL/CMOS compatible.
34	GCLK		
35	BCLK		
36	DGND		Digital Ground.
38, 51	AGND		Analog Ground.
32	$\overline{CE}$		Chip Enable pin. High: Part Disabled Low: Part Enabled
54, 55, 58, 59, 62, 63	AV_{DD}		Analog Power Supply.

Pin Descriptions and Equivalent Circuits (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
45	V_{REF} OUT R		Reference Output. Typically connected to the Reference Decoupling inputs (COMP R, COMP G, COMP B). See Figures 11 and 12 for various configurations.
47	V_{REF} OUT G		
49	V_{REF} OUT B		
46	COMP R		Reference Decoupling. Connect a decoupling capacitor (0.1µF) to reduce noise on reference to AV_{DD}.
48	COMP G		
50	COMP B		
39	FS ADJUST R		Full Scale Adjust. Typically connect a 1.2kΩ resistor, R_{SET}, to AGND. R_{SET} is used to determine full scale output current.
40	FS ADJUST G		
41	FS ADJUST B		
42	V_{REFR}		Voltage Reference Input. Typically set to 2V and determines full scale output current. $I_{OUT}(\text{Full Scale}) = \frac{V_{REF}}{R_{SET}} \times 16$
43	V_{REFG}		
44	V_{REFB}		
52	ROUT		Current Outputs.
56	GOUT		
60	BOUT		
53	$\overline{\text{ROUT}}$		Inverted Current Outputs.
57	$\overline{\text{GOUT}}$		
61	$\overline{\text{BOUT}}$		
64	DV_{DD}		Digital Power Supply.

Absolute Maximum Ratings $T_A = 25^oC$

Digital Supply Voltage, DV_{DD} to DGND . . . . . +7V
Analog Supply Voltage, AV_{DD} to AGND . . . . . +7V
Digital Input Voltages . . . . . DV_{DD} to DGND
Analog Output Current (I_{OUT}) 30mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 80
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

Operating Conditions

Supply Voltage, AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Clock Pulse Width (t_{PW1}, t_{PW0}) . . . . . 10ns (Min)
Temperature Range (T_{OPR}) . . . . . -20^oC to 75^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications AV_{DD} = +5V, DV_{DD} = +5V, f_{CLK} = 50MHz, R_L = 75Ω, V_{REF} = 2V, R_{SET} = 1.2kΩ, $T_A = 25^oC$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		-	10	-	Bits
Maximum Conversion Speed		50	-	-	MSPS
Integral Linearity Error, INL	"Best Fit" Straight Line	-2.0	-	2.0	LSB
Differential Linearity Error, DNL		-0.5	-	0.5	LSB
Output Offset Voltage, V_{OS}		-	-	1	mV
Output Full Scale Ratio Error, F_{SRE}	(Note 2)	0	1.5	3	%
Full Scale Output Current, I_{FS}		-	27	30	mA
Full Scale Output Voltage, V_{FS}		1.8	1.9	2.0	V
Output Voltage Compliance Range		-	2.5	-	V
DYNAMIC CHARACTERISTICS					
Glitch Energy, GE		-	50	-	pV/s
Settling Time	I_{OUT} = 13.5mA	-	40	-	ns
Crosstalk	10MHz Output Sine Wave	-	50	-	dB
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_{IH}		-	-	5	µA
Input Logic Current, I_{IL}		-5	-	-	µA
Digital Input Capacitance, C_{IN}		-	10	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1	-	5	7	ns
Data Hold Time, t_{HLD}	See Figure 1	-	1	3	ns
Propagation Delay Time, t_{PD}	See Figure 1	-	10	-	ns
Clock Pulse Width, t_{PW1}, t_{PW0}	See Figure 1	10	-	-	ns
POWER SUPPLY CHARACTERISITICS					
Total Supply Current, AI_{DD} + DI_{DD}		-	100	110	mA
Analog Supply Current, AI_{DD}		-	92	-	mA
Digital Supply Current, DI_{DD}		-	8	-	mA
Power Dissipation		-	500	550	mW

NOTE:

2. Configured for Common Reference.

$$F_{SRE} = \left| \frac{\text{Full Scale Voltage of Channel}}{\text{Average Full Scale Voltage of All Channels}} - 1 \right| \times 100\%$$

Timing Diagram

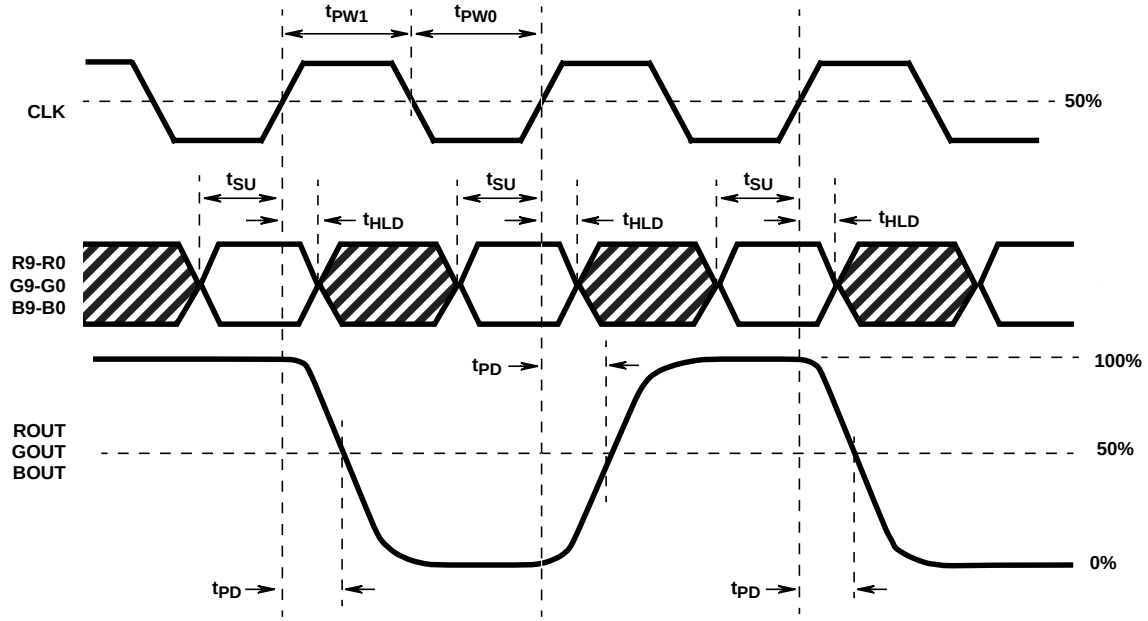


FIGURE 1. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

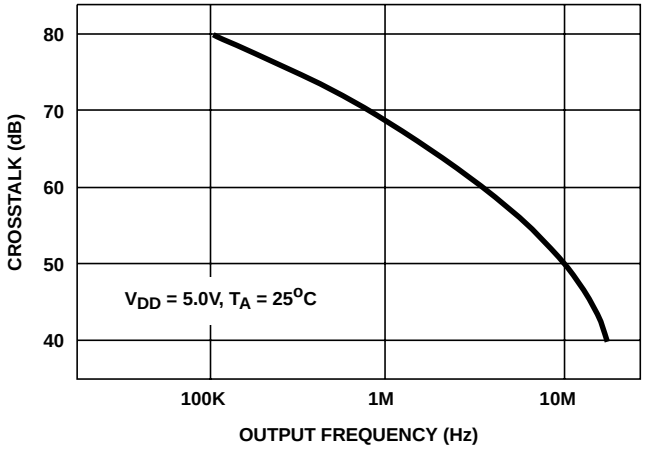


FIGURE 2. CROSSTALK vs OUTPUT FREQUENCY

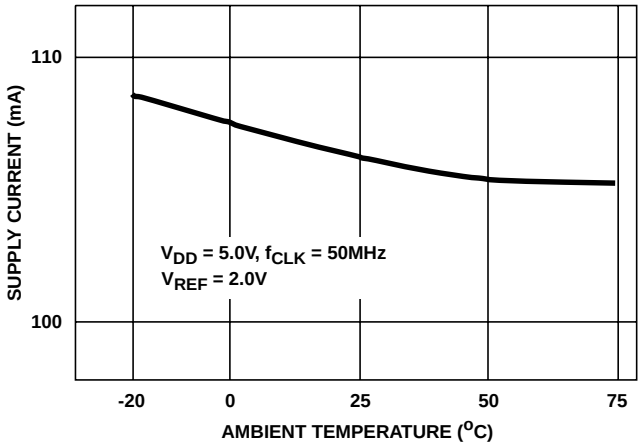


FIGURE 3. SUPPLY CURRENT vs AMBIENT TEMPERATURE

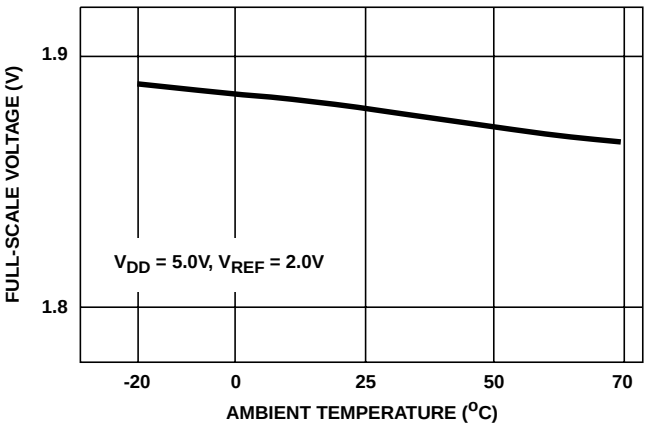


FIGURE 4. FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

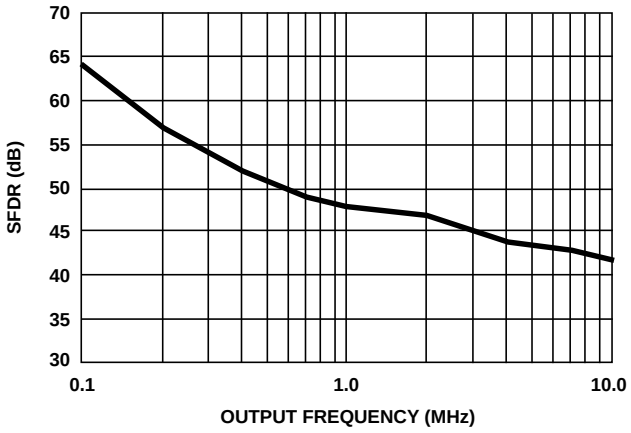


FIGURE 5. SFDR vs OUTPUT FREQUENCY

DAC INPUT/OUTPUT CODE TABLE (NOTE 1)

INPUT CODE										
MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	OUTPUT VOLTAGE
1	1	1	1	1	1	1	1	1	1	2.0V
				•						
				•						
				•						
1	0	0	0	0	0	0	0	0	0	1.0V
				•						
				•						
				•						
0	0	0	0	0	0	0	0	0	0	0V

NOTE:

1. V_{REF} = 2.0V, R_{SET} = 1.2K, R_{LOAD} = 75Ω.

Detailed Description

The HI3050 contains three matched, individual, 10 bit current output digital-to-analog converters. The DACs can convert at 50MHz and run on +5V for both the analog and digital supplies. The architecture is a current cell arrangement. 10-bit linearity is obtained without laser trimming due to an internal calibration.

Digital Inputs

The digital inputs to the HI3050 have TTL level thresholds. Due to the low input currents CMOS logic can be used as well. The digital inputs are latched on the rising edge of the clock.

To reduce switching noise from the digital data inputs, a series termination resistor is the best solution. Using a 50Ω to 130Ω resistor in series with the data lines, the edge rates are slowed. Slower edge rates reduce the amount of overshoot and undershoot that directly couples through the lead frame of the device. TTL drivers such as the 74ALS or 74F series or CMOS logic series drivers, ACT, AC, or FCT, are excellent for driving the TTL/CMOS inputs of the converter.

Clocks and Termination

The HI3050 clock rate can run to 50MHz, therefore, to minimize reflections and clock noise into the part, proper termination should be considered. In PCB layout clock traces should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance traces should be used with a characteristic line impedance.

To terminate the clock line, a shunt terminator to an AC ground is the most effective type at a 50MHz clock rate. Shunt termination is best used at the receiving end of the transmission line or as close to the HI3050 CLK pin as possible.

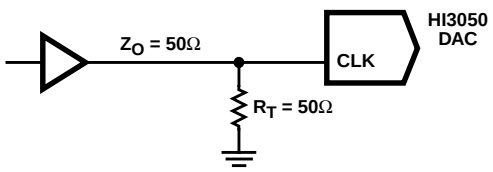


FIGURE 6. AC TERMINATION OF THE HI3050 CLOCK LINE

Rise and fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Power Supplies

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI3050 as possible on the analog (AV_{DD}) and digital (DV_{DD}) supplies. The analog and digital ground returns should be connected together at the device to ensure proper operation on power up.

Reference

The HI3050 DACs have their own references and can be set individually, see Figure 13. The three references can also share a common reference voltage, see Figure 12. A shared reference gives DAC to DAC matching of 1.5%, typically.

The HI3050 requires an external reference voltage to set the full scale output current. The external reference voltage is connected to the V_{REF} inputs (V_{REFR}, V_{REFG}, and VREFB). The Full Scale Adjust input (FS ADJUST R, FS ADJUST G, FS ADJUST B) should be connected to AGND through a 1.2kΩ resistor, R_{SET}. The reference outputs (V_{REF} OUT R, V_{REF} OUT G, V_{REF} OUT B) should be connected to the decoupling input (COMP R, COMP G, COMP B) and decoupled to AV_{DD} with a 0.1µF capacitor. This improves settling time by decoupling switching noise from the reference output of the HI3050.

The full scale output current is controlled by the voltage reference pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = (V_{REF}/R_{SET}) x 16, I_{OUT} is in mA (EQ.1)

Blanking Input

The BLANK input, when pulled high, will force the outputs of all three DACs to 0mA.

Chip Enable

The chip enable input, $\overline{CE}$, will shut down the HI3050 causing the outputs to go to 0mA. The analog and digital supply current will decrease to less than 1mA, reducing power for low power applications.

Outputs

The HI3050 DAC outputs are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The current output can be converted to a voltage by using a resistor load or I/V converting op amp. If only one output of a converter is being used, the unused output can be connected to ground or to a load equal to the used output. The output voltage when using a resistor load is:

$$V_{OUT} = I_{OUT} \times R_{OUT} \quad \text{(EQ. 2)}$$

The compliance range of the outputs is from 0V to +2.5V.

To convert the output current of the D/A converter to a voltage a load resistor followed by a buffer amplifier can be used as shown in Figure 5. The DAC needs a 75Ω termination resistor on the I_{OUT} pin to ensure proper settling.

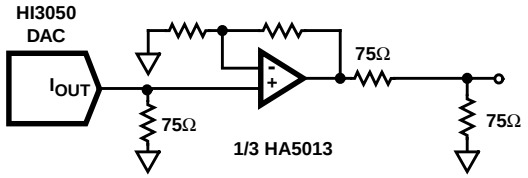


FIGURE 7. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Glitch

The output glitch of the HI3050 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. To minimize this, the Intersil HI3050 employs an internal register, just prior to the current sources, that is updated on the clock edge.

In measuring the output glitch of the HI3050, the output is terminated into a 75Ω load. The glitch is measured at the major carries throughout the DACs output range.

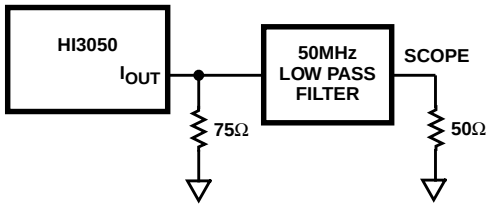
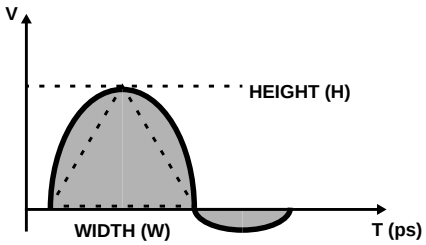


FIGURE 8. GLITCH TEST CIRCUIT

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 9 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt/seconds (pV/s).



GLITCH AREA = $^1/_2$ (H X W)

FIGURE 9. GLITCH ENERGY

Test Circuits

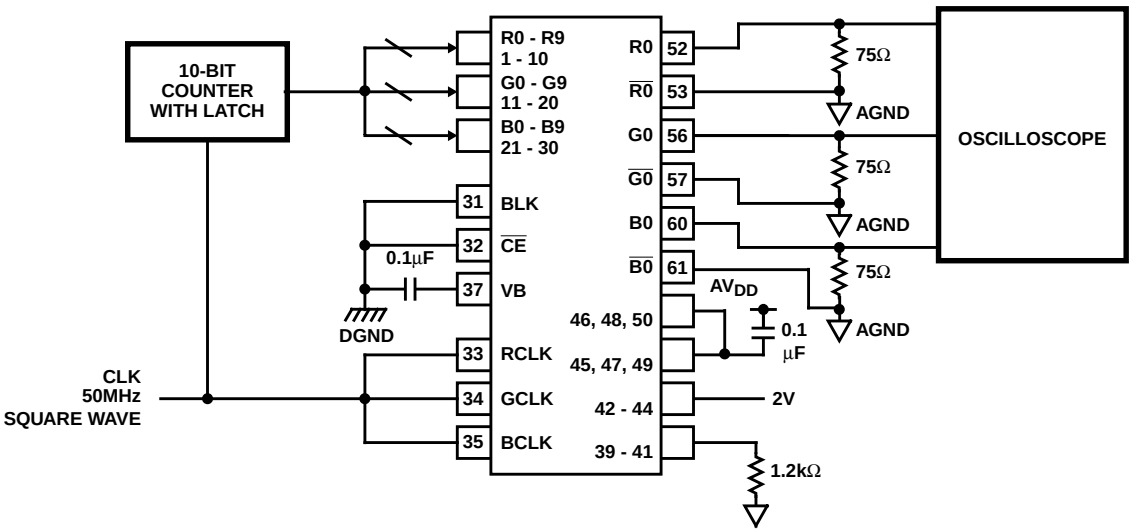


FIGURE 10. MAXIMUM CONVERSION SPEED TEST CIRCUIT

Test Circuits (Continued)

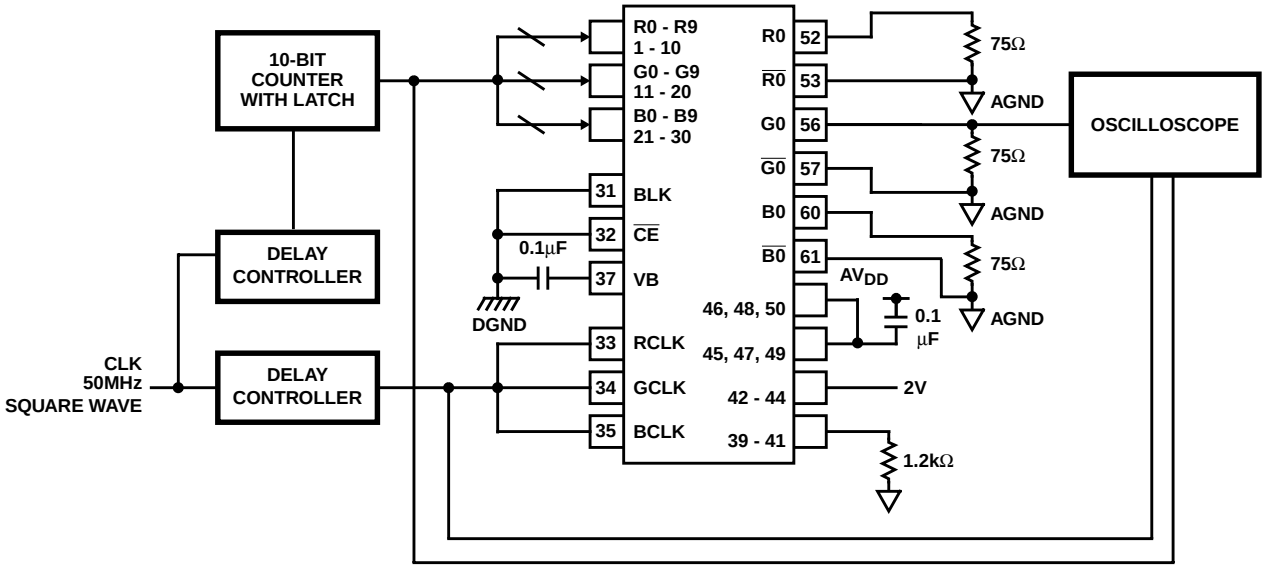


FIGURE 11. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

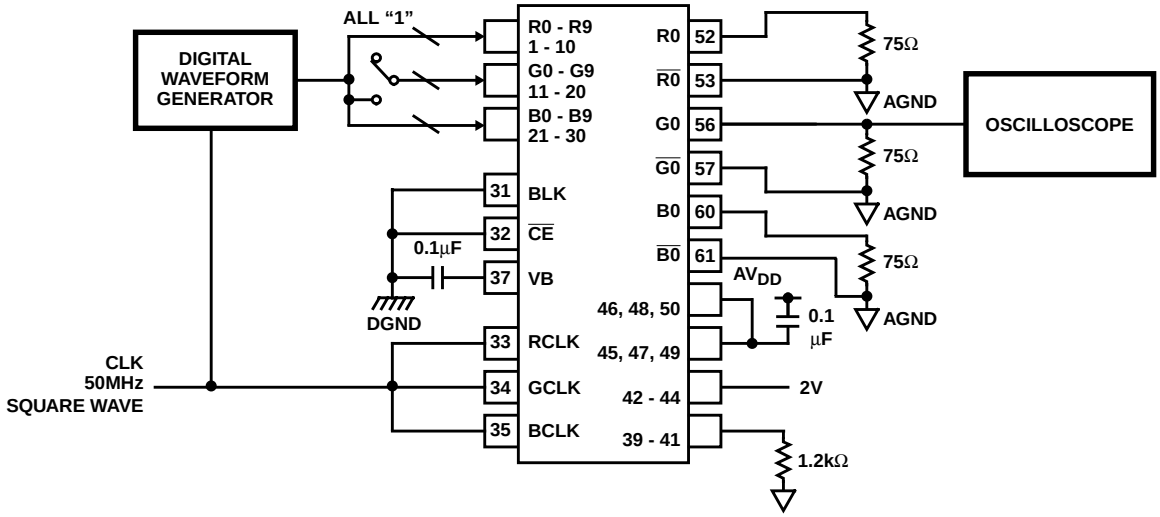


FIGURE 12. CROSSTALK TEST CIRCUIT

Applications Circuits

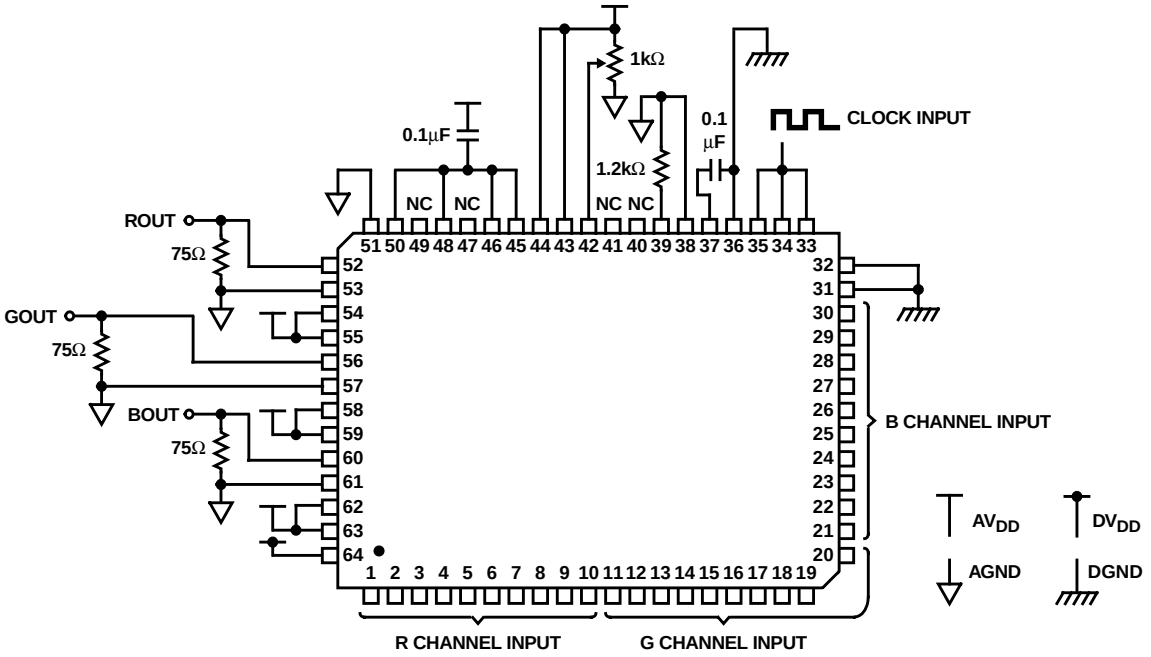


FIGURE 13. COMMON VOLTAGE REFERENCE

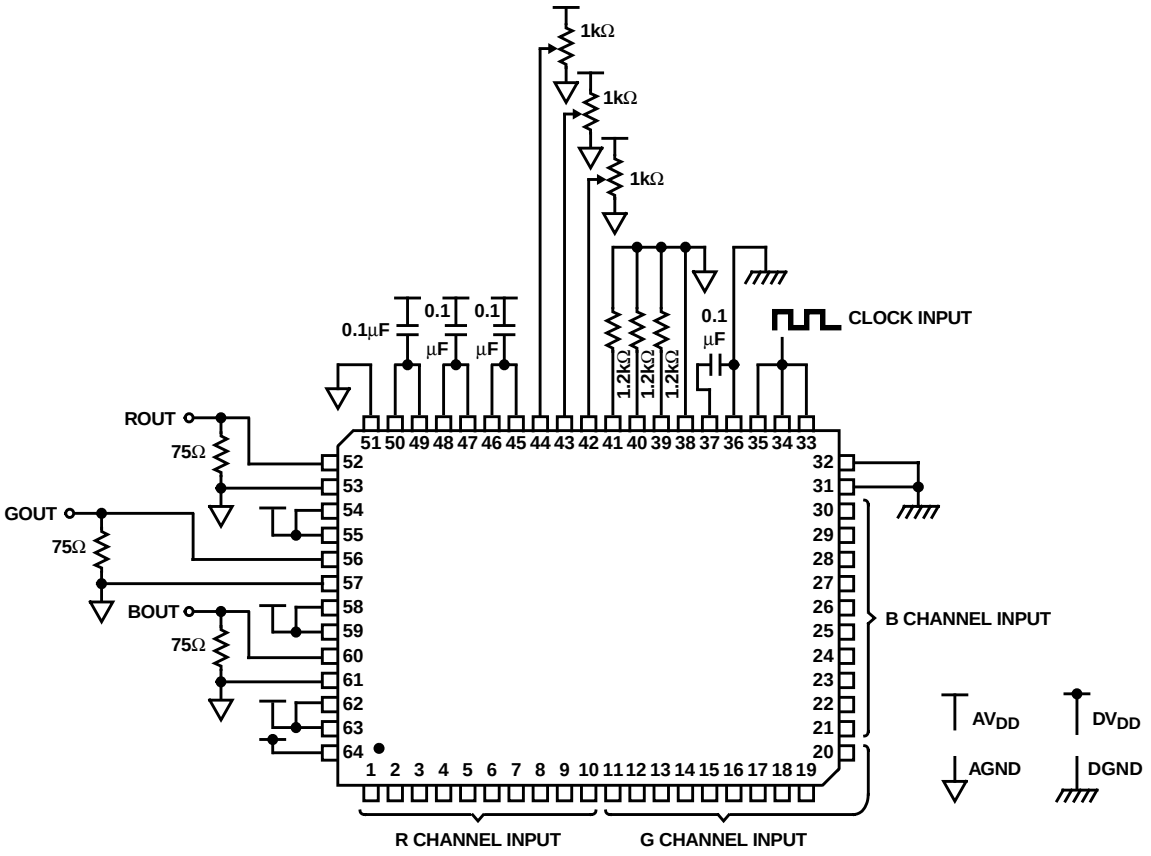


FIGURE 14. INDEPENDENT REFERENCES

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Crosstalk, is the undesirable signal coupling from one channel to another.

Feedthrough, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $^1/_2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Energy, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, DG, is the peak difference in chrominance amplitude (in percent) at two different DC levels.

Differential Phase, DP, is the peak difference in chrominance phase (in degrees) at two different DC levels.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD, is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is:

$$IMD = \frac{20\ \text{Log (RMS of Sum and Difference Distortion Products)}}{(\text{RMS Amplitude of the Fundamental})}$$