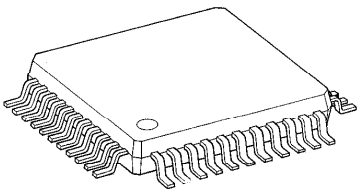
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9287AF

2 CHANNEL 1BIT AD / DA CONVERTER FOR AUDIO

TC9287AF is 2'nd order Σ-Δ modulation 1bit AD / DA converter for Digital Audio. This IC built-in 2 channel AD / DA converter, and digital and analog filter, so construct hi-performance and low cost AD / DA converter system.



QFP44-P-1010-0.80

Weight : 0.5g (Typ.)

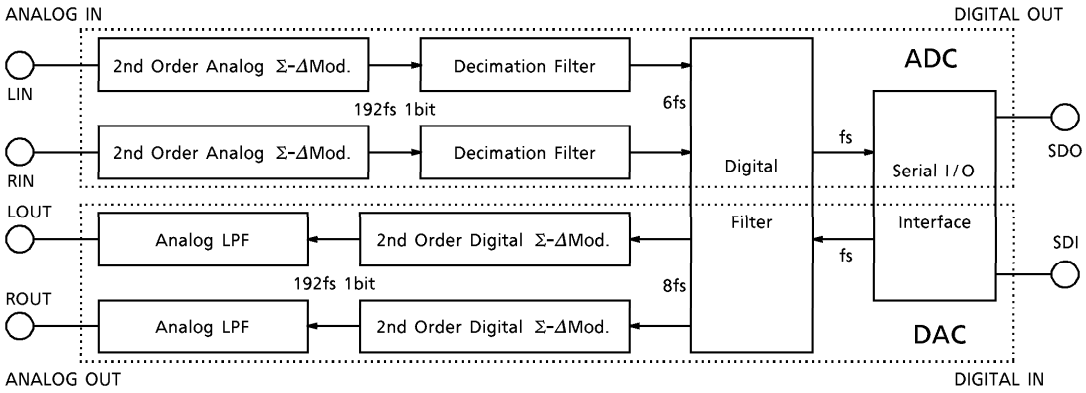
FEATURES

- Built in input and output digital / analog filter circuit, so external filter is CR filter.
- Operating voltage is 5.0V.
- Power dissipation is 250mW (V_{DD} = 5V) [At ADOFF mode, 190mW (V_{DD} = 5V)]
- Package is QFP44-P-1010-0.80.

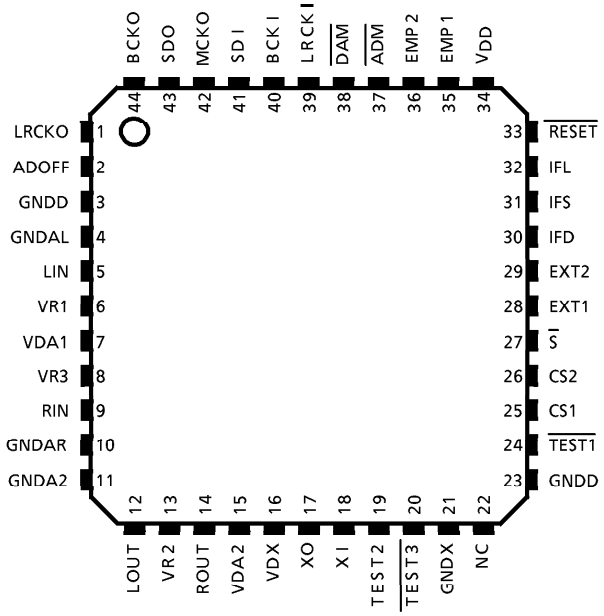
AD / DA AC characteristics is as follows.

	S / N (A-Weight)	THD + N
AD converter	92dB (Typ.)	– 82dB (Typ.)
DA converter	95dB (Typ.)	– 87dB (Typ.)

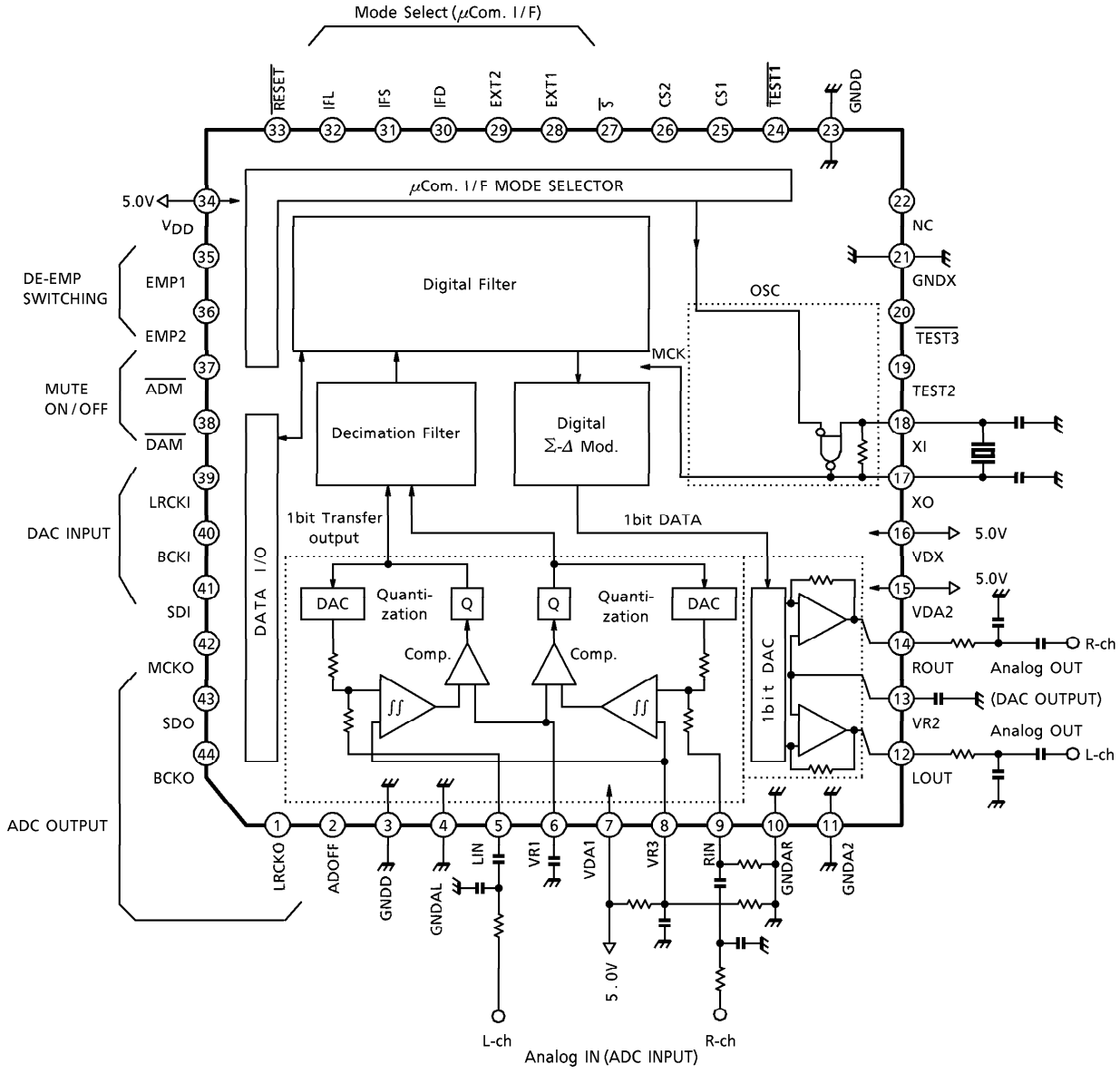
SYSTEM BLOCK



PIN CONNECTION



BLOCK DIAGRAM



Pin DESCRIPTION

NO.	TERMINAL	I / O	FUNCTION	REMARK
1	LRCKO	O	Channel clock (LRCK) output pin.	
2	ADOFF	I	A / D converter off setting pin. At "H" level, A / D modulation and decimation filter block operation are OFF.	Pull-down
3	GNDD	—	Digital GND pin.	0V
4	GNDAL	—	Analog GND pin for A / D converter Left channel.	0V
5	LIN	I	A / D converter Left channel analog signal input pin.	2.5V ± α
6	VR1	—	Reference voltage pin for A / D converter comparator.	2.5V
7	VDA1	—	Power supply pin for A / D converter.	5.0V
8	VR3	—	Reference voltage pin for A / D converter integrator.	2.5V
9	RIN	I	A / D converter Right channel analog signal input pin.	2.5V ± α
10	GNDAR	—	Analog GND pin for A / D converter Right channel.	0V
11	GNDA2	—	Analog GND pin for D / A converter.	0V
12	LOUT	O	D / A converter Left channel analog signal output pin.	2.5V – α
13	VR2	O	Reference voltage pin for D / A converter.	2.5V
14	ROUT	O	D / A converter Right channel analog signal output pin.	2.5V – α
15	VDA2	—	Power supply pin for D / A converter.	5.0V
16	VDX	—	Power supply pin for Oscillator.	5.0V
17	XO	O	Crystal oscillator connection pin.	
18	XI	I	Crystal oscillator connection pin.	
19	TEST2	O	Test pin 2. Usually use at open state.	
20	$\overline{\text{TEST3}}$	I	Test pin 3. Usually use at "L" level.	
21	GNDX	—	GND pin for Oscillator.	0V
22	NC	—	Non-connecting. NC pin is use in the open state.	
23	GNDD	—	Digital GND pin.	0V
24	$\overline{\text{TEST1}}$	I	Test pin 1. Usually use at "H" level.	Pull-up
25	CS1	I	Master mode setting pin 1.	Pull-up
26	CS2	I	Master mode setting pin 2.	Pull-up
27	$\overline{\text{S}}$	I	Serial mode pin. (fixed "L" level)	Pull-up
28	EXT1	O	External output pin 1.	Serial mode
29	EXT2	O	External output pin 2.	Serial mode
30	IFD	I	Micro controller interface data input pin.	Pull-up Serial mode
31	IFS	I	Micro controller interface shift clock input pin.	Pull-up Serial mode
32	IFL	I	Micro controller interface latch pulse input pin.	Pull-up Serial mode

NO.	Pin	I / O	FUNCTION	REMARK
33	$\overline{\text{RESET}}$	I	Reset pin.	Pull-up
34	V_{DD}	—	Digital voltage supply pin.	5.0V
35	EM1	I	De-emphasis Coefficient select pin 1.	Pull-down
36	EM2	I	De-emphasis Coefficient select pin 2.	Pull-down
37	$\overline{\text{ADM}}$	I	AD converter output mute pin. At "L" level, mute "ON".	Pull-up
38	$\overline{\text{DAM}}$	I	AD converter output mute pin. At "L" level, mute "ON".	Pull-up
39	LRCKI	I	External channel clock (LRCK) input pin.	
40	BCKI	I	External bit clock (BCK) input pin.	
41	SDI	I	Digital data input pin. (DA converter serial data input)	
42	MCKO	O	384fs clock output pin. (system clock)	
43	SDO	O	Digital data output pin. (AD converter serial data output)	
44	BCKO	O	Bit clock (BCK) output pin.	

FUNCTION / APPLICATION

1. Analog pin

1) LIN : L-ch ADC input (pin 5)

- Input is inverting amplifier, input impedance is 25kΩ (Typ.).
- Ri (= 1kΩ) must not change, because this value effect total gain.
- Full-scale analog input is $1V_{rms}$ (V_{DD} = 5V, Ri = 1kΩ), if input level is more, digital data becomes over scale. In this case, digital data is clip.
- ADC full-scale input level is sifted by V_{DD} level.

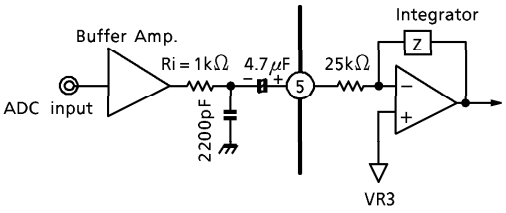


Fig.1

2) VR1 : Reference voltage input for ADC comparator (pin 6)

- Impedance is 5kΩ (Typ.).
- This IC generates 1 / 2 VDA internally by resister dividing, so please put on only external decoupling condenser.

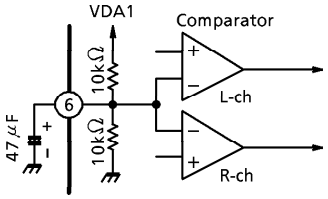


Fig.2

3) VR3 : Reference voltage for ADC integrator (pin 8)

- Impedance is 6.2kΩ (Typ.).
- This IC generates 1 / 2 VDA internally by resister dividing. Further it is necessary to connect 3.0kΩ between VR3 pin and VDA1, 3.3kΩ between VR3 pin ad GNDAR, and then decoupling condenser externally, because of offset adjustment

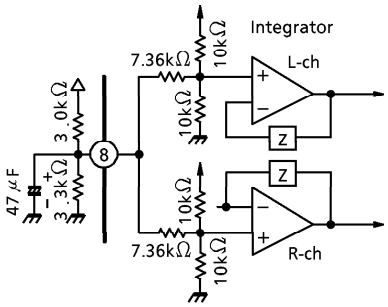


Fig.3

4) PIN : R-ch ADC input (pin 9)

- Input is inverting amplifier, input impedance is 25kΩ (Typ.).
- Ri (= 1kΩ) must not change, because this value effect total gain.
- Full-scale analog input is $1V_{rms}$ (V_{DD} = 5V, Ri = 1kΩ), if input level is more, digital data becomes over scale. In this case, digital data is clip.
- ADC full-scale input level is sifted by V_{DD} level.
- Because of offset compensation, it is necessary to connect 2.2MΩ between RIN and GNDAR pin.

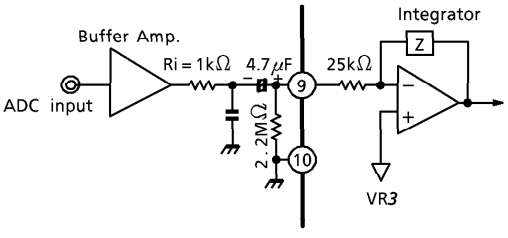


Fig.4

5) LOUT / ROUT : DAC output (pin 12 / 14)

- R does not only construct low pass filter, but also protect output signal form capacitor load and short.
- Full-scale output level is $1.25V_{rms}$ ($V_{DD} = 5V$).
- DAC full-scale output level is sifted by V_{DD} level.

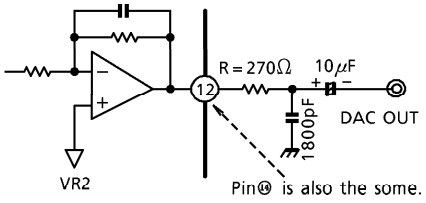


Fig.5

6) VR2 : Reference voltage for DAC output amplifier (pin 13)

- Impedance is 7.5kΩ (Typ.).
- This IC generates 1 / 2 VDA internally by resister dividing, so please put on only external decoupling condenser.
- Nothing decoupling condenser is OK, but AC output characteristics becomes worse. (S / N, PSRR, CT, etc.)

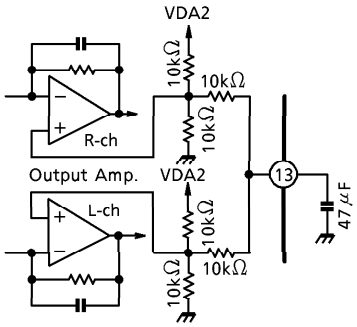


Fig.6

7) Crystal oscillator circuit input / output XI (pin 18), XO (pin 19)

- C1, C2 is 33pF typical, but all oscillator is not so. Please ask Oscillator maker.
- XI pin is very high sensitive In case of input external noise from XI, the clock jitter in creases sharply. Consequently, the characteristic of A / D, D / A conversion is worsened greatly.

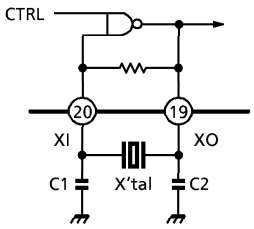


Fig.7

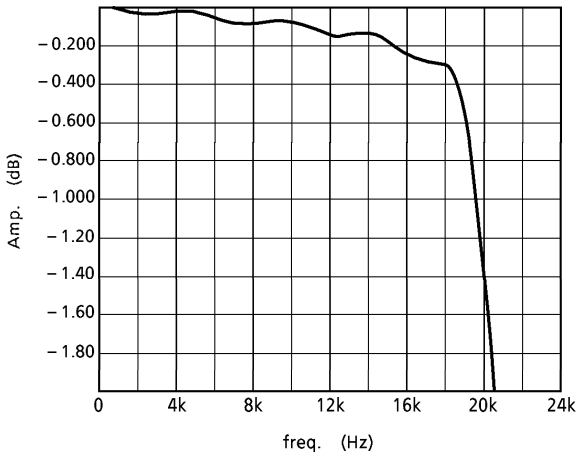


Fig.13 (a)
A / D Converter Digital + Analog Filter
Characristic for fs = 44.1kHz (1)

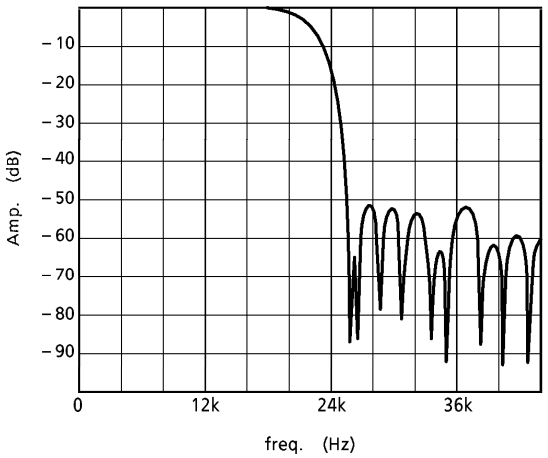


Fig.13 (b)
A / D Converter Digital + Analog Filter
Characristic for fs = 44.1kHz (2)

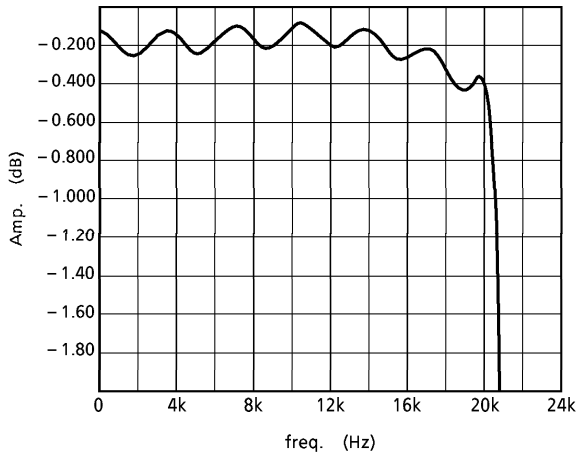


Fig.13 (a)
D / A Converter Digital + Analog Filter
Characristic for fs = 44.1kHz (1)

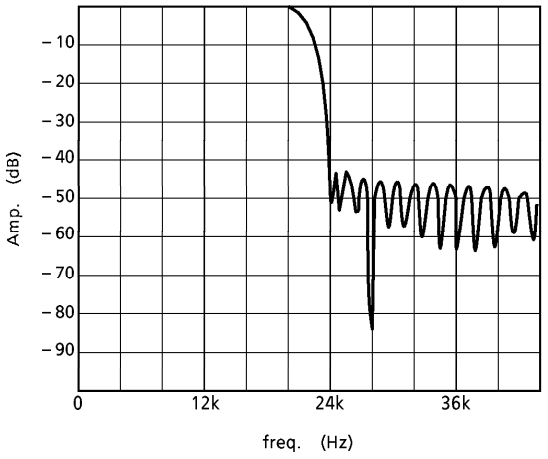
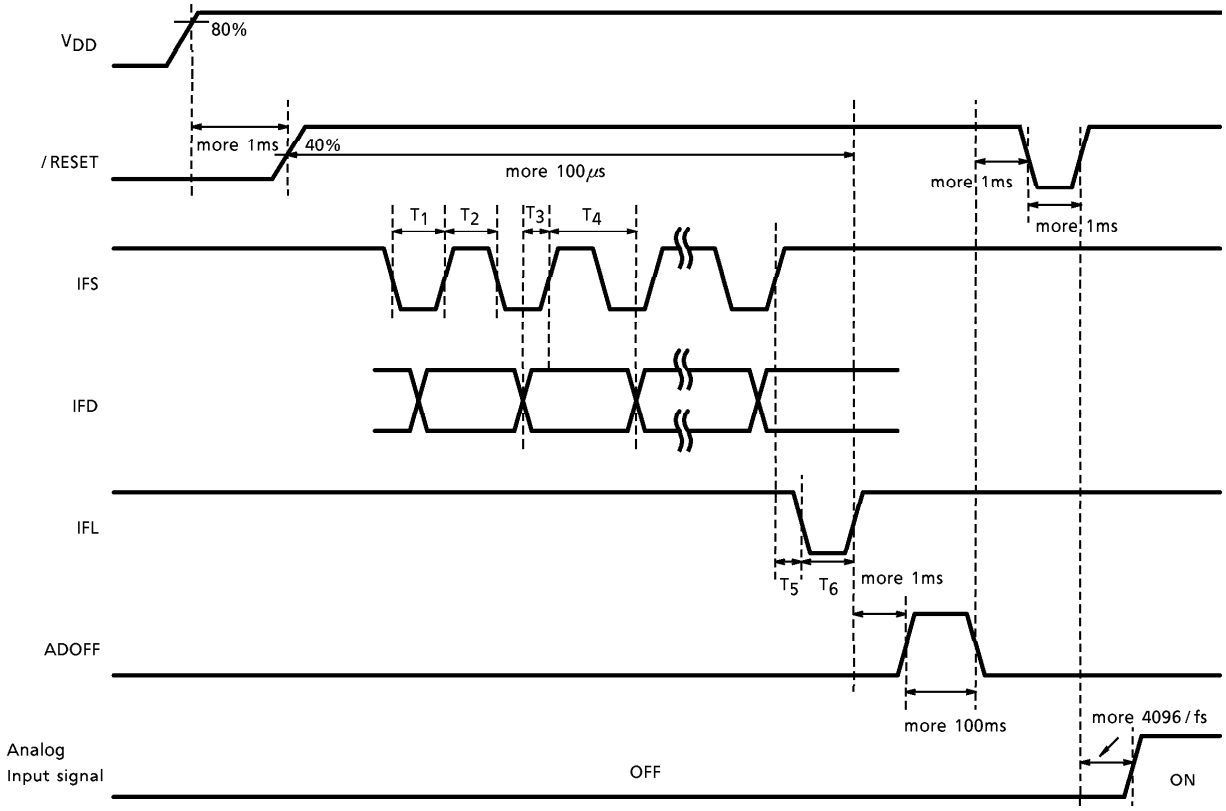


Fig.13 (b)
D / A Converter Digital Filter Characristic
for fs = 44.1kHz (2)

2. Timing



T1, T2, T6	:	Clock pulse width	>1μs
T3	:	Set time	>1μs
T4	:	Hold time	>1μs
T5	:	Hold time	>1μs

Fig.8 Timing Chart

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~6.0	V
	V_{DX}		
	V_{DA1}		
	V_{DA2}		
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.6	V
Power Dissipation	P_D	250	mW
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, $V_{DD} = V_{DX} = V_{DA1} = V_{DA2} = 5V$)
DC Characteristics

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Supply Voltage		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.25	V
		V_{DX}						
		V_{DA1}						
		V_{DA2}						
Power Dissipation		I_{DD}	—	XI = 16.9344MHz ADOFF = "L"	—	50	90	mA
Power Dissipation (at ADOFF = OFF)				XI = 16.9344MHz MHz ADOFF = "H"	—	35	63	
Input Voltage	"H" レベル	V_{IH}	—		3.5	—	—	V
	"L" レベル	V_{IL}			—	—	1.5	
Output Current	"H" レベル	I_{OH}	—	42pin V_{OH} = 0.4V	−9.4	—	−3.6	mA
				1, 28, 29, 43, 44pin V_{OH} = 0.4V	−5.0	—	−2.1	
	"L" レベル	I_{OL}	—	42pin V_{OL} = 4.6V	8.0	—	22.0	
				1, 28, 29, 43, 44 pin V_{OL} = 4.6V	3.5	—	14.0	
Input Current		I_{IN}	—		−10	—	10	μA
Pull Up / Dowin Rester		$R_{U/D}$	—		60	—	150	kΩ

AC Characteristics
A / D converter

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Maximum Input Voltage	V_{IM}	1	Input voltage = Output level of A / D converter is full scall	0.9	1.0	1.1	V_{rms}
Input Impedance	Z_{IN}	1		—	25.0	—	kΩ
S / N Ratio	S/N_A	1	A-Weight	88	92	—	dB
Table Harmonic Distortion + Noise	THD_A	1		—	−82	−77	dB
Cross-tolk	CT_A	1	A-Weight	—	−90	−85	dB
Output Offset	OFST	1	Input AC is short circuit	−100	0	+100	LSB

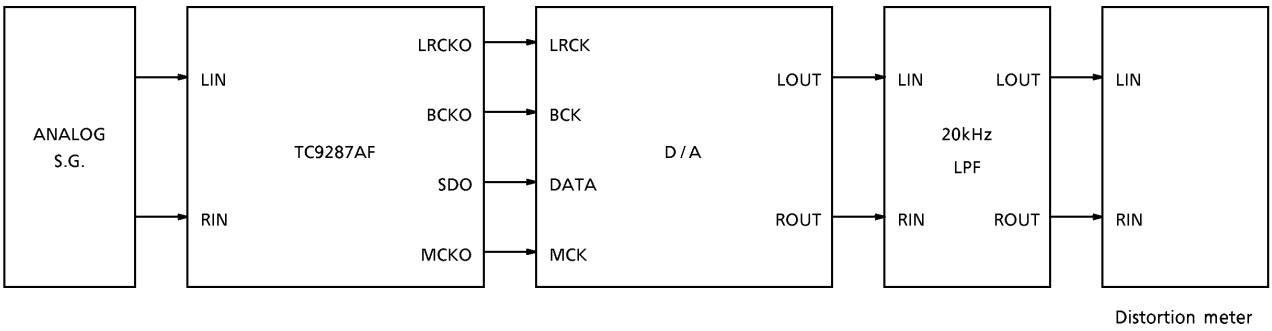
D / A converter

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Maximum output Voltage	V_{OM}	2	Output voltage at full scall level input	—	1.25	—	V_{rms}
S / N Ratio	S/N_D	2	At A-Weight	88	95	—	dB
Table Harmonic Distortion + Noise	THD_{AD}	2		—	−87	−80	dB
Dynamic Range	DR_D	2	At A-Weight	85	92	—	dB
Cross-tolk	CT_D	2	At A-Weight	—	−90	−85	dB

Common item

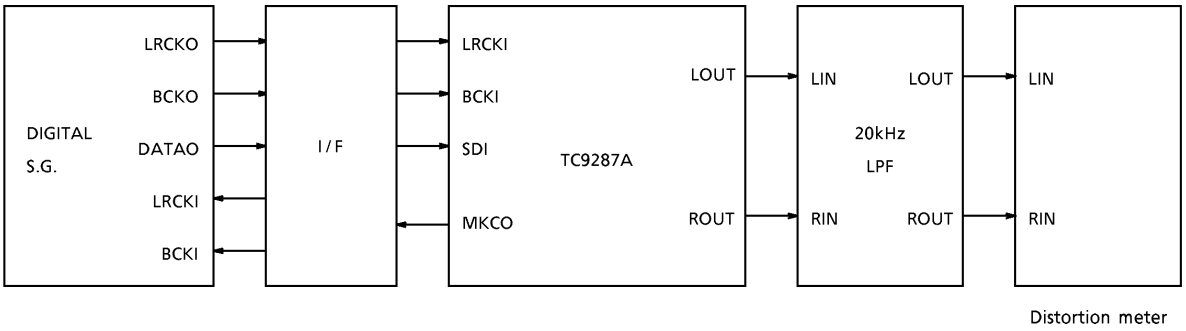
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Frequency		f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 4.5V$	12	16.9344	18.5	MHz
Input Frequency		f_{LRCKI}	—		30	44.1	50	MHz
		f_{BCKI}			1	1.41	6.2	
Rise Time of Input Signal		t_{ri}	—	LRCKI, BCKI pin (10~90%)	—	—	15	ns
Fall Time of Input Signal		t_{fi}	—		—	—	15	
Delay Time of Input Signal		t_{di}	—	The falling edge of BCKI→ LRCKI, SDI	—	—	40	
MCUI I / F	Rise Time of Input Signal	t_{riM}	—	IFL, IFS pin (10~90%)	—	—	15	
	Fall Time of Input Signal	t_{fiM}	—		—	—	15	
	Delay Time of Input Signal	t_{diM}	—	The falling edge of IFS→ IFL, IFD	—	—	40	
Rise Time of Output Signal		t_{ro}	—	LRCKO, BCKO pin (10~90%)	—	—	15	
Fall Time of Output Signal		t_{fo}	—		—	—	15	
Delay Time of Output Signal		t_{do}	—	The falling edge of BCKO→ LRCKO, SDO	—	—	40	

TEST CIRCUIT 1 : A / D converter evaluation system



ANALOG S.G. : SHIBASOKU, AM51A
20kHz LPF : SHIBASOKU, INTERNAL FILTER OF AM51A
Distortion meter : SHIBASOKU, AM51A

TEST CIRCUIT 2 : D / A converter evaluation system

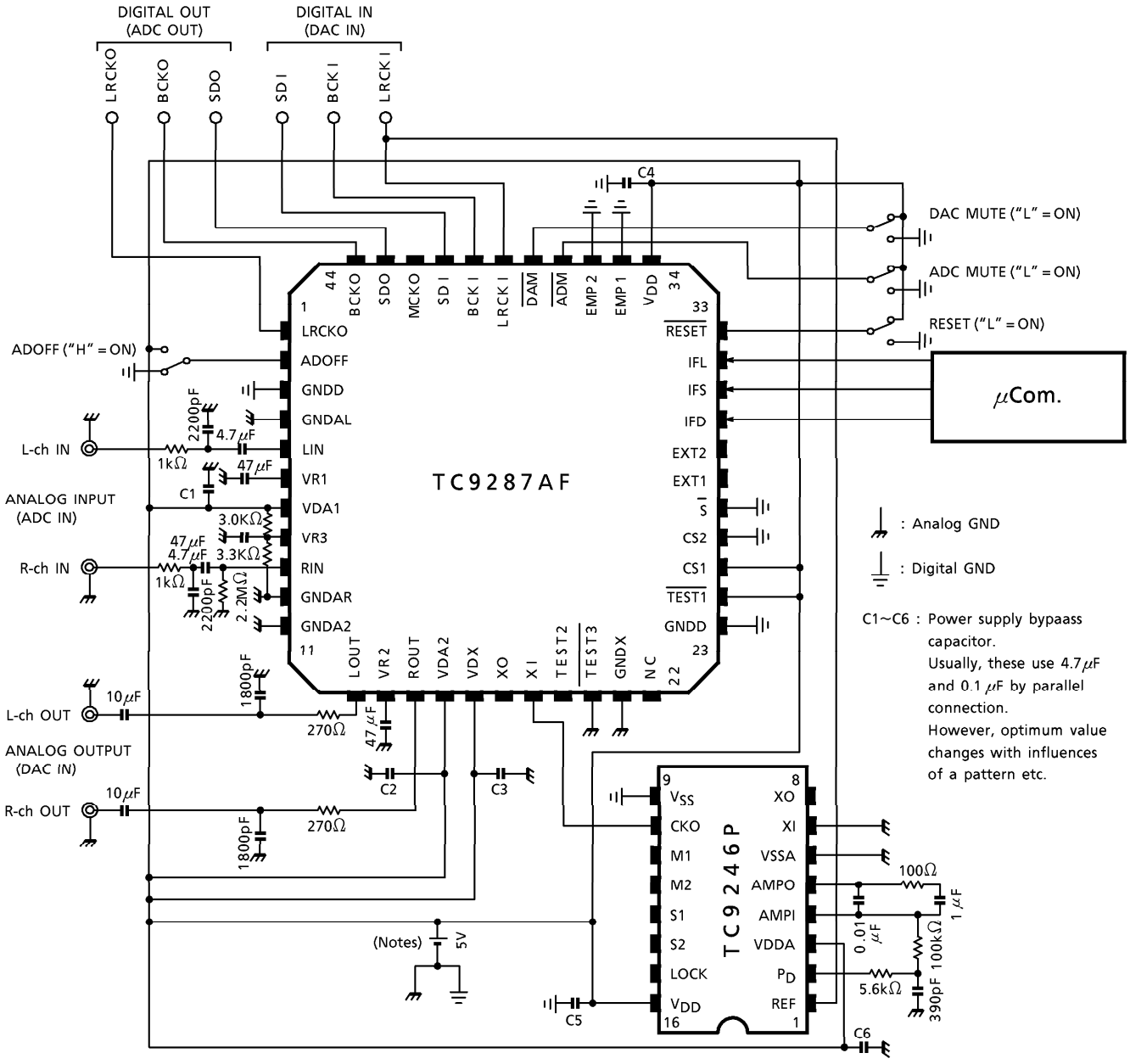


DIGITAL S.G. : ANRITSU, MG-22A
20kHz LPF : SHIBASOKU, INTERNAL FILTER OF 725C
Distortion meter : SHIBASOKU, 725C

APPLICATION CIRCUIT 1

(use external PLL IC : TC9246F / P)

* Slave and Serial mode

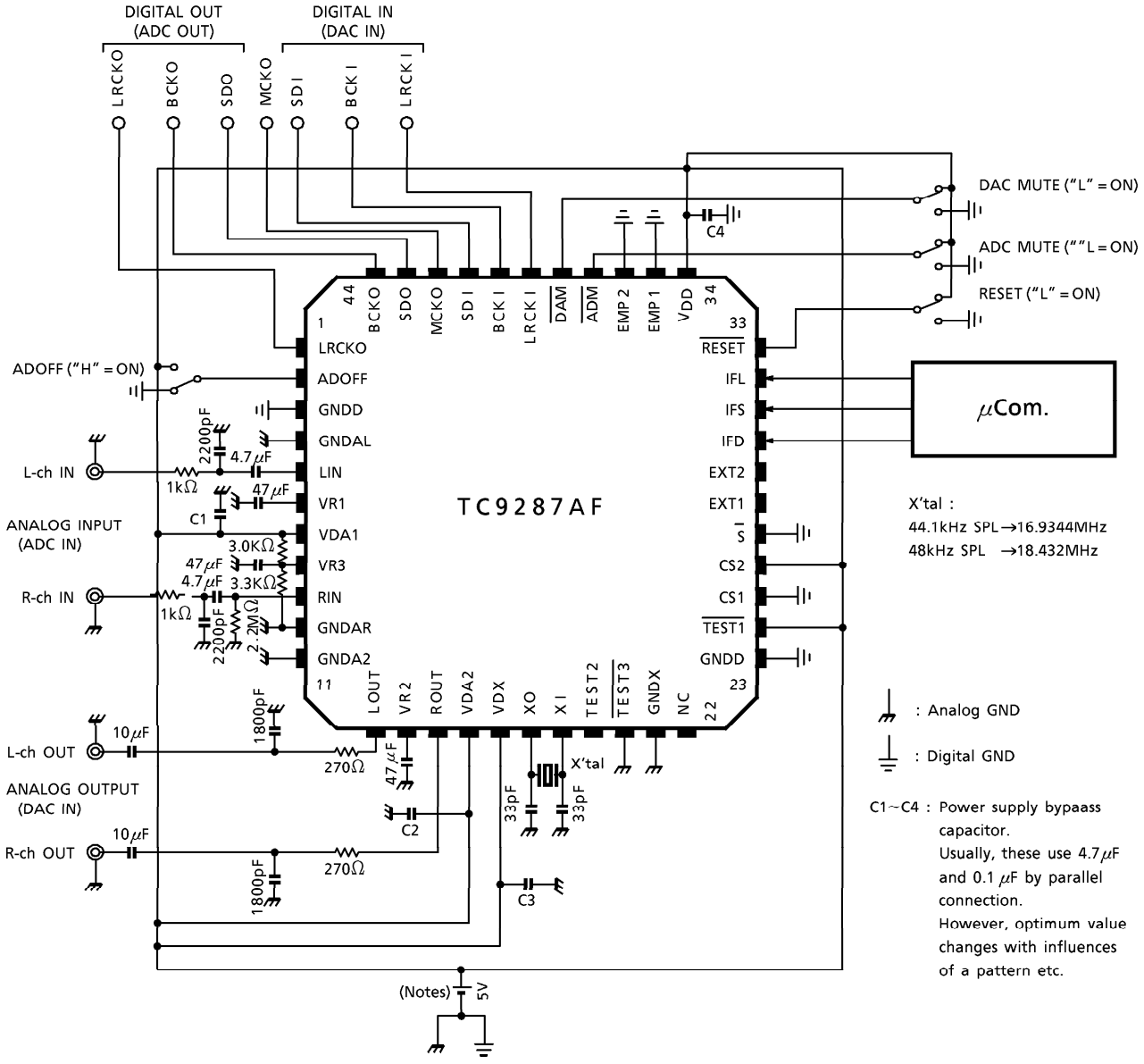


(Notes) : Wiring of a power supply divides a digital system and an analog system completely, and it is necessary to consider that TC9287AF is not influenced of common impedance.

- After turning on the power supply, and in case that the power supply voltage rang is exceeded temporarily, please set RESET pin to "L" at once, and then set ADOFF pin to "H". (ADOFF period is required 100ms or more.)

APPLICATION CIRCUIT 2

* Master and Serial mode



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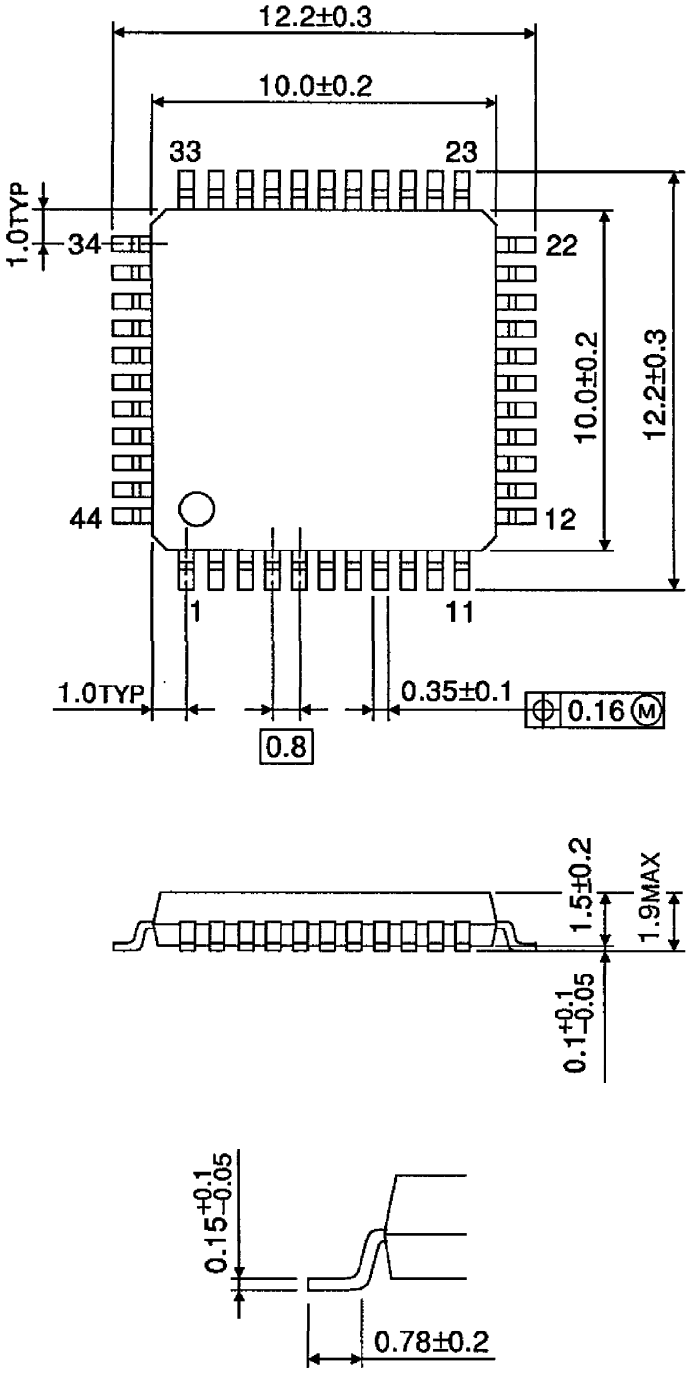
- After turning on the power supply, and in case that the power supply voltage rang is exceeded temporarily, please set RESET pin to "L" at once, and then set ADOFF pin to "H". (ADOFF period is required 100ms or more.)

PACKAGE DIMENSIONS

QFP44-P-1010-0.80 Unit : mm



Weight : 0.5g (Typ.)