



N- and P-Channel 40-V (D-S) MOSFET

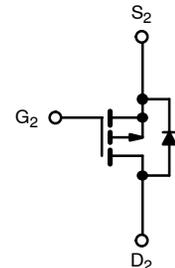
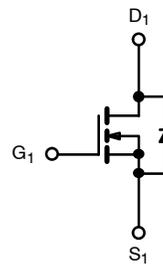
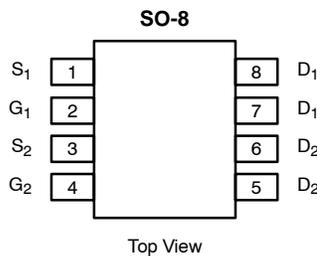
PRODUCT SUMMARY				
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
N-Channel	40	0.040 @ V _{GS} = 10 V	5.2	8
		0.045 @ V _{GS} = 4.5 V	4.9	
P-Channel	-40	0.054 @ V _{GS} = -10 V	-4.5	9
		0.072 @ V _{GS} = -4.5 V	-3.9	

FEATURES

- TrenchFET® Power MOSFET
- 100% R_g Tested
- UIS Tested

APPLICATIONS

- CCFL Inverter



Ordering Information: Si4565DY—E3
Si4565DY-T1—E3 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 secs	Steady State	10 secs	Steady State		
Drain-Source Voltage	V _{DS}	40		-40		V	
Gate-Source Voltage	V _{GS}	±12		±16			
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	5.2	3.9	-4.5	-3.3	A	
	T _A = 70 °C	4.2	3.1	-3.6	-2.7		
Pulsed Drain Current	I _{DM}	30					
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	0.9	-1.7	-0.9		
Avalanche Current	I _{AS}	13		16			
Single Pulse Avalanche Energy	E _{AS}	8.5		13		mJ	
Maximum Power Dissipation ^a	T _A = 25 °C	2.0	1.1	2	1.1	W	
	T _A = 70 °C	1.3	0.7	1.3	0.7		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150				°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ	Max	Typ	Max		
Maximum Junction-to-Ambient ^a	t ≤ 10 sec	52	62.5	50	62.5	°C/W	
	Steady State	90	110	85	110		
Maximum Junction-to-Foot (Drain)	Steady State	32	40	30	40		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6		1.6	V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.8		-2.2		
V _{DS} Temperature Coefficient	ΔV _{DS/TJ}	I _D = 250 μA	N-Ch		40		mV/°C	
			P-Ch		-40			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)/TJ}		N-Ch		-3.8			
			P-Ch		3.4			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V	N-Ch			±100	nA	
		V _{DS} = 0 V, V _{GS} = ±16 V	P-Ch			±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = -40 V, V _{GS} = 0 V	P-Ch			-1		
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10		
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			-10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	20			A	
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-20				
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5.2 A	N-Ch		0.033	0.040	Ω	
		V _{GS} = -10 V, I _D = -4.5 A	P-Ch		0.045	0.054		
		V _{GS} = 4.5 V, I _D = 4.9 A	N-Ch		0.037	0.045		
		V _{GS} = -4.5 V, I _D = -3.9 A	P-Ch		0.059	0.072		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.2 A	N-Ch		18		S	
		V _{DS} = -15 V, I _D = -4.5 A	P-Ch		13			
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.75	1.2	V	
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch		-0.79	-1.2		
Dynamic^b								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		700		pF	
Output Capacitance	C _{oss}		P-Channel V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		76		
Reverse Transfer Capacitance	C _{rss}			P-Ch		120		
Total Gate Charge	Q _g	N-Channel V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 5.2 A	N-Ch		8	12	nC	
			P-Ch		9	14		
Gate-Source Charge	Q _{gs}		P-Channel V _{DS} = -20 V, V _{GS} = -4.5 V, I _D = -4.5 A	N-Ch		1.5		
				P-Ch		2		
Gate-Drain Charge	Q _{gd}		N-Ch		2.4			
			P-Ch		3.6			
Gate Resistance	R _g		N-Ch	0.9	1.9	2.9	Ω	
			P-Ch	5	11.5	18		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω	N-Ch		7	11	ns	
Rise Time	t _r		P-Ch		8	13		
			N-Ch		11	17		
Turn-Off Delay Time	t _{d(off)}		P-Ch		12	18		
			N-Ch		27	40		
Fall Time	t _f		P-Ch		74	110		
			N-Ch		8	13		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		25		40
		I _F = -1.7 A, di/dt = 100 A/μs	P-Ch		27	45		
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		17	26	nC	
		I _F = -1.7 A, di/dt = 100 A/μs	P-Ch		17	26		

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

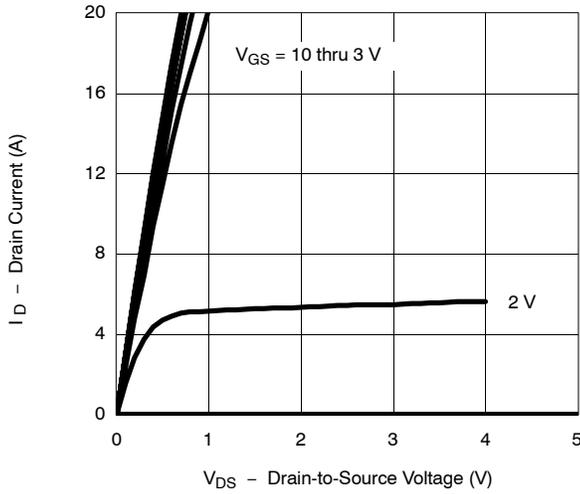
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



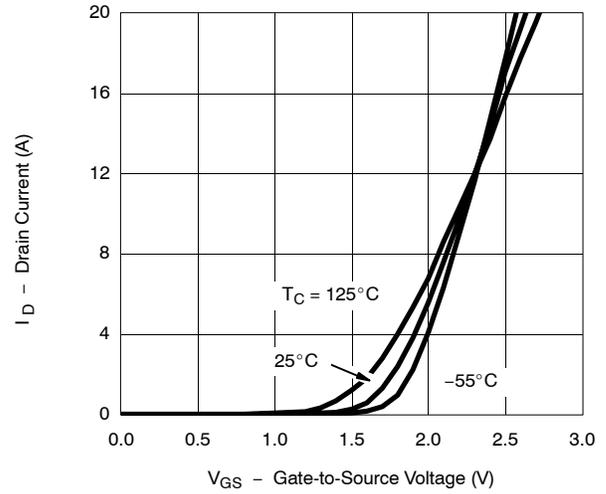
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL

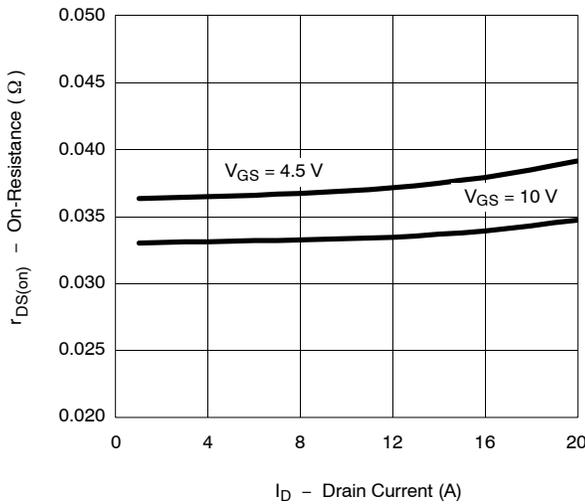
Output Characteristics



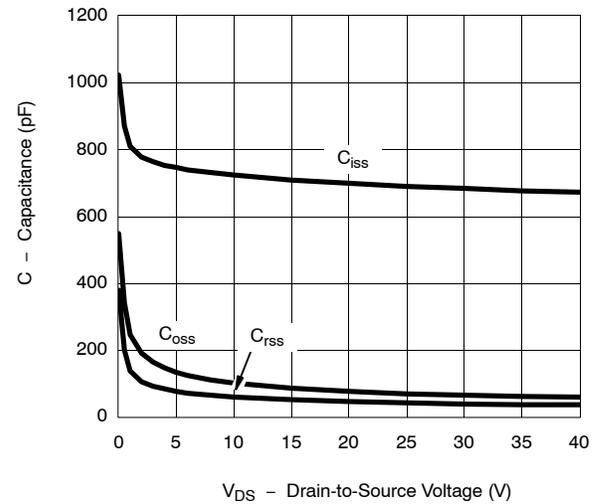
Transfer Characteristics



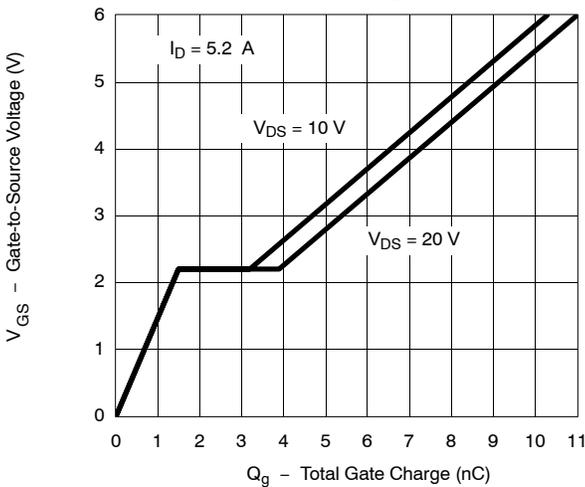
On-Resistance vs. Drain Current



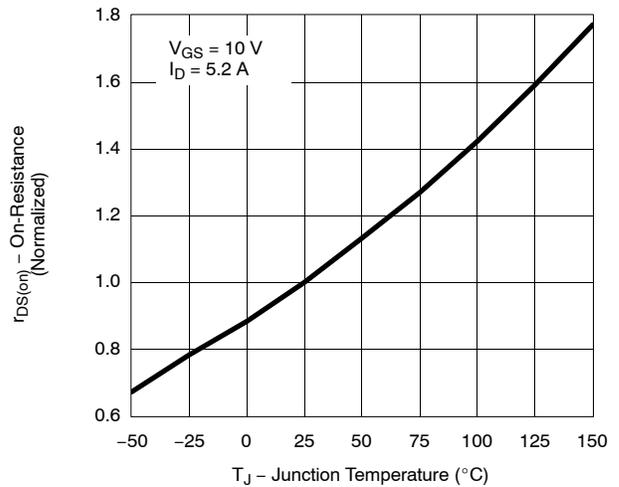
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

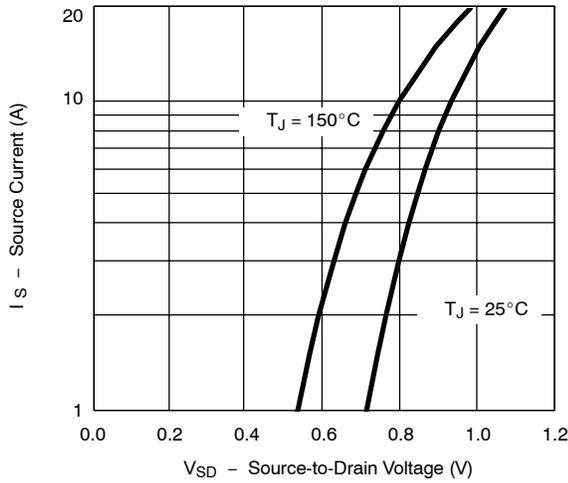




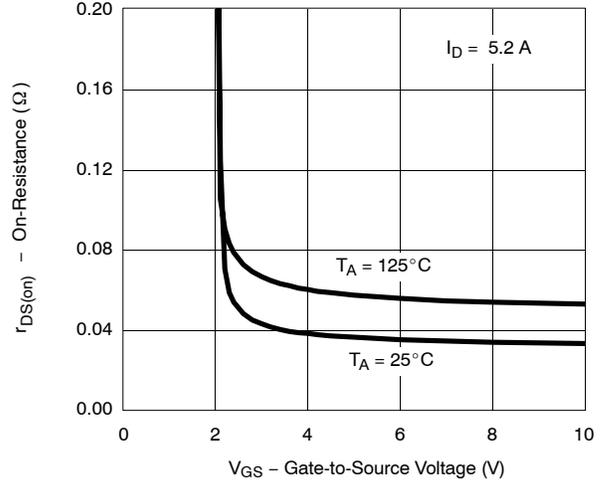
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

N-CHANNEL

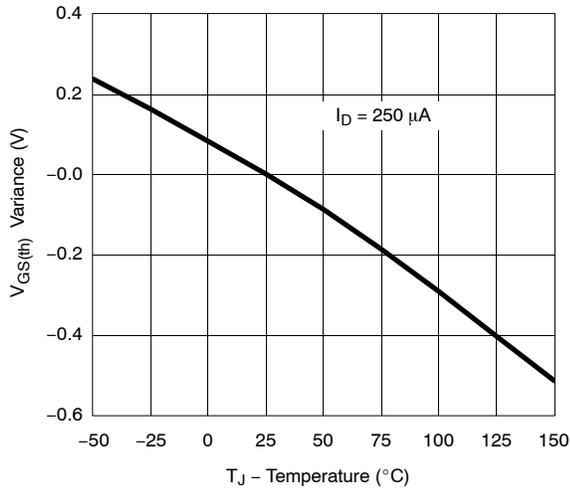
Source-Drain Diode Forward Voltage



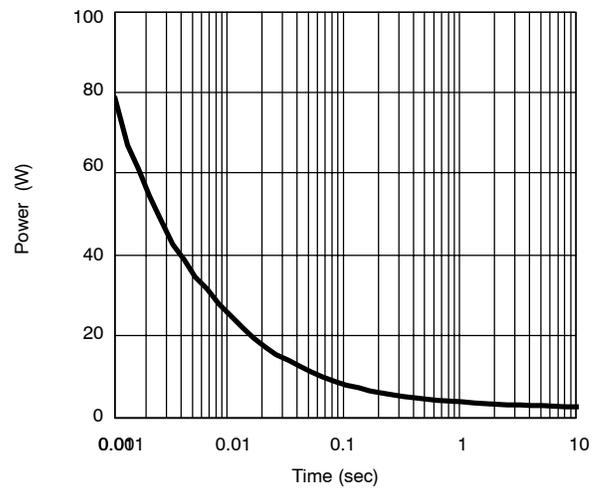
On-Resistance vs. Gate-to-Source Voltage



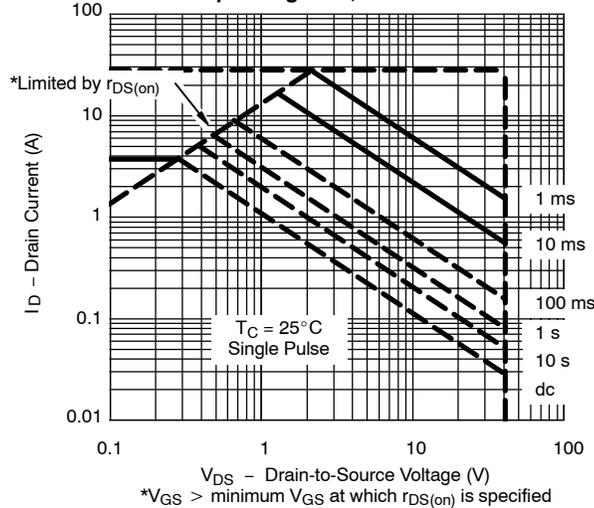
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



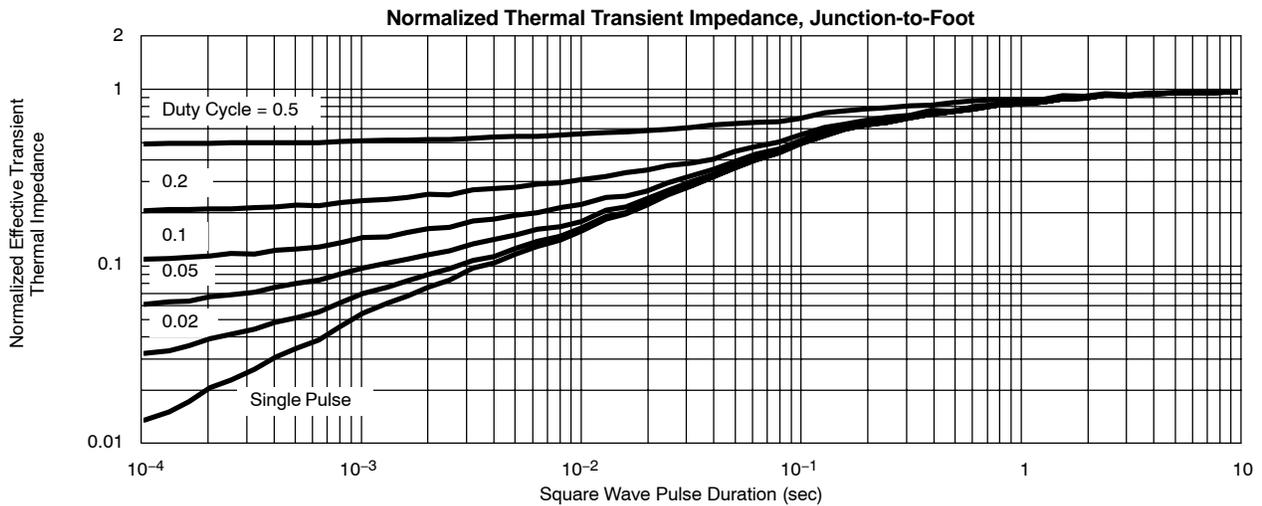
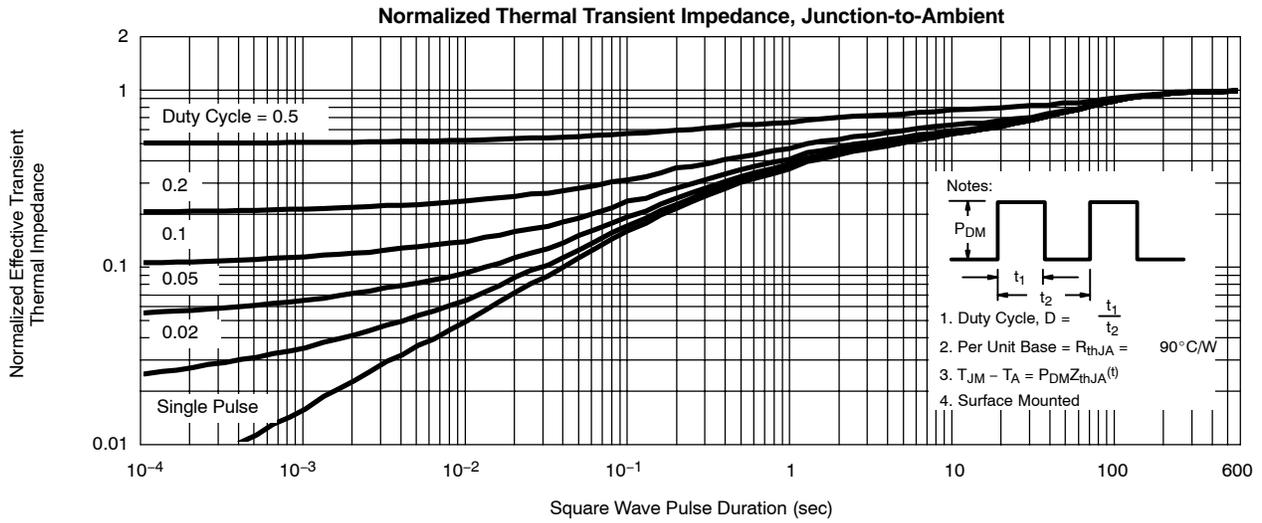
Safe Operating Area, Junction-to-Foot





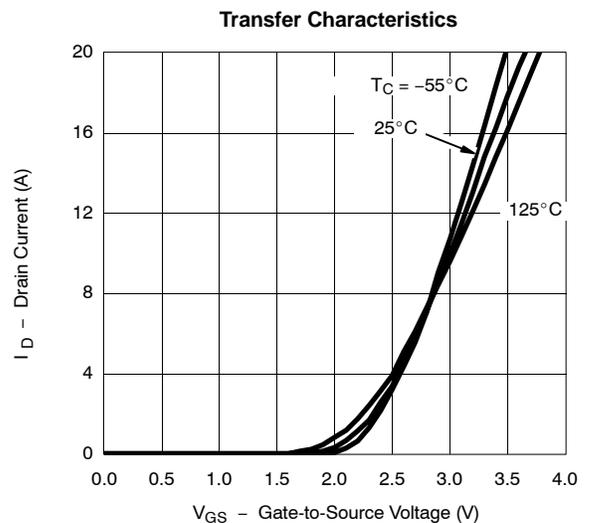
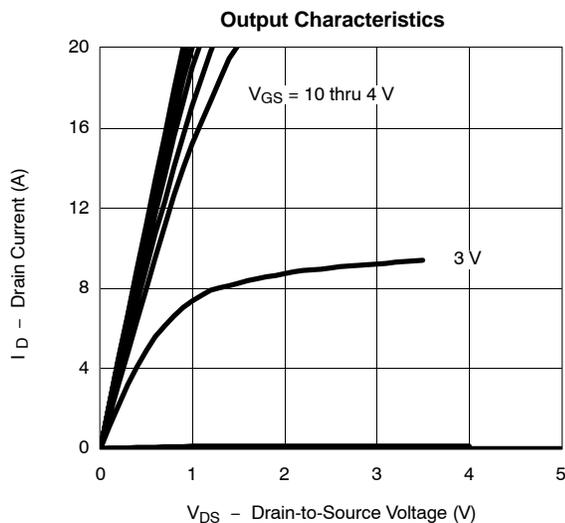
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL

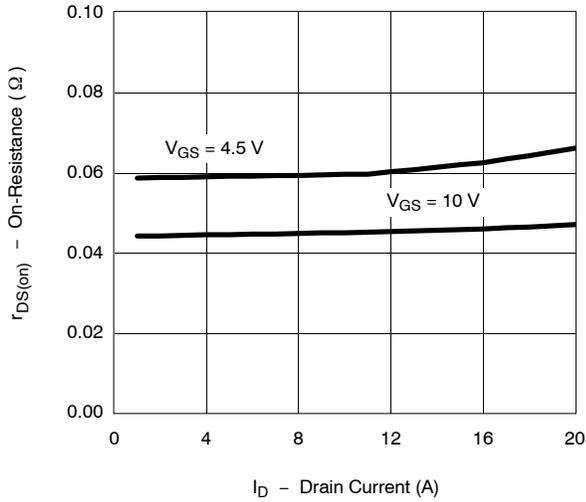




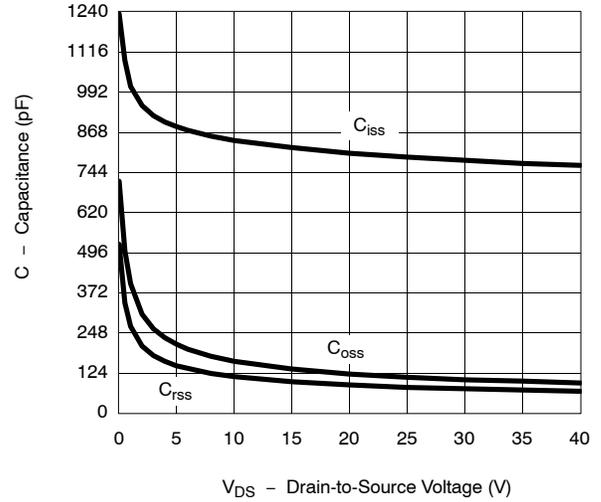
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P-CHANNEL

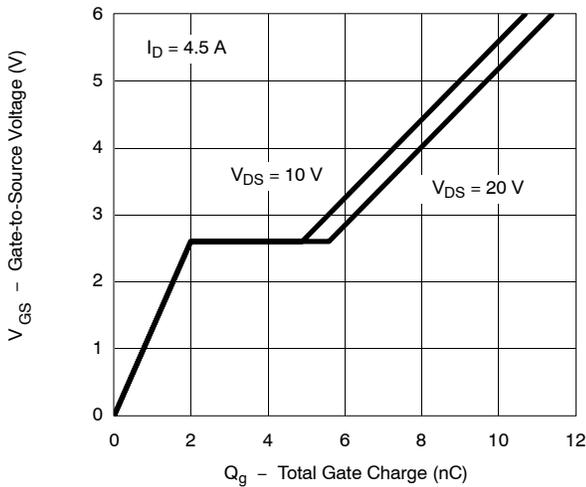
On-Resistance vs. Drain Current



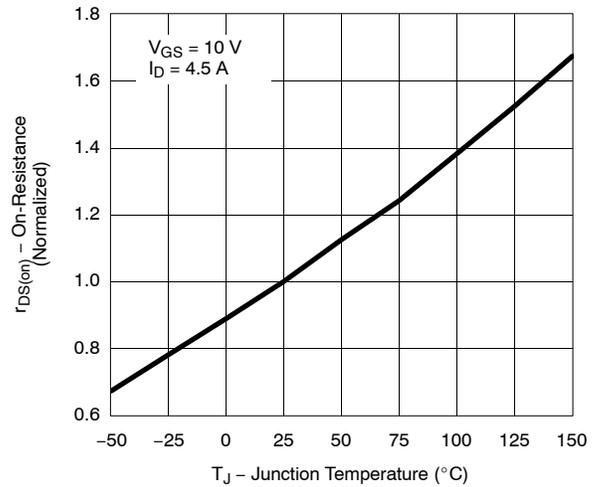
Capacitance



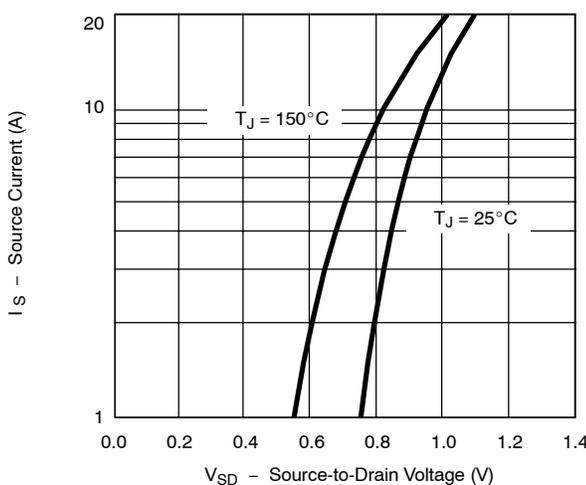
Gate Charge



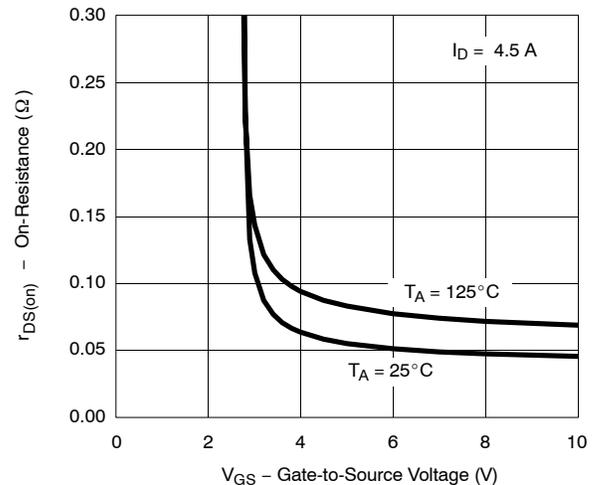
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



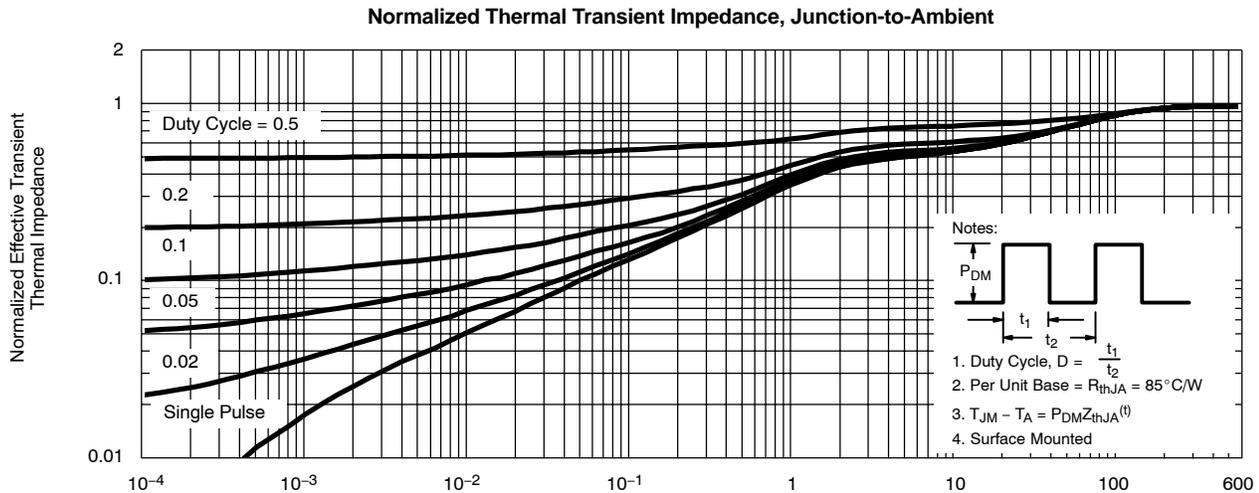
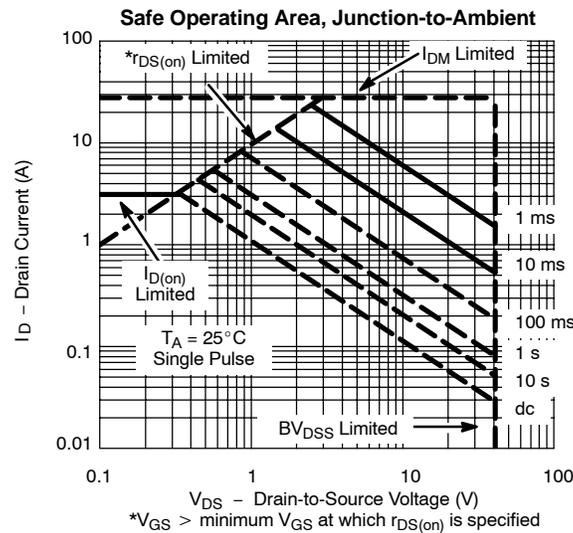
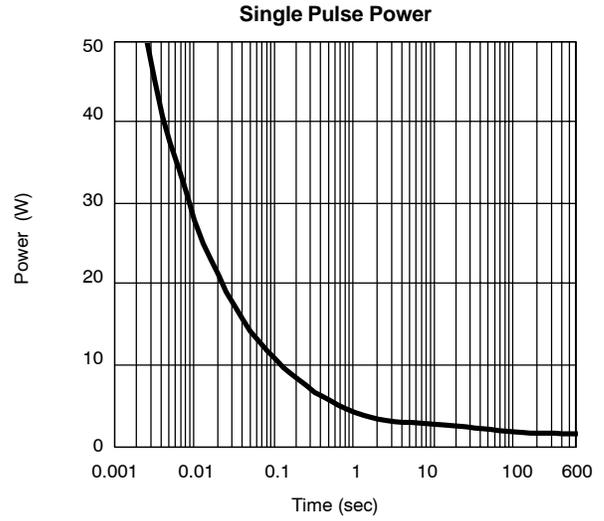
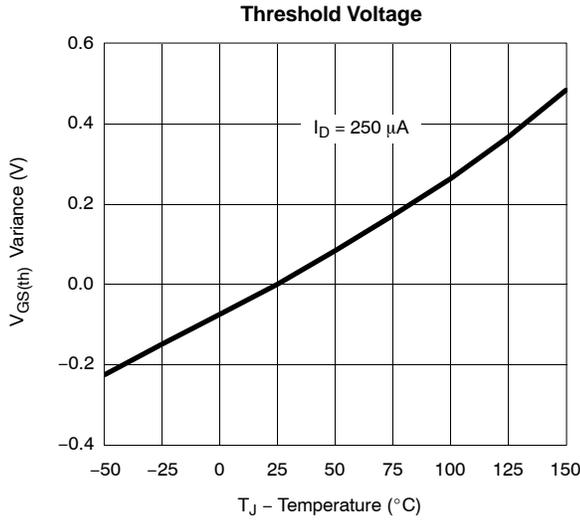
On-Resistance vs. Gate-to-Source Voltage





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

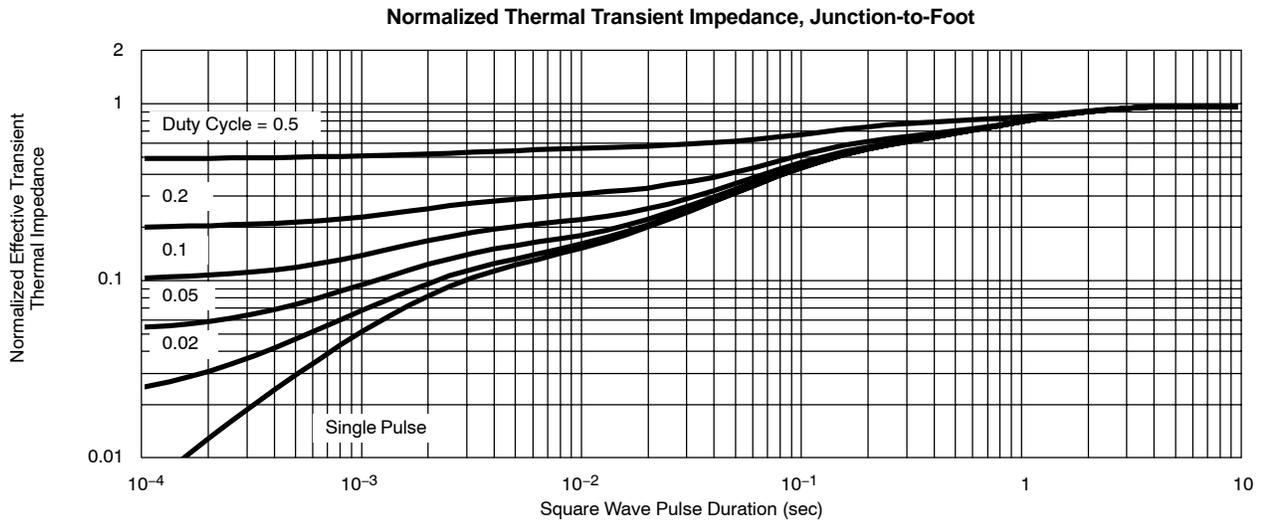
P-CHANNEL





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL



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