



# HCF4515B

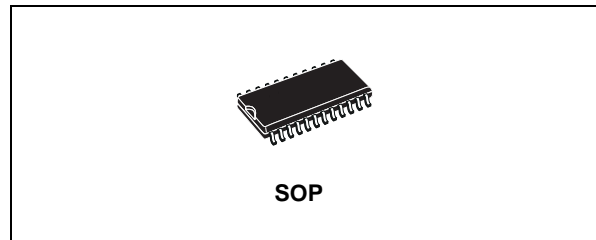
## OUTPUT "LOW" ON SELECT 4-BIT LATCH/4-TO-16 LINE DECODER

- QUIESCENT CURRENT SPECIF. UP TO 20V
- STROBED INPUT LATCH
- INHIBIT CONTROL
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

HCF4515B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in SOP package.

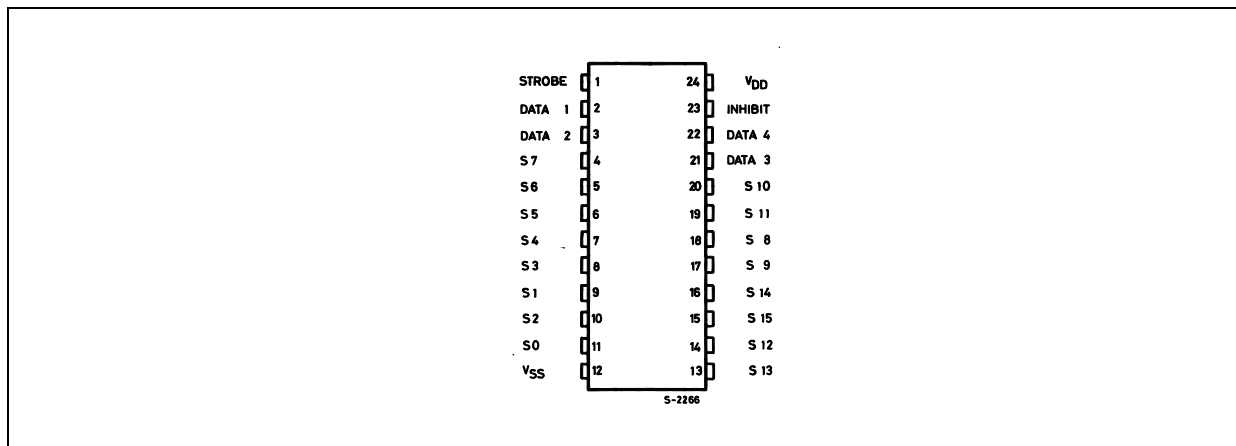
HCF4515B consists of a 4-bit strobed latch and a 4 to 16 line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 1 regardless of the state of the data or strobe inputs. The decode truth table indicates all combinations of data inputs and appropriate selected outputs.



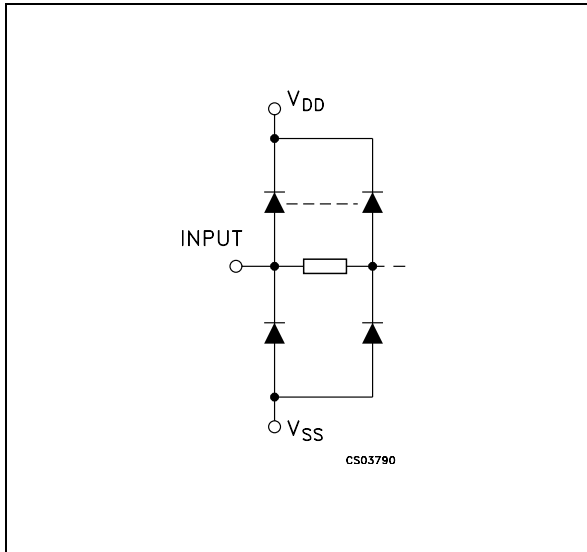
### ORDER CODES

PACKAGE	TUBE	T & R
SOP	HCF4515BM1	HCF4515M013TR

### PIN CONNECTION



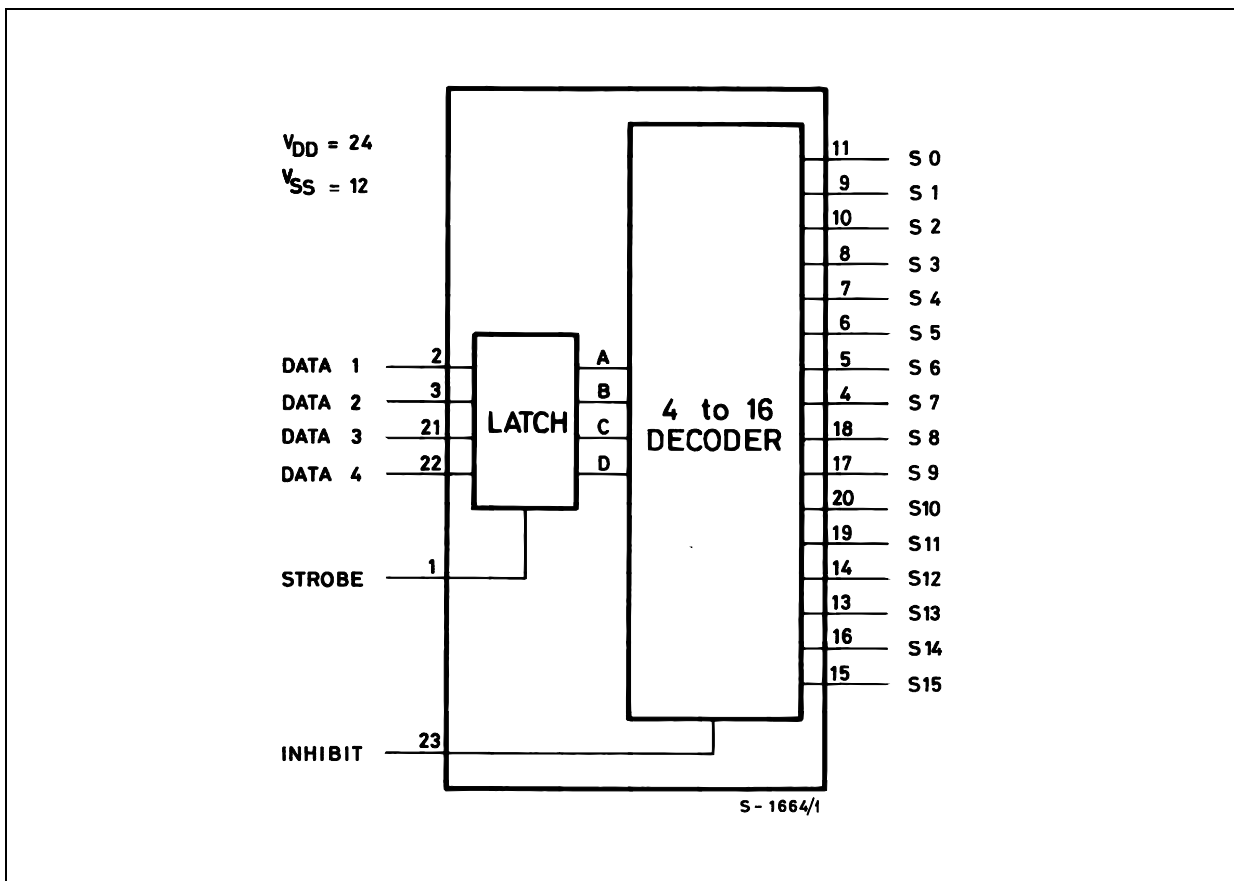
IINPUT EQUIVALENT CIRCUIT



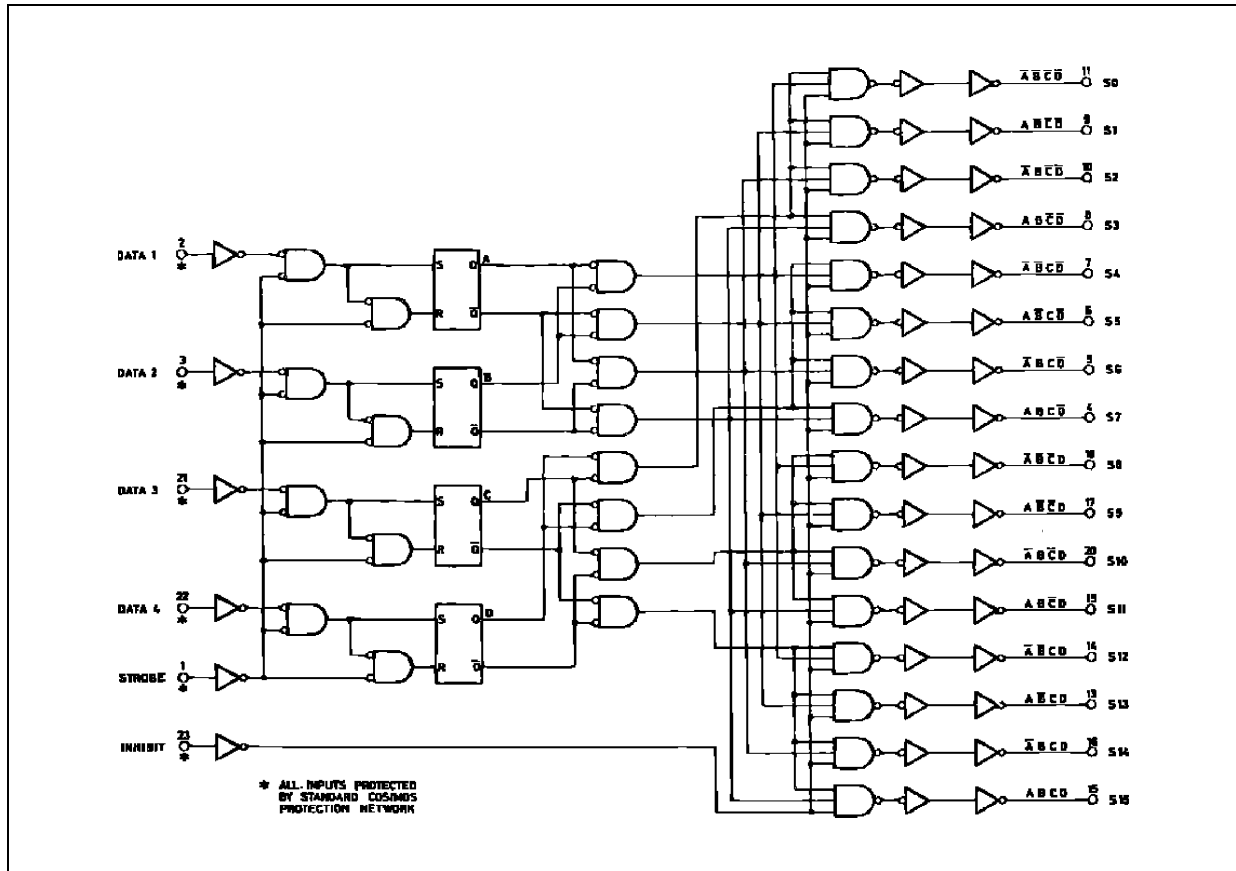
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2, 3, 21, 22	DATA 1 to 4	Address Inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	S0 to S15	Multiplexer Outputs (Active HIGH)
23	INHIBIT	Enable Input
12	$V_{SS}$	Negative Supply Voltage
24	$V_{DD}$	Positive Supply Voltage

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUTS					STROBE	SELECT OUTPUT
INHIBIT	A	B	C	D		
L	L	L	L	L	STROBE = "H" Refer to truth table	S0
L	H	L	L	L		S1
L	L	H	L	L	STROBE = "L" Data at the negative going transition of strobe shall be provided on the each output while strobe is held low.	S2
L	H	H	L	L		S3
L	L	L	H	L		S4
L	H	L	H	L		S5
L	L	H	H	L		S6
L	H	H	H	L		S7
L	L	L	L	H		S8
L	H	L	L	H		S9
L	L	H	L	H		S10
L	H	H	L	H		S11
L	L	L	H	H		S12
L	H	L	H	H		S13
L	L	H	H	H		S14
L	H	H	H	H		S15
H	X	X	X	X		ALL OUTPUTS "L"

X : Don't Care



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.04	5		150		150	$\mu$ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

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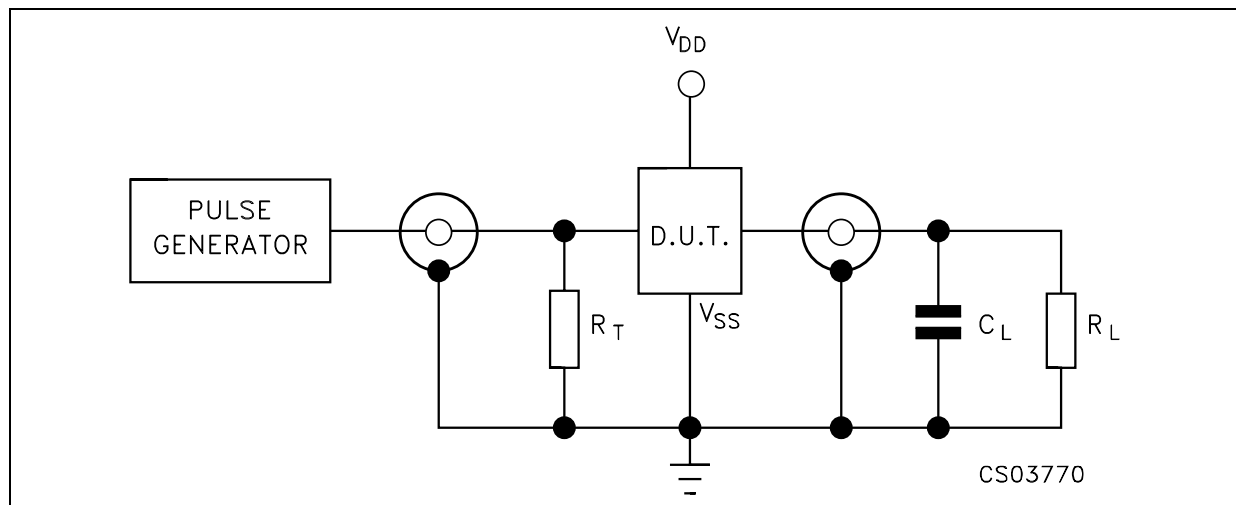
## DYNAMIC ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ , $C_L = 50\text{pF}$ , $R_L = 200\text{K}\Omega$ , $t_r = t_f = 20\text{ ns}$ )

Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PHL}$ $t_{PLH}$	Propagation Delay Time	5	Strobe or Data		485	970	ns
		10			185	370	
		15			135	270	
$t_{PHL}$ $t_{PLH}$	Propagation Delay Time	5	Inhibit		250	500	ns
		10			110	220	
		15			85	170	
$t_{THL}$ $t_{TLH}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$t_w$	Strobe Pulse Width	5		250	125		ns
		10		100	50		
		15		70	35		
$t_{setup}$	Setup Time	5		150	75		ns
		10		70	35		
		15		40	20		

(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C

(1) : If more than one unit is cascaded,  $t_r$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

### TEST CIRCUIT

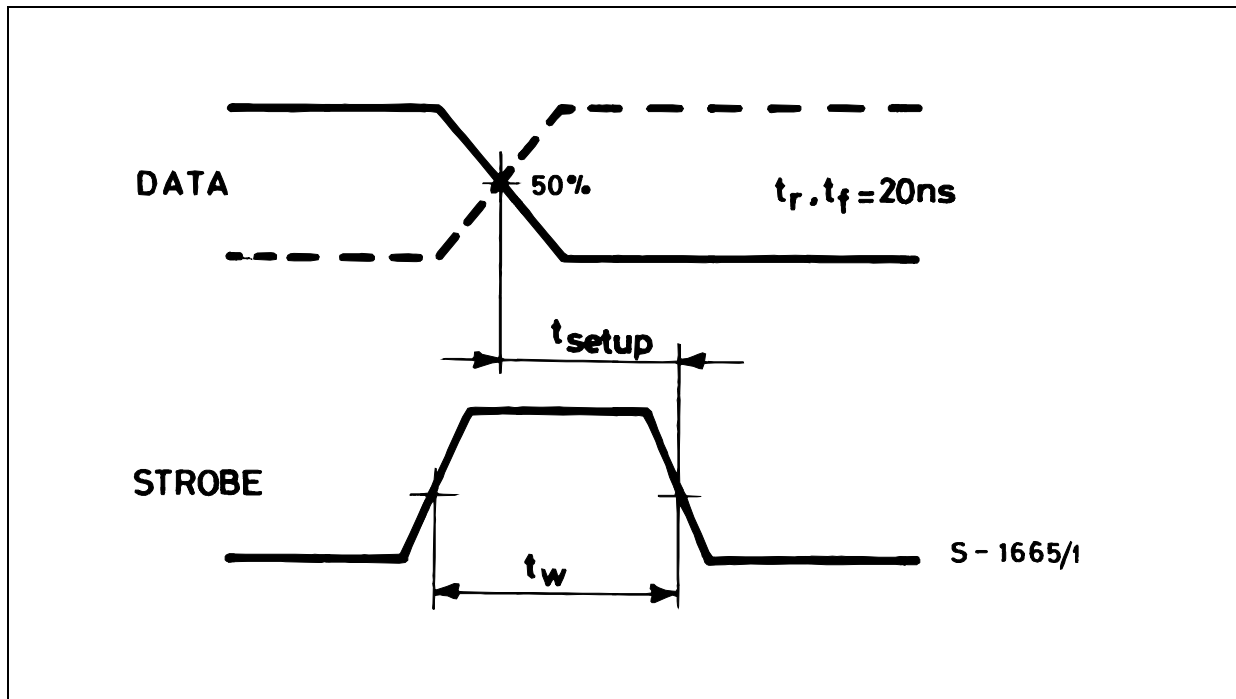


$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)

$R_L = 200\text{K}\Omega$

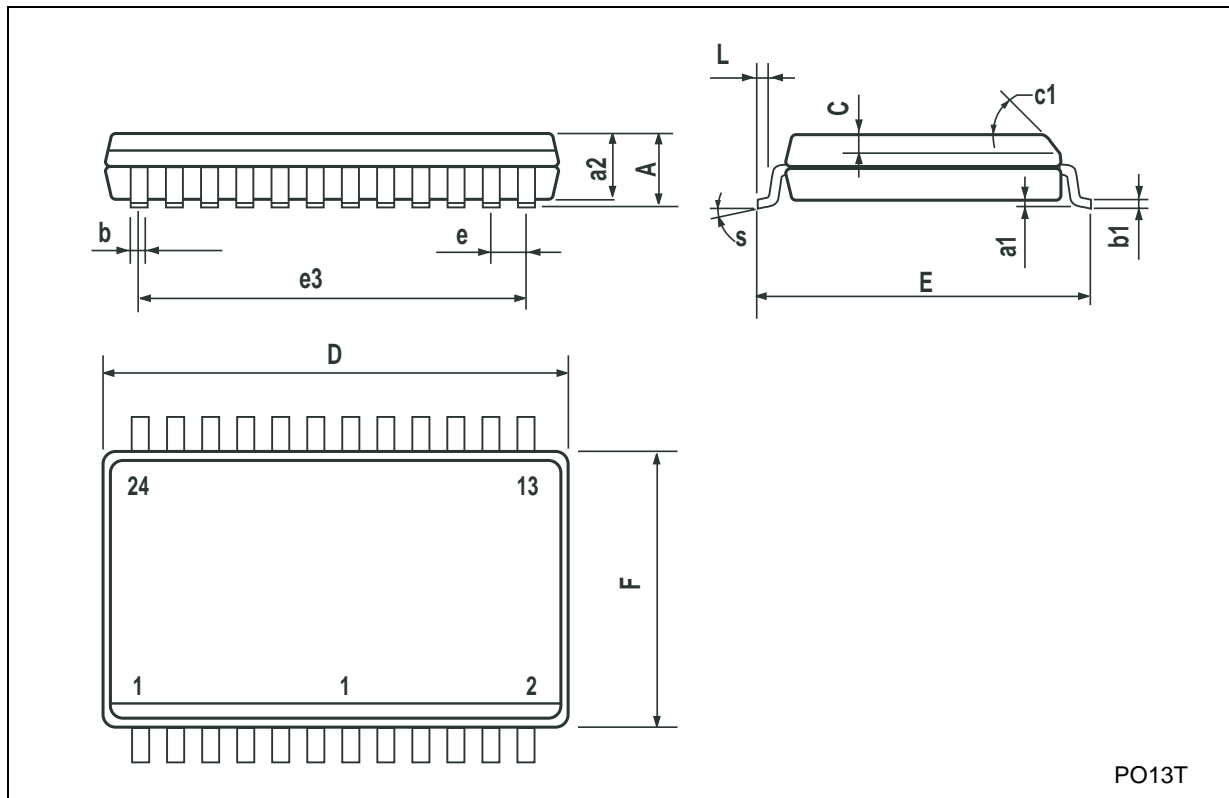
$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM : SETUP TIME and STROBE PULSE WIDTH (f=1MHz; 50% duty cycle)



**SO-24 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



PO13T



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