ZMD31010

RBic$_{Lite}$™ Low-Cost Sensor Signal Conditioner

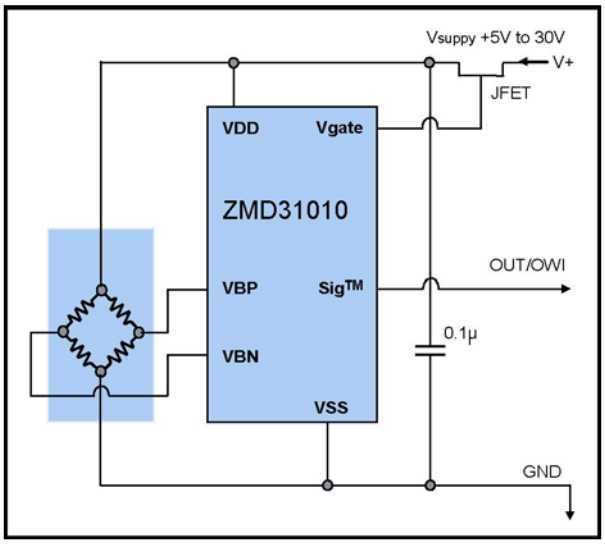
Datasheet PRELIMINARY

Features

- Digital compensation of sensor offset, sensitivity, temperature drift and non-linearity
- Accommodates differential sensor signal spans from 1.2mV/V to 60mV/V
- ZACwire™ one-wire interface.
- Internal temperature compensation and detection via bandgap PTAT*
- Optional sequential output of both temperature and bridge readings on ZACwire™ digital output
- Output options: rail-to-rail analog output voltage, absolute analog voltage, digital one-wire-interface
- Supply voltage 2.7 to 5.5V, with external JFET 5.5V to 30V
- Current consumption, depending on adjusted sample rate: 0.25mA to 1mA
- Wide operational temperature: –50 to +150°C
- Fast response time 1ms(typical)
- High voltage protection up to 30V with external JFET
- Chopper-stabilized true differential ADC
- Buffered and chopper-stabilized output DAC

* Proportional to absolute temperature

Application Circuit



Typical RBic $_{Lite}$™ Application Circuit

Benefits

- No external trimming components required
- PC-controlled configuration and calibration via one-wire interface – simple, low cost
- High accuracy (±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -40 to 125°C)
- Single pass calibration – quick and precise
- Suitable for battery-powered applications
- Small SOP8 package

Brief Description

The RBic$_{Lite}$™ is a CMOS integrated circuit, which enables easy and precise calibration of resistive bridge sensors via EEPROM. When mated to a resistive bridge sensor, it will digitally correct offset and gain with the option to correct offset and gain coefficients and linearity over temperature. A second order compensation can be enabled for temperature coefficients of gain and offset or bridge linearity. RBic$_{Lite}$™ communicates via ZMD's ZACwire™ serial interface to the host computer and is easily mass calibrated in a Windows® environment. Once calibrated, the output SIG™ pin can provide selectable 0 to 1V, rail-to-rail ratiometric analog output, or digital serial output of bridge data with optional temperature data.

- **Development Kit available**
- **Multi-Unit Calibrator Kit available**
- **Support for industrial mass calibration available**
- **Quick circuit customization possible for large production volumes**

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

ZMD31010

RBic$_{Lite}$™ Low-Cost Sensor Signal Conditioner

Datasheet PRELIMINARY

CONTENTS

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

1 Circuit Description

1.1 Signal Flow and Block Diagram

The RBic$_{Lite}$™ series of resistive bridge sensor interface ICs were specifically designed as a cost-effective solution for sensing in building automation, industrial, office automation and white goods applications.

The RBic$_{Lite}$™ employs ZMD's high precision bandgap with proportional-to-absolute-temperature (PTAT) output; low-power 14-bit ADC; and on-chip DSP core with EEPROM to precisely calibrate the bridge output signal.

Three selectable outputs, two analog and one digital, offer the ultimate in versatility across many applications.

The RBic$_{Lite}$™ rail-to-rail ratiometric analog output V_{out} signal (0 to 5V V_{out} @ V_{DD}=5V) suits most building automation and automotive requirements.

Typical office automation and white goods applications require the 0~1V_{out} signal, which in the RBic$_{Lite}$™ is referenced to the internal bandgap.

Direct interfacing to µP controllers is facilitated via ZMD's single-wire serial ZACwire™ digital interface.

RBic$_{Lite}$™ is capable of running in high-voltage (5.5-30V) systems when combined with an external JFET.

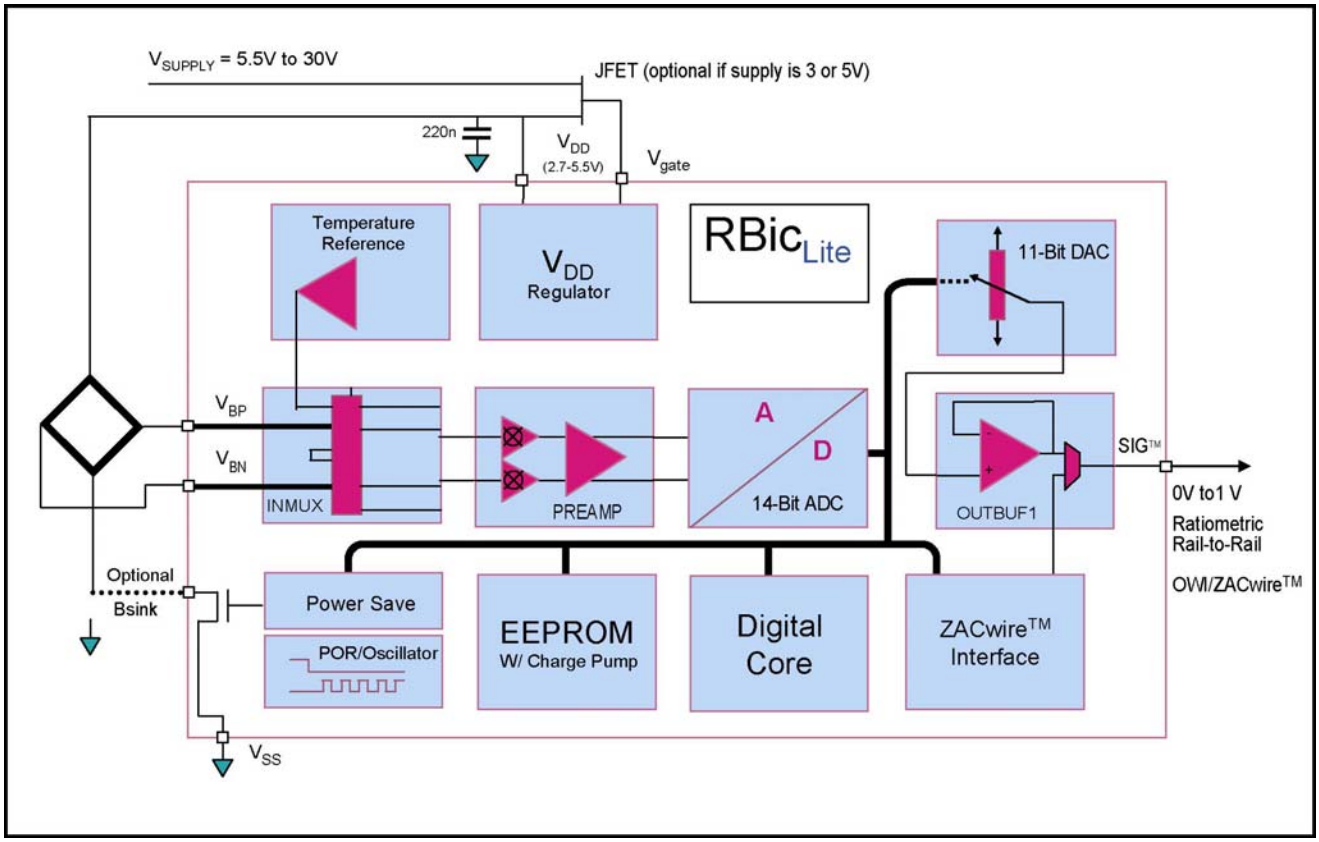


Figure 1.1 – RBic$_{Lite}$™ Block Diagram

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

1.2 Analog Front End

1.2.1 Bandgap/PTAT and PTAT Amplifier

The Bandgap/PTAT provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm Bandgap provides a stable voltage reference over temperature for the operation of the rest of the IC.

The PTAT signal is amplified through a path in the pre-amp and fed to the ADC for conversion. The most significant 12-bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in digital mode only the most significant 8-bits are given.

1.2.2 Bridge Supply

The voltage driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the RBic$_{Lite}$™ also includes a switched transistor to interrupt the bridge current via pin 1 (Bsink). The transistor switching is synchronized to the A-to-D conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5% or 1%.

1.2.3 Pre-Amp Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance designed for low noise and low drift. This pre-amp provides gain for the differential signal and re-centers its DC to $V_{DD}/2$. The output of the Pre-Amp block is fed into the A-to-D converter. The calibration sequence performed by the digital core includes an auto zero sequence to null any drift in the Pre-Amp state over temperature.

The Pre-Amp is nominally set to a gain of 24. Other possible gain settings are 6,12, and 48.

The inputs to the Pre-Amp from (VBN/VBP pins) can be reversed via an EEPROM configuration bit.

1.2.4 Analog to Digital Converter (ADC)

A 14-bit/1ms 2nd order charge-balancing analog-to-digital converter is used to convert signals coming from the pre-amplifier. The converter, designed in full differential switched capacitor technique, is used for converting the various signals in the digital domain. This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independent from clock frequency drift and clock jitter
- Fast conversion time owing to second order mode

Four selectable values for the zero point of the input voltage allow conversion to adapt to the sensor's offset parameter. Together with the reverse input polarity mode, this results in four possible zero point adjustments.

The conversion rate varies with the programmed update rate. The fastest conversation rate is 1k samples/s and the response time is then 1ms. Based on a best fit, the Integral Nonlinearity (INL) is less then 4 LSB$_{14Bit.}$

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

1.3 Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as performing temperature correction, and computing temperature value for output on the digital channel.

The digital core reads correction coefficients from EEPROM, and can correct for:

1. Bridge Offset
2. Bridge Gain
3. Variation of Bridge offset over Temperature (Tco)
4. Variation of Bridge gain over Temperature (Tcg)
5. A single second order effect (SOT) (Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following

- 2nd Order behavior of bridge measurement
- 2nd Order behavior of Tco
- 2nd Order behavior of Tcg

If the SOT applies to correcting the bridge reading then the correction formula for the bridge reading is represented as a two step process as follows:

$$\mathbf{ZB} = \mathbf{Gain_B}[1 + \Delta\mathbf{T}*\mathbf{Tcg}]*[\mathbf{BR\_Raw} + \mathbf{Offset_B} + \Delta\mathbf{T}*\mathbf{Tco}]$$

$$\mathbf{BR} = \mathbf{ZB}*(1.25+\mathbf{SOT}*\mathbf{ZB})$$

Where:

BR	=	Corrected Bridge reading that is output as digital or analog on SIG™ pin.
ZB	=	Intermediate result in the calculations.
BR_Raw	=	Raw Bridge reading from A2D.
T_Raw	=	Raw Temp reading converted from PTAT signal
Gain_B	=	Bridge gain term
Offset_B	=	Bridge offset term
Tcg	=	Temperature coefficient gain
Tco	=	Temperature coefficient offset
ΔT	=	(**T_Raw** - $\mathbf{T_{SETL}}$)
T_Raw	=	Raw Temp reading converted from PTAT signal
$\mathbf{T_{SETL}}$	=	T_Raw reading at which low calibration was performed (typically 25C)
SOT	=	Second Order Term

If the **SOT** applies to correcting 2nd Order behavior of **Tco** then the formula for bridge correction is as follows:

$$\mathbf{BR} = \mathbf{Gain\_B[1 + \Delta T*Tcg]*[BR\_Raw + Offset\_B + \Delta T(SOT*\Delta T + Tco)]}$$

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

If the SOT applies to correcting 2nd Order behavior of Tcg then the formula for bridge correction is as follows:

BR = Gain_B[1 + ΔT(SOT*ΔT + Tcg)]*[BR_Raw + Offset_B_ + ΔT*Tco)]

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

Corrected Temp Reading:

T = **Gain_T***[**T_Raw** + **Offset_T**]

Where:

T_Raw	=	Raw Temp reading converted from PTAT signal
Offset_T	=	TempSensor offset coefficient
Gain_T	=	TempSensor gain coefficient

1.3.1 EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. When programming the EEPROM, an internal charge pump voltage is used thus a high voltage supply is not needed.

The charge pump is internally regulated to 12.5 V voltage and the programming time amounts to 6ms.

1.3.2 One-Wire Interface - ZACwire™

The IC communicates via a one-wire serial interface. There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration Commands
- Entering various test modes
  - DAC test modes
  - Oscillator, 1V, and Pre-Amp
  - EEPROM test modes
  - Oscillator override & Scan test modes
- Reading from the EEPROM (dump of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

1.4 Output Stage

1.4.1 Digital to Analog Converter (Output DAC)

An 11-bit DAC based on sub-ranging resistor strings is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Selection during calibration configures the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption.

1.4.2 Output Buffer

A rail-to-rail op amp configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 2.5kΩ and capacitances up to 15nF. In addition, to limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces offset voltage to < 1mV.

1.4.3 Voltage Reference Block

This block uses the absolute reference voltage provided by the bandgap to produce two regulated on-chip voltage references. A 1V reference is used for the output DAC high reference when the part is configured in 0-1V analog output mode. For this reason, the 1V reference must be very accurate and includes trim so that its value can be trimmed within +/- 2mV of 1.00V. The 1V reference is also used as the on-chip reference for the JFET regulator block. Thus the regulation set point of the JFET regulator can be fine tuned using the 1V trim.

1V Reference Trim (1V vs. Trim for Nominal Process Run):

1Vref_trim3	1Vref_trim2	1Vreft_trim1	1Vref_trim0	1Vref deltaV	5Vref deltaV
1	1	1	1	-0.0184	-0.0920
1	1	1	0	-0.0161	-0.0805
1	1	0	1	-0.0138	-0.0690
1	1	0	0	-0.0115	-0.0575
1	0	1	1	-0.0092	-0.0460
1	0	1	0	-0.0069	-0.0345
1	0	0	1	-0.0046	-0.0230
1	0	0	0	-0.0023	-0.0115
0	1	1	1	Nominal	Nominal
0	1	1	0	+0.0023	+0.0115
0	1	0	1	+0.0046	+0.0230
0	1	0	0	+0.0069	+0.0345
0	0	1	1	+0.0092	+0.0460
0	0	1	0	+0.0115	+0.0575
0	0	0	1	+0.0138	+0.0690
0	0	0	0	+0.0161	+0.0805

Sample: Programming “0000” → the trimmed voltage = nominal value + 0.0161V

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

1.5 Clock Generator / Power On Reset (CLKPOR)

If the power supply exceeds 2.5V (maximum), the reset signal de-asserts and the clock generator starts working at a frequency of approximately 512kHz (±20%). The exact value only influences the conversion cycle time and communication to the outside world but not the accuracy of signal processing. In addition, to minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator is used to supply the oscillator block.

1.5.1 Trimming the Oscillator

Trimming is performed at wafer level, and it is strongly recommended that this not be changed during calibration, as ZAC wire™ communication is no longer guaranteed at different oscillator frequencies.

Trimming Bits	Delta Frequency (KHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Sample: Programming ”011” → the trimmed frequency = nominal value – 110KHz

2 Functional Description

2.1 General Working Mode

The command/data transfer takes place via the one-wire Sig™ pin using the ZAC Wire™ serial communication protocol.

After Power ON the IC is waiting for 6ms(=Command window) for the Start_CM command.

Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM).

Command Mode (CM) can only be entered during the 6ms command window after Power ON. If the IC receives the Start_CM command during the command window, it remains in the Command Mode. The CM allows changing to one of the other modes via command. After command Start_RW, the IC is in the Raw Mode. Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by Power OFF. Raw Mode is used by the calibration software for collection of raw bridge and temperature data so the correction coefficients can be calculated.

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

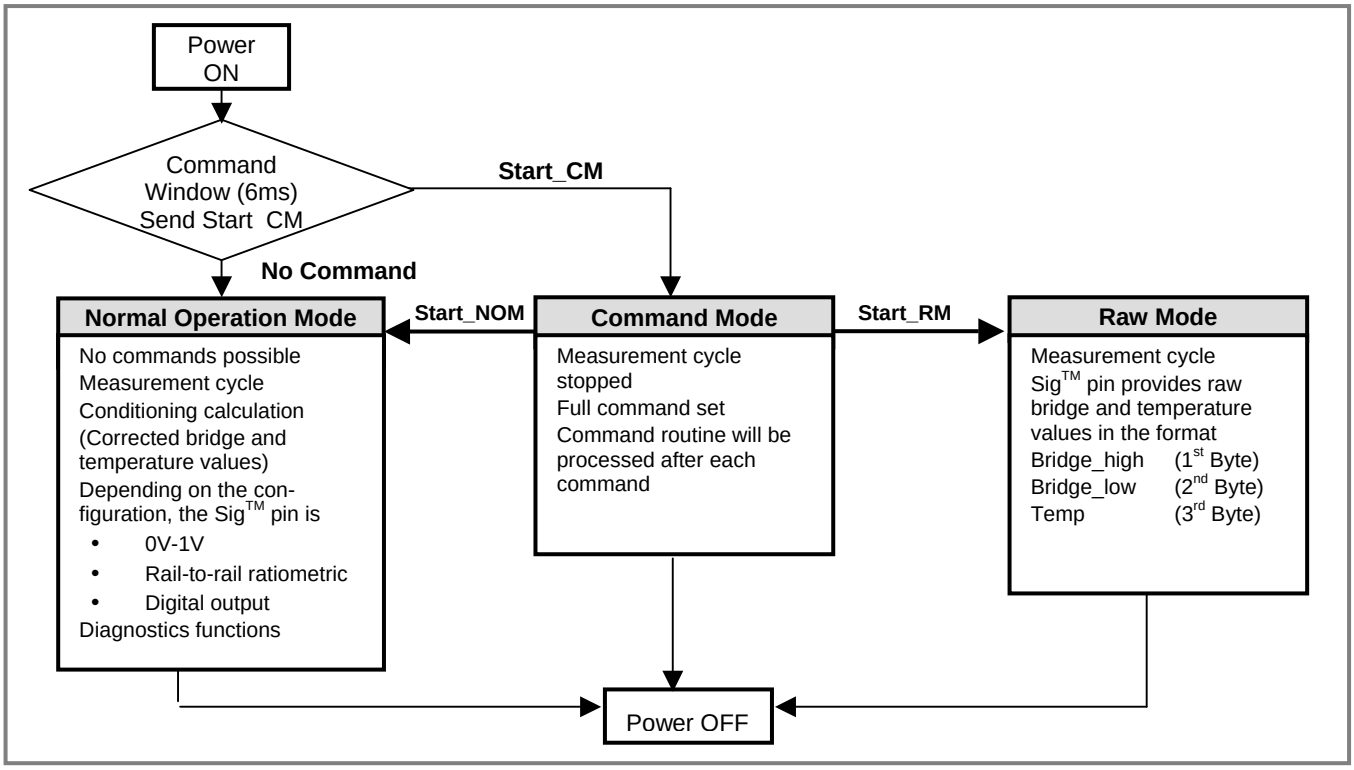


Figure 2.1 – General Working Mode

2.2 ZACwire™ Communication Interface

2.2.1 Properties and Parameters

	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during CM mode (first 6ms power up)
2	ZACwire™ rise time	$t_{ZAC,rise}$			9	µs	Any user RC network included in Sig™ path must met this rise time
3	ZACwire™ load capacitance	$C_{ZAC,load}$	0	1	15	nF	Also see section 6.3
4	Voltage level - low	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver
5	Voltage level - high	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.2.2 Bit Encoding

Start bit => 50% duty cycle used to set up strobe time

Logic 1 => 75% duty cycle

Logic 0 => 25% duty cycle

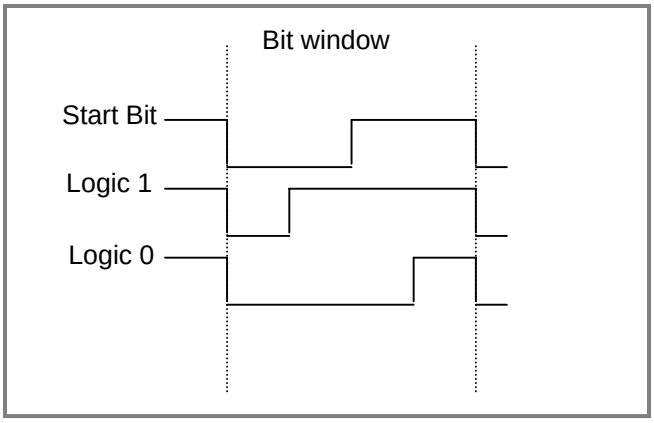


Figure 2.2 – Duty Cycle Manchester

2.2.3 Write Operation from Master to RBic$_{Lite}$™

The calibration master sends a 19-bit packet frame to the IC.

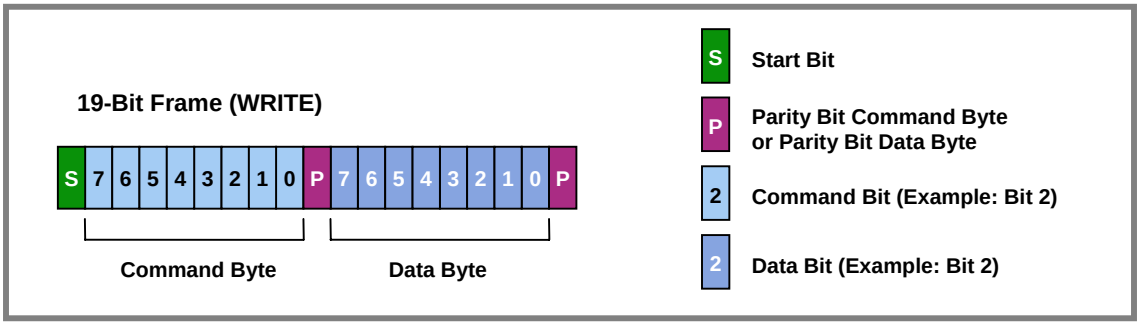


Figure 2.3 – 19-Bit Write Frame

The incoming serial signal will be sampled at a 512kHz clock rate. This protocol is very tolerant to clock skew and can easily tolerate baud rates in the 6kHz to 48kHz range.

2.2.4 RBIC$_{Lite}$™ READ Operations

The incoming frame will be checked for proper parity on both command and data bytes, as well as for any edge timeouts prior to a full frame being received.

Once a command/data pair is received, the RBic$_{Lite}$™ will perform that command. Once the command has been successfully executed by the IC, it will acknowledge success by a transmission of an A5H byte back to the master. If the master does not receive an A5H transmission within 130msec of issuing the command, it must assume the command was either improperly received or could not be executed.

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

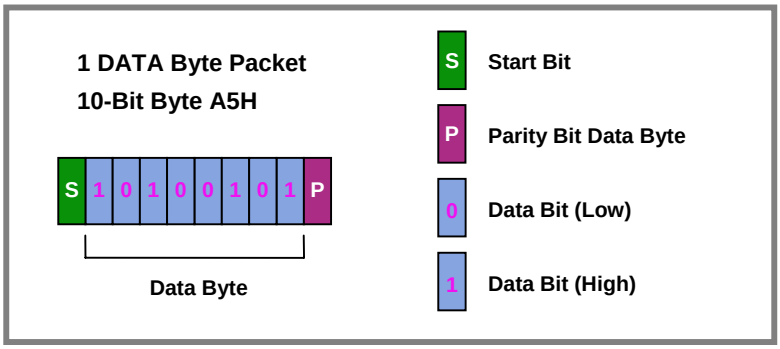


Figure 2.4 – Read Acknowledge

The RBic$_{Lite}$™ transmits 10-bit bytes (1 start bit, 8 data, 1 parity). During calibration and configuration, transmissions are normally either A5H or data. A5H indicates successful completion of a command. There are two different digital output modes configurable (digital output with temperature and digital output with only bridge data). During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data followed by the low byte. The bridge data is 14-bits in resolution, so the upper two bits of the high byte are always zero padded. There is a half stop bit time between bytes in a packet. That means for the time of a half a bit width, the signal level is high.

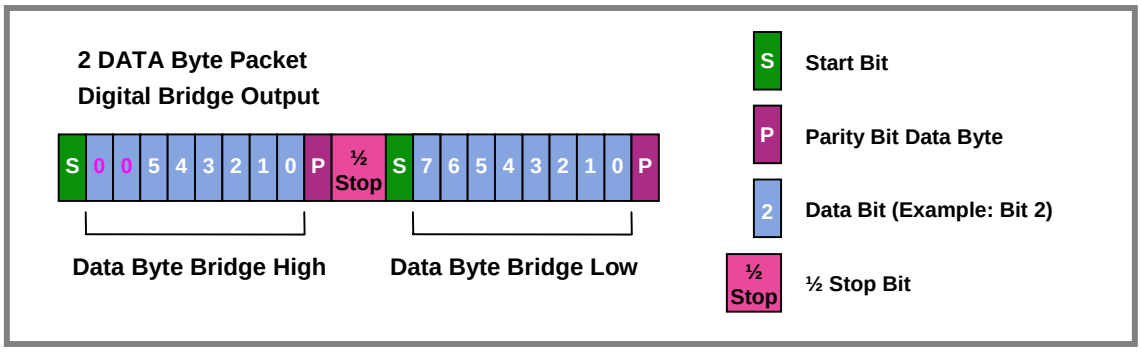


Figure 2.5 – Digital Output (NOM) Bridge Readings

The second different digital output mode is digital output bridge reading with temperature. It will be transmitted as 3 data packets. The temperature byte represents an 8-bit temperature quantity spanning from –50°C to 150°C.

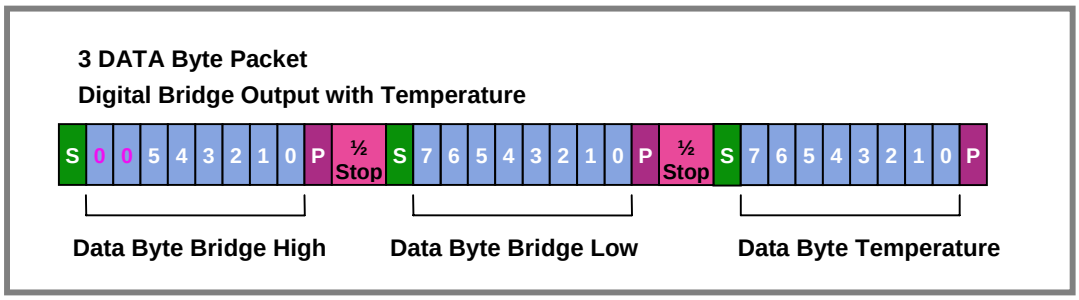


Figure 2.6 – Digital Output (NOM) Bridge Readings with Temperature

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

The EEPROM transmission occurs in a packet with 14 data bytes as shown in Figure 2.7.

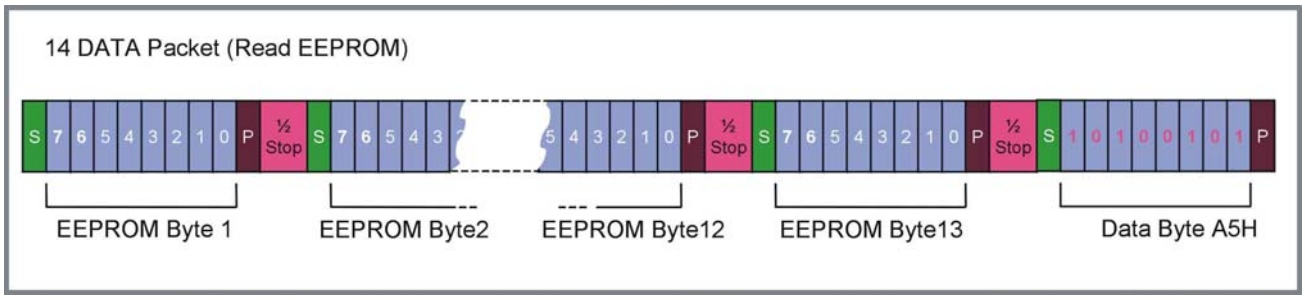


Figure 2.7 – Read EEPROM Contents

There is a variable idle time between packets. This idle time varies with the update rate setting in EEPROM.

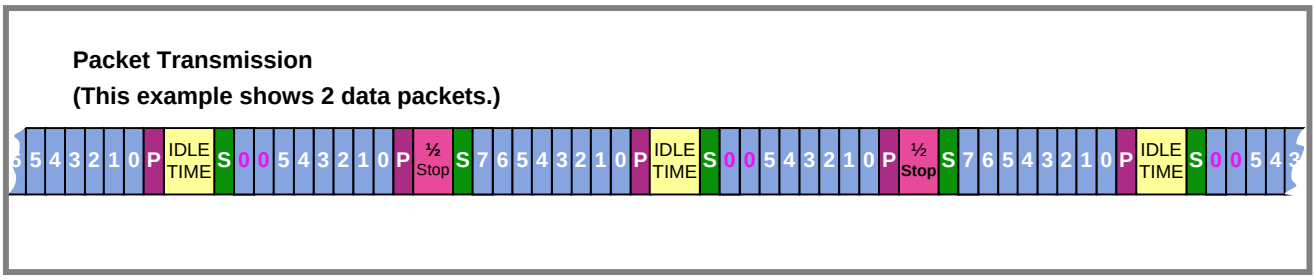


Figure 2.8 – Transmission of a Number of Data Packets

The table below shows the idle time between packets versus update rate. This idle time can vary by nominal +/-15% between parts and over a temperature range of –50°C to 150°C

Update Rate Setting:	Idle Time between Packets:
00	1ms
01	4.85ms
10	22.5ms
11	118ms

Transmissions from the IC occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (1ms or 5ms) then the baud rate of digital transmission will be 32kHz. If however, the user chooses one of the two slower update rates (25ms or 125ms), then the baud rate of digital transmission will be 8kHz.

One can easily program any standard µcontroller to communicate with the RBic$_{Lite}$™. ZMDA can provide sample code for a MicroChip PIC µController.

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.2.5 High Level Protocol

The RBic$_{Lite}$™ will listen for a command/data pair to be transmitted for the 6ms after the de-assert of its internal Power On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In NOM, it will output bridge data in either 0-1V analog, rail-to-rail ratiometric analog output, or digital depending on how the part is currently configured.

If the RBic$_{Lite}$™ receives a Start CM command within the first 6ms after the de-assert of POR, then it will go into Command Mode(CM). In this mode, calibration/configuration commands will be executed. The RBic$_{Lite}$™ will acknowledge successful execution of commands by transmission of an A5H. The calibrating/configuring master will know a command was not successfully executed if no response is received after 130ms of issuing the command. Once in command interpreting/executing mode, the RBic$_{Lite}$™ will stay in this mode until power is removed, or a Start NOM (Start Normal Operation Mode) command is received. The START CM command is used as an interlock mechanism to prevent a spurious entry into command mode on power up. The first command received within the 6ms window of POR must be a START CM command to enter into command interpreting mode. Any other commands will be ignored.

2.3 Command/Data Pair Encoding

The 16-bit command/data stream sent to the RBic$_{Lite}$™ can be broken into four 4-bit nibbles. The most significant nibble encodes the command. The 2nd nibble is reserved for possible future expansion, and should be sent as “0x0”. The last two nibbles encode the data byte.

Command nibble:	Data:	Description:
0H	0XXH	Read EEPROM Command via SIG™ pin.
2H	0YXH	Enter Test Mode (Subset of command mode for testing purpose only): SIG™ pin will assume the value of different internal test points, depending on most significant nibble of data sent. Y = 0H => Internal oscillator Y = 1H => 2.5V reference Y = 2H => PTAT Y = 3H => Pre-Amp Output+ Y = 4H => Scan Mode (SDO* routed to SIG ™ pin, part goes into Clock Override Mode and Scan Mode) Y = 5H => DAC Ramp testmode. Gain_b[13:3] contains the starting point, and the increment is (offset_b/8). The increment will be added every 125usec. Y = 6-7H => Part goes into Clock Override Mode. Y = 8-FH => Undefined.

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

<table>
<tr><th>Command nibble:</th><th>Data:</th><th>Description:</th></tr>
<tr><td>3H

X => Don’t care

H => Hex</td><td>0WDH

W => What

D => Data

H => Hex</td><td>Trim/Configure: 3rd nibble determines what is trimmed/configured. 4th nibble is data to be programmed.
<table>
<tr><th>3rd nibble</th><th>4th data nibbles</th><th>Description:</th></tr>
<tr><td>0H</td><td>XH</td><td>Trim oscillator least significant 3 bits of data used.</td></tr>
<tr><td>1H</td><td>XH</td><td>Trim 1V reference. Least significant 4 bits of data used.</td></tr>
<tr><td>2H</td><td>XH</td><td>Offset Mode. Least significant 2 bits of data used.</td></tr>
<tr><td>3H</td><td>XH</td><td>Set output mode. Least significant 2 bits used.</td></tr>
<tr><td>4H</td><td>XH</td><td>Set update rate. Least significant 2 bits used.</td></tr>
<tr><td>5H</td><td>XH</td><td>Configure JFET regulation</td></tr>
<tr><td>6H</td><td>XH</td><td>Program the tc_cfg register.
Least significant 3-bits used. Most significant bit of data nibble should be 0.</td></tr>
<tr><td>7H</td><td>XH</td><td>Program bits [99:96] of EEPROM. {SOT_cfg,Pamp_Gain}</td></tr>
<tr><td>8H</td><td>XH</td><td>Clear all case: Used to clear all bits in EEPROM to 0.</td></tr>
<tr><td>9H</td><td>XH</td><td>0101… case: Used to set whole EEPROM to alternating pattern.</td></tr>
<tr><td>AH</td><td>XH</td><td>1010…case: Used to set opposite alternating pattern.</td></tr>
<tr><td>BH</td><td>XH</td><td>Set all case: Used to set all bits in EEPROM to 1.</td></tr>
<tr><td>CH</td><td>XH</td><td>EEPROM Endurance Mode.
Initial setting of Offset_B[13:3] determines the # of cycles. Offset_t must be programmed to zero initially.</td></tr>
<tr><td>7H & C-FH</td><td>XH</td><td>Reserved.</td></tr>
</table></td></tr>
</table>

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

Command nibble:	Data:	Description:
4H	000H	Start NOM => Ends Command Mode, transition to Normal Operation Mode Mode.
4H	010H	Start Raw Mode (RM) In this mode if Gain_B = 800H, and Gain_T = 80H then the digital output will simply be the raw values of the A2D for the Bridge reading, and the PTAT conversion.
5H	000H	START CM => Start the Command Mode, used to enter command interpret mode. If data is sent with this command then that data sets up the start data for the DAC Test Mode.
6H	0YYH	Program SOT (2nd Order Term).
7H	0YYH	Program TSETL
8H	0YYH	Program Gain$_B$ upper 7-bits
9H	0YYH	Program Gain$_B$ lower 8-bits
AH	0YYH	Program Offset$_B$ upper 6-bits
BH	0YYH	Program Offset$_B$ lower 8-bits
CH	0YYH	Program GainT
DH	0YYH	Program OffsetT
EH	0YYH	Program Tco
FH	0YYH	Program Tcg

*SDO: Scan Data Out

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.4 Calibration Sequence:

Although the RBic$_{Lite}$™ IC can work with many different types of resistive bridges, lets assume a pressure bridge for the following discussion on calibration.

Calibration essentially involves collecting raw bridge and temperature data from the IC for different known pressures and temperatures. This raw data can then be "crunched" by the calibration master (lets assume a PC), and the calculated coefficients can then be written to the IC.

ZMDA can provide software and hardware with samples to perform the calibration.

There are three main steps to calibration:

1. Assigning a unique identification to the IC. This identification is programmed in EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings and temp reading for that part, as well as the known pressure and temperature the bridge was exposed to. This unique identification can be stored in a combination of the following EEPROM registers T_{SETL}, Tcg, Tco. These registers will be overwritten at the end of the calibration process, so this unique identification is not a permanent serial number.
2. Data collection. Data collection involves getting raw data from the bridge at different known pressures and temperatures. This data is then stored on the calibration PC using the unique identification of the IC as the index to the database.
3. Coefficient calculation and write. Once enough data points have been collected to calculate all the desired coefficients then the coefficients can be calculated by the calibrating PC and written to the IC.

Step 1 Assigning Unique Identification

Assigning a unique identification number is as simple as using the commands Program TSETL, Program Tcg, and Program Tco. These 3 8-bit registers will allow for 16Meg unique devices. In addition Gain_B needs to be programmed to 800H (unity) and Gain_T needs to be programmed to 80H (unity).

Step 2 Data Collection

The number of different unique (pressure, temperature) points that calibration needs to be performed at depends on the customer's needs. The minimum is a 2-point calibration, and the maximum is a 5-point calibration. To acquire raw data from the part one has to get RBic$_{Lite}$™ to enter Raw Mode. This is done by issuing a Start CM (Start Command Mode 5000H) command to the IC followed by a Start RM (Start Raw Mode 4010H) command with the LSB of the upper data nibble set. Now if the Gain_B term was set to unity (800H) and the Gain_T term was also set to unity (80H) then the part will be in the Raw Mode and will be outputting raw data on its SIG™ pin instead of corrected bridge and temperature. The calibration system should now grab several of these data points (16 each of bridge and temperature is recommended) and average them. These raw bridge and temperature setting should be stored in the database along with the known pressure and temperature. The ouput format during Raw Mode is Bridge_High, Bridge_Low, Temp. Each of these being 8-bit quantities. The upper 2-bits of Bridge_High are zero filled. The Temp data (8-bits only) would not really be enough info for accurate temperature calibration. Therefore the upper three bits of

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

temp information are not given, but rather assumed known. Therefore effectively 11-bits of temperature information is provided in this mode.

Step 3 Coefficient Calculations

The math to perform the coefficient calculation is very complicated and will not be discussed in detail. There is a rough overview in the "Calibration Math" section. Rather ZMDA will provide software to perform the coefficient calculation. ZMDA can also provide source code of the algorithms in a C code format. Once the coefficients are calculated the final step is to write them to the EEPROM of the RBic$_{Lite}$™.

The number of calibration points required can be as few as two or as many as five. This depends on the precision desired, and the behavior of the resistive bridge in use.

1. 2-point calibration would be used if one simply wanted a gain and offset term for a bridge with no temperature compensation for either term.
2. 3-point calibration would be used if one wanted to have 1st order compensation for either a Tco or Tcg term but not both.
3. 3-point calibration could also be used if one wanted 2nd order correction for the bridge, but no temperature compensation of the bridge output.
4. 4-point calibration would be used if one wanted 1st order compensation for both Tco and Tcg
5. 4-point calibration could also be used if one wanted 1st order compensation for either Tco or Tcg but not both, and wanted 2nd order correction for the bridge measurement.
6. 5-point calibration would be used if one wanted both 1st order Tco correction and 1st order Tcg correction, plus a 2nd order correction that could be applied to one and only one of the following: 2nd order Tco, 2nd order Tcg, or 2nd order bridge.

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.5 EEPROM Bits

Programmed through the serial interface:

EEPROM Range	Description	Note
2:0	Osc_Trim	See the table in the “Trimming the Oscillator” section for complete data 100 => Fastest 101 => 3 clicks faster than nominal . 111 => 1 click faster than nominal 000 => Nominal 001 => 1 click slower than nominal . 010 => 2 clicks slower than nominal 011 => Slowest
6:3	1V_Trim/JFET_Trim	See table in the “Voltage Reference Block” section.
8:7	A2D_Offset	Offset selection: 11 => [-1/2,1/2] mode bridge inputs 10 => [-1/4,3/4] mode bridge inputs 01 => [-1/8,7/8] mode bridge inputs 00 => [-1/16,15/16] mode bridge inputs To change the bridge signal polarity set Tc_cfg[3](=Bit 87)
10:9	Output_Select	00 => Digital (3-bytes with parity) Bridge High {00,[5:0]} Bridge Low [7:0] Temp [7:0] 01 => 0-1V Analog 10 => Rail-to-rail ratiometric analog output 11 => Digital (2-bytes with parity) (No Temp) Bridge High {00,[5:0]} Bridge Low [7:0]
12:11	Update_Rate	00 => 1 msec (1kHz) 01 => 5 msec (200Hz) 10 => 25 msec (40Hz) 11 => 125 msec (8 Hz)

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

EEPROM Range	Description	Note
14:13	JFET_Cfg	00 => No JFET regulation (lower power) 01 => No JFET regulation (lower power) 10 => JFET regulation centered around 5.0V 11 => JFET regulation centered around 5.5V (i.e. overvoltage protection).
29:15	Gain_B	Bridge Gain: Gain_B[14] => mult x 8 Gain_B[13:0] => 14-bit unsigned number representing a number in the range [0,8).
43:30	Offset_B	Signed 14-bit offset for bridge correction
51:44	Gain_T	Temperature gain coefficient used to correct PTAT reading.
59:52	Offset_T	Temperature offset coefficient used to correct PTAT reading.
67:60	T_{SETL}	Stores Raw PTAT reading at temperature in which low calibration points were taken
75:68	Tcg	Coefficient for temperature correction of bridge gain term. Tcg = 8-bit magnitude of Tcg term. Sign is determined by tc_cfg (bits 87:84)
83:76	Tco	Coefficient for temperature correction of bridge offset term. Tco = 8-bit magnitude of Tco term. Sign and scaling are determined by tc_cfg (bits 87:84)
87:84	Tc_cfg	This 4-bit term determines options for Temperature compensation of the bridge. Tc_cfg[3] => If set, Bridge Signal Polarity flips Tc_cfg[2] => If set Tcg is negative Tc_cfg[1] => Scale magnitude of Tco term by 8 Tc_cfg[0] => If set Tco is negative

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

EEPROM Range	Description	Note
95:88	SOT	2nd Order Term. This term is a 7-bit magnitude with sign. SOT[7] = 1 ➔ negative SOT[7] = 0 ➔ positive SOT[6:0] = magnitude [0-127] This term can apply to a 2nd order Tcg correction or a 2nd order bridge correction. (See Tc_cfg above)
99:96	{SOT_cfg, Pamp_Gain}	Bits [99:98] = SOT_cfg 00 = SOT applies to Bridge 01 = SOT applies to Tcg 10 = SOT applies to Tco 11 = Prohibited Bits [97:96] = Pre-Amp Gain 00 => 6 01 => 24 (default setting) 10 => 12 11 => 48 (Only the default gain setting (24) is tested at the factory, all other gain settings are not guaranteed)

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.6 Calibration Math

2.6.1 Correction Coefficients

(All terms calculated external to the DUT and then programmed to EEPROM through serial interface)

Gain_B = Gain term used to compensate span of Bridge reading.

Offset_B= Offset term used to compensate offset of Bridge reading

Gain_T = Gain term used to compensate span of Temp reading

Offset_T = Offset term used to compensate offset of Temp reading

SOT = Second Order Term. This term can be used applied as a second order correction term for:

1. The bridge measurement
2. Temperature coefficient of offset (Tco)
3. Temperature coefficient of gain (Tcg)

EEPROM bits 99:98 determine what SOT applies to.

T_{SETL} = RAW PTAT reading at low temperature at which calibration was performed (typically at room temp)

Tcg = Temperature correction coefficient of bridge gain term

This term has a 8-bit magnitude, a sign bit, and a scaling bit which can multiply its magnitude by 8.

Tco = Temperature correction coefficient of bridge offset term

This term has a 8-bit magnitude, and a sign bit..

2.6.2 Interpretation of Binary Numbers for Correction Coefficients:

BR_Raw should be interpreted as an unsigned number in the set [0,16383] with resolution of 1.

T_Raw should be interpreted as an unsigned number in the set [0,16383] with resolution of 4

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.6.2.1 Gain_B interpretation

Gain_B should be interpreted as a number in the set [0,8). The MSB (bit 14) is a scaling bit that will multiply the effect of the $Gain_B$ term by 8. The remaining bits ($Gain_B$[13:0]) represent a number in the range of [0,8) with $Gain_B$[13] having a weighting of 4, and each subsequent bit has a weighting of ½ the previous bit.

Table 2.1 – Gain_B Weightings

Bit Position:	Weighting:
13	4
12	2
11	1
.	
.	
.	
1	2^{-10}
0	2^{-11}

Examples:

The binary number: 010010100110001 = 4.6489; The scaling number is 0 so there is no multiply by 8 of the number represented by Gain_B[13:0]

The binary number: 101100010010110 = 24.586; The scaling number is 1 so there is a multiply by 8 of the number represented by Gain_B[13:0]

Limitation: Using the 5-point calibration 5pt-Tcg&Tco&SOT_Tco (including the second order SOT_Tco), the Gain_B is limited to a value equal or less than 8 (instead of 64).

2.6.2.2 Offset_B Interpretation

Offset_B is a 14-bit signed binary number in two's complement form. This implies the MSB has a weighting of –8192. The following bits then have a weighting of: 4096, 2048, 1024, …

Table 2.2 – Offset_B Weightings

Bit Position:	Weighting:
13	-8192
12	4096
11	2048
.	
.	
.	
1	$2^1 = 2$
0	$2^0 = 1$

Thus the binary number: 11111111111100 = -4

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.6.2.3 Gain_T interpretation

Gain_T should be interpreted as a number in the set [0,2). Gain_T[7] having a weighting of 1, and each subsequent bit has a weighting of ½ the previous bit.

Table 2.3 – Gain_T Weightings

Bit Position:	Weighting:
7	1
6	0.5
5	0.25
.	
.	
.	
1	2^{-6}
0	2^{-7}

2.6.2.4 Offset_T Interpretation

Offset_T is an 8-bit signed binary number in two's complement form. This implies the MSB has a weighting of –128. The following bits then have a weighting of: 64, 32, 16 …

Table 2.4 – Offset_T Weightings

Bit Position:	Weighting:
7	-128
6	64
.	
.	
.	
1	$2^1 = 2$
0	$2^0 = 1$

Thus the binary number: 00101001 = 41

2.6.2.5 Tco Interpretation

Tco is specified as an 8-bit magnitude with an additional sign bit and a scalar bit. The scalar bit when set multiplies the signed Tco by 8.

Tco Resolution:	0.175uV/V/^{o}C	(input referred)
Tco Range:	+/- 44.6uV/V/^{o}C	(input referred)

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

If the scaling bit is used then the above resolution and range are scaled by 8 to give:

Tco Scaled Resolution:	1.40uV/V/°C input referred
Tco Scaled Range:	+/- 357uV/V/°C input referred

2.6.2.6 Tcg Interpretation

Tcg is specified as an 8-bit magnitude with an additional sign bit.

The resolution of Tcg is:	17.0ppm/°C
The range of Tcg is:	+/- 4335ppm/°C

2.6.2.7 SOT Interpretation

SOT is a second order term that can apply to one and only one of the following: (bridge non-linearity correction, Tco non-linearity correction, or Tcg non-linearity correction.

As it applies to bridge non-linearity correction:

The resolution is:	0.25% @ Full Scale
The range is:	+31.75% @ Full Scale to -16% @ Full Scale
	(Saturation in internal arithmetic will occur at greater negative non-linearities)

As it applies to Tcg:

The resolution is:	0.3 ppm/(°C)^2
The range is:	+/- 38ppm/(°C)^2

As it applies to Tco:

2 settings are possible. It is possible to scale the effect of SOT by 8. If Tc_cfg[1] is set, then both Tco and SOT's contribution to Tco are multiplied by 8.

Resolution at unity scaling:	1.51nV/V/(°C)^2	(input referred)
Range:	+/- 0.192µV/V/(°C)^2	(input referred)

Resolution at 8x scaling:	12.1nV/V/(°C)^2	(input referred)
Range:	+/- 1.54µV/V/(°C)^2	(input referred)

Limitation: If the second order term SOT applies to Tco, the bridge gain Gain_B is limited to values equal or less than 8 (instead of 64).

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

2.7 Reading EEPROM Contents

The contents of the entire EEPROM memory can be read out using the Read EEPROM Command (00H). This command will cause the IC to output consecutive bytes on the ZAC Wire™. The interpretation of these bytes is given in the following table.

Read EEPROM (Bit order):

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1:	Offset_B[11:4]							
Byte 2:	Gain_T[1:0]		Offset_B[13:12]					
Byte 3:	Offset_T[1:0]		Gain_T[7:2]					
Byte 4:	T_{SETL}[1:0]		Offset_T[7:2]					
Byte 5:	Tcg[1:0]		T_{SETL}[7:2]					
Byte 6:	Tco[1:0]		Tcg[7:2]					
Byte 7:	Tc_cfg[1:0]		Tco[7:2]					
Byte 8:	SOT[5:0]		Tc_cfg[3:2]					
Byte 9:	Osc_Trim[1:0]		SOT_cfg[3:0]*				SOT[7:6]	
Byte 10:	Output_Select[0]	A2D_offset[1:0]		1V_Trim[3:0]**				Osc_Trim[2]
Byte 11:	Gain_B[2:0]			JFET_Cfg[1:0]		Update_Rate[1:0]		Output_Select[1]
Byte 12:	Gain_B[10:3]							
Byte 13:	Offset_B[3:0]				Gain_B[14:11]			
Byte 14:	A5H							

* SOT_cfg/Pamp_Gain

** 1V_Trim/JFET_Trim

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

3 Application Circuit Examples

Typical output analog load resistor R_L= 10kΩ (minimum 2.5kΩ). This optional load resistor can be configured as a pull-up or pull-down. If it is configured as a pull-down, it cannot be part of the module to be calibrated because this would prevent proper operation of the ZACwire™. If a pull-down load is desired, it must be added to system after module calibration.

There is no output load capacitance needed.

EEPROM contents: OUTPUT_select, JFET_Cfg, 1V_Trim/JFET-Trim

3.1 Three-Wire Rail-to-Rail Ratiometric Output

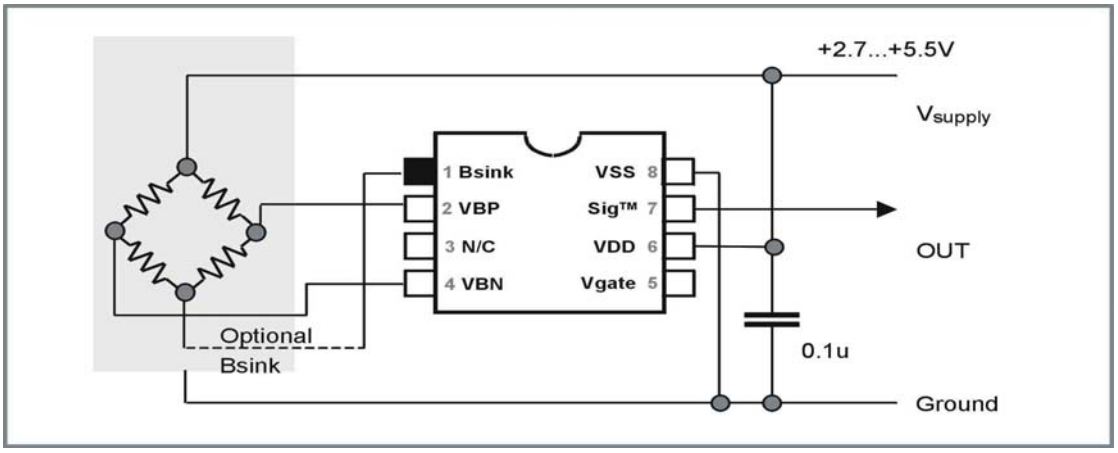


Figure 3.1 – Rail-to-Rail Ratiometric Voltage Output, Temperature Compensation via Internal PTAT.

The optional bridge sink allows a power savings of bridge current. The output voltage can be

a) Rail-to-rail ratiometric analog output V_{DD}(=Vsupply).

b) 0 to 1V analog output is also possible. The absolute voltage output reference is trimmable 1V (+/-2mV) in the 1V output mode via a 4-bit EEPROM field.

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

3.2 Analog Voltage Output

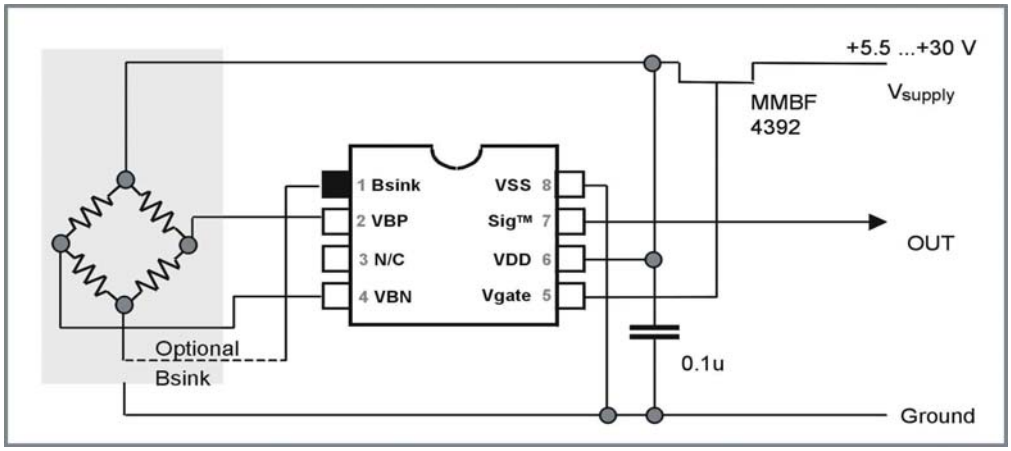


Figure 3.2 – Absolute Voltage Output with Temperature Compensation via Internal Temperature PTAT External JFET Regulation for all Industry Standard Applications

The output signal range is

a) 0 to 1V analog output. The absolute voltage output reference is trimmable 1V (+/-2mV) in the 1V output mode via a 4-bit EEPROM field.

b) Rail-to-rail analog output. The on-chip reference for the JFET regulator block is trimmable 5V (+8/-9mV) in the ratiometric output mode via a 4-bit EEPROM field.

3.3 Three-Wire Ratiometric Output with Over-Voltage Protection

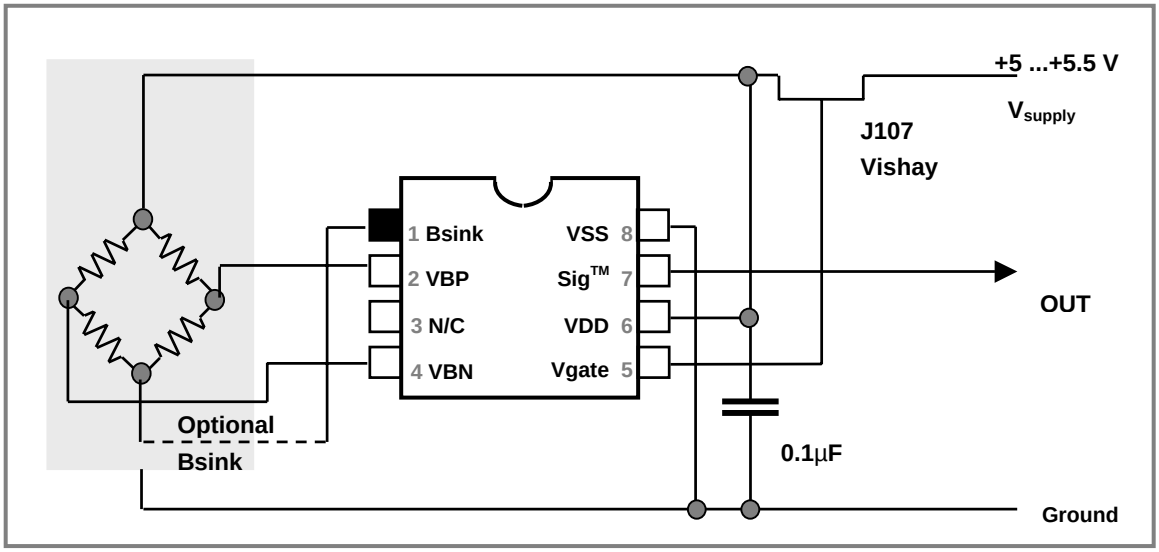


Figure 3.3 – Ratiometric Output, Temperature Compensation via Internal Diode

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

In this application, the JFET is used for voltage protection. The Config_JFET bits in EEPROM are configured to 5.5V. There is an additional maximal error of 8mV caused by non-zero r_{ON} of the limiter JFET.

3.4 Digital Output

For all three circuits the output signal can also be digital. Depending from the output select bits bridge signal or the bridge signal and temperature signal are sent.

For the digital output no load resistor or load capacity are necessary. No pull down resistor is allowed. If a line resistor or pull up resistor is used, the requirement for the rise time must be met (≤ 9 µs). The IC output includes a pull up resistor of about 100kΩ. The digital output can easily be read by firmware from a microcontroller and ZMD can provide the customer with software in developing the interface.

4 ESD/Latch-Up-Protection

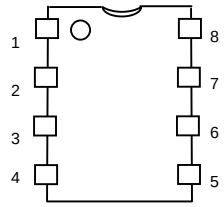
All pins have an ESD Protection of >4000V and a Latch-up protection of ±100mA or of +8V/ –4V (to VSS/VSSA). ESD Protection referred to the human body model is tested with devices in SOP-8 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

5 Pin Configuration and Package

Figure 5.1 – RBic$_{Lite}$™ Pin Out Diagram



The standard package of the RBic$_{Lite}$™ is SOP-8 (3.81mm body (150mil) wide) with lead-pitch. 1.27mm (50mil).

Pin-No.	Name	Description
1	Bsink	Optional ground connection for bridge ground. Used for power savings
2	VBP	Positive Bridge Connection
3	N/C	No Connection
4	VBN	Negative Bridge Connection
5	Vgate	Gate control for external JFET regulation/over-voltage protection
6	VDD	Supply voltage (2.7-5.5V)
7	Sig™	ZACWire™ interface (analog out, digital out, calibration interface)
8	VSS	Ground supply

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

6 IC Characteristics

6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{DD}	-0.3		6.0	V
Voltages at Analog I/O – In Pin	V_{INA}	-0.3		V_{DD}+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}	-0.3		V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	-50		150	°C
Storage Temperature Range	T_{STG}<10h	-50		170	°C

6.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage to Gnd	V_{DD}	2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}	5.5	7	30	V
Ambient Temperature Range [1&2]	T_{AMB}	-50		150	°C
External Capacitance between V_{DD} and Gnd	C_{VDD}	100	220	470	nF
Output Load Resistance to V_{SS} or V_{DD} [3]	$R_{L,OUT}$	2.5	10		kΩ
Output Load Capacitance [4]	$C_{L,OUT}$		10	15	nF
Bridge Resistance	R_{BR}	0.2 [5]		100	kΩ
Power ON Rise Time	t_{PON}			100	ms

[1] Note that the maximum calibration temperature is 85°C.

[2] If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.

[3] When using the output for digital calibration, no pull down resistor is allowed.

[4] Using the output for digital calibration, $C_{L,OUT}$ is limited by the maximum rise time $T_{ZACrise}$.

[5] Note: Minimum bridge resistance is only a factor if using the Bsink feature. The R_{DS}(ON) of the Bsink transistor is 1.1Ω when operating at VDD=5V, and 1.6Ω when operating at V_{DD}=3.0V. This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

6.3 Electrical Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE / REGULATION						
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At minimum update rate.		250		µA
		At maximum update rate.		1000		
Temperature Coefficient – PTAT Source	TC_{PTAT}			20	100	ppm/K*
Power Supply Rejection Ratio	PSRR		60			dB*
Power-On Reset Level	POR		1.4		2.6	V
ANALOG TO DIGITAL CONVERTER (ADC)						
Resolution	r_{ADC}			14		Bit
Integral Nonlinearity (INL)	INL_{ADC}	Based on ideal slope	-4		+4	LSB[1]
Differential Nonlinearity (DNL)	DNL_{ADC}		-1		+1	LSB*
Response Time	$T_{RES,ADC}$	Varies with update rate. Value given at fastest rate.		1		ms
ANALOG OUTPUT PARAMETERS (DAC + BUFFER)						
Max. Output Current	I_{OUT}	Max current maintaining accuracy	2.2			mA
Resolution	r_{OUT}	Referenced to V_{DD}			11	Bit
Absolute Error	E_{ABS}	DAC input to output	-10		+10	mV
Differential Nonlinearity	DNL	No missing codes	-0.9		+1.5	LSB_{11Bit}*
Upper Output Voltage Limit	V_{OUT}	R_L =2.5kΩ	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}				2.5	mV
ZAC_{wire}™ Serial Interface*						
ZAC_{wire}™ Line Resistance	$R_{ZAC,line}$				3.9[2]	kΩ
ZAC_{wire}™ Load Capacitance	$C_{ZAC,load}$				1[3]	nF
Voltage Level Low	$V_{ZAC,low}$			0	0.2	V_{DD}
Voltage Level High	$V_{ZAC,low}$		0.8	1		V_{DD}
TOTAL SYSTEM						
Start-Up-Time	t_{STA}	Power-up to output			10	ms
Response Time	t_{RESP}	Update_rate=<1ms		1	2	ms
Sampling Rate	f_S	Update_rate=<1ms		1000		Hz

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	Update_rate=<1ms		1		mA
Overall Linearity Error	E_{LIND}	Bridge input to output -- Digital		0.02	TBD	%
Overall Linearity Error	E_{LINA}	Bridge input to output -- Analog		0.1	TBD	
Overall Ratiometricity Error	RE_{out}	Not using Bsink feature		0.035	TBD	%
Overall Accuracy	AC_{out}	Only IC, without sensor bridge		TBD	0.3%	%FSO

** The parameters with an * under "Units" are tested by design.*

[1] Note this is +/- 4 LSBs to the 14-bit A-to-D conversion. This implies absolute accuracy to 12-bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.

[2] The rise time must be $t_{ZAC,rise} = 2\ R_{ZAC,load} * C_{ZACload} \leq 9\mu s$. If using a pull up resistor instead of the line resistor, it must meet this specification.

6.4 Analog Inputs

RBic $_{Lite}$™ incorporates an extended 14-bit charge-balanced ADC which allows for a single gain setting on the Pre-Amplifier to handle bridge sensitivities from 1.2 - 36mV/V while maintaining 8-12 bits of output resolution(default analog gain 24). The table below illustrates the minimum resolution achievable for a variety of bridge sensitivities.

Analog Gain 12				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
43.3	60.0	79.3	3%	13.0
36.1	50.0	66.1	17%	12.7
25.3	35.0	46.3	53%	12.2
18.0	25.0	33.0	101%	11.7
14.5	20.0	26.45	142%	11.4
7.2	10.0	13.22	351%	10.4
3.6	5.0	6.6	767%	9.4

[1] In addition to Tco,Tcg

 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

Analog Gain 24				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
16	25.0	36	25%	12.6
12.8	20.0	28.8	50%	12
6.4	10.0	14.4	150%	11
3.2	5.0	7.2	400%	10
1.6	2.5	3.6	900%	9
0.8	1.2	1.7	2000%	8

[1] *In addition to Tco,Tcg*

Analog Gain = 48				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
10.8	15.0	19.8	3%	13
7.2	10.0	13.2	35%	12.4
4.3	6.0	7.9	100%	11.7
2.9	4.0	5.3	190%	11.1
1.8	2.5	3.3	350%	10.4
1.0	1.4	1.85	675%	9.6
0.72	1.0	1.32	975%	9.1

[1] *In addition to Tco,Tcg*

6.5 Temperature Compensation and Temperature Output

A highly-linear Bandgap/PTAT circuit is used in order to produce a signal which can be used in compensation of the bridge over temperature. In addition, when digital mode is activated both bridge and temperature signals (8-bit temperature quantity) can be broadcast on the ZACwire™ pin.

6.6 High Voltage Operation

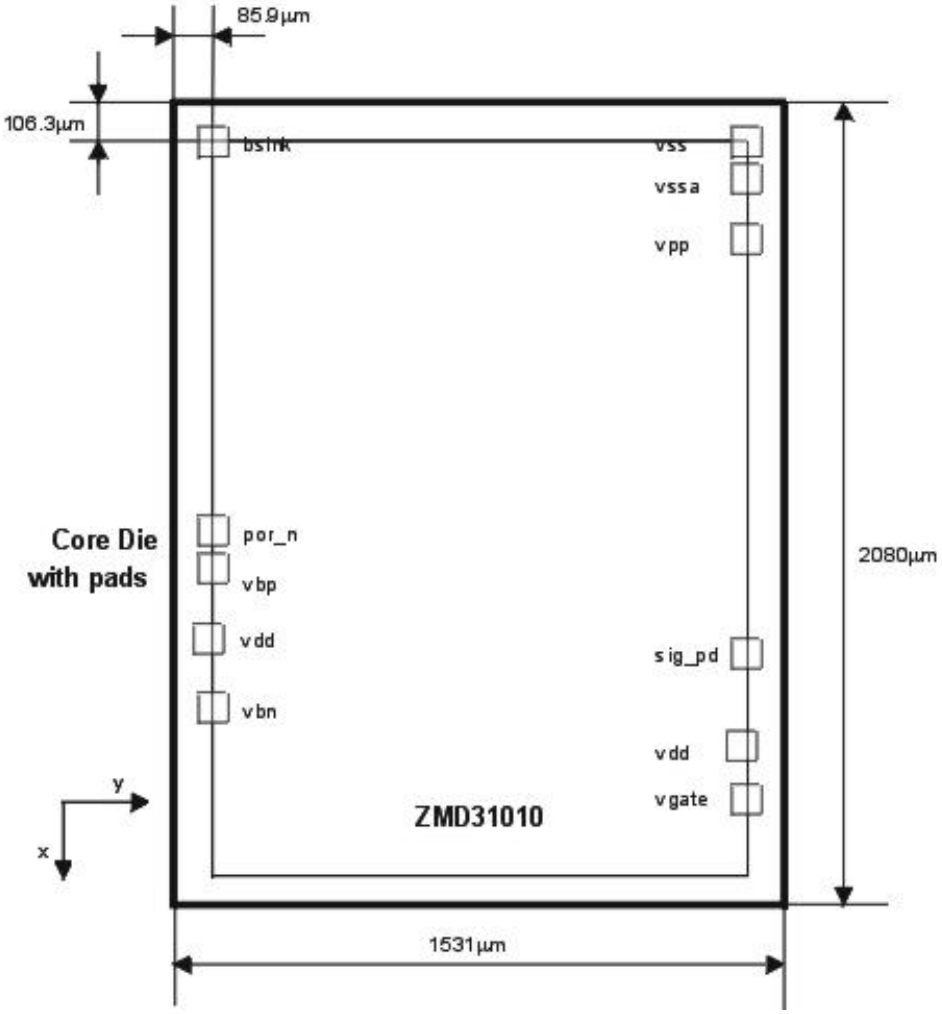
A linear regulator control circuit is included on the IC to interface with an external JFET to allow for operation in systems where the supply voltage exceeds 5.5V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjust (EEPROM bit) that can adjust the set point around 5.0 or 5.5V. In addition, the 1V trim will also act as a fine adjust for the regulation set point. Note: If using the external JFET for over-voltage protection purposes (i.e., 5V at JFET drain and expecting 5V at JFET source), there will be a voltage drop across the JFET, thus ratiometricity will be compromised somewhat depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice that would produce only an 8mV drop worst case. If using as regulation instead of over-voltage, a MMBF4392 also works well.

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

7 Die Dimensions and Pad Coordinates

7.1 Die Dimensions

- Die size (including scribeline): 2230µm x 1681µm ≈ 3.75sqmm
- Core die size (without scribeline): 2080µm x 1531µm ≈ 3.19sqmm
- Die thickness: 390µm
- Scribeline (distance between two core dice on wafer): 150µm
- Pads size: 68µm x 68µm



 © ZMD AG, 2005

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

7.2 Pad Coordinates

All pads coordinates are for pad centers and related to the corner.

Name	X Coordinate in µ	Y Coordinate in µ
bsink	106.3	85.9
por_n	1109.7	85.9
vbp	1210.0	85.9
vdd	1389.3	77.3
vbn	1568.1	85.9
vss	107.2	1444.7
vssa	198.3	1444.7
vpp	356.1	1444.7
sig_pd	1428.6	1444.7
vdd	1672.3	1435.8
vgate	1809.2	1444.7

8 Test

The test program is based on this datasheet. The final parameters that will be tested during series production are listed in the tables of section 6.3.

The digital part of the IC includes a scan path, which can be activated and controlled during wafer test. It guarantees failure coverage more than 98%. Further test support for testing of the analog parts on wafer level is included in the DSP.

9 Reliability

A reliability investigation according to the in-house non-automotive standard will be performed.

10 Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZM31010, ZMD can customize the circuit design by adding or removing certain functional blocks.

For it ZMD has a considerable library of sensor-dedicated circuitry blocks.

Thus ZMD can provide a custom solution quickly. Please contact ZMD for further information.

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.

11 Related Documents

- ZMD31010 RBic$_{Lite}$™ *Development Kit Documentation*
- ZMD31010 RBic$_{Lite}$™ *SSC Kits Feature Sheet* (includes ordering codes and price information)
- ZMD31010 RBic$_{Lite}$™ *Technical Notes – B1 Engineering Samples*
- ZMD31010 RBic$_{Lite}$™ *Application Notes – In-Circuit Programming Boards*
- ZMD31010 RBic$_{Lite}$™ *Die Dimensions and Pad Coordinates*
- ZMD31010 RBic$_{Lite}$™ *Multi-Unit Calibrator Kit Documentation*

For the most recent revisions of this document and of the related documents, please go to www.zmd.biz

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. ZMD assumes no obligation regarding future manufacture unless otherwise agreed in writing. The information furnished hereby is believed to be correct and accurate. However, ZMD shall not be liable to any customer, licensee or any other third party for any damages in connection with or arising out of the furnishing, performance or use of this technical data. No obligation or liability to any customer, licensee or any other third party shall result from ZMD's rendering of technical or other services.

For further information:

ZMD AG
Grenzstrasse 28
01109 Dresden, Germany
Phone +49 (0)351-8822-366
Fax +49 (0)351-8822-337
sales@zmd.de
www.zmd.biz

ZMD America, Inc.
201 Old Country Road, Suite 204
Melville, NY 11747, USA
Phone +01 (631) 549-2666
Fax +01 (631) 549-2882
sales@zmda.com
www.zmd.biz

All rights reserved. The material contained herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner. The Information furnished in this publication is preliminary and subject to changes without notice.