Digitally Programmable 2, 4 and 8 Mux LCD Driver

Features

- Very simple 1-bit interface (see Fig. 1)
- V6123 mux mode 2 with 2 rows and 58 columns
- V6123 mux mode 4 with 4 rows and 56 columns
- V6123 mux mode 8 with 8 rows and 52 columns
- Very simple 1-bit interface, reduced to its simplest form
- Frame frequency on chip by internal RC oscillator
- Voltage bias and mux signal generation on chip
- 1 display RAM addressable as 8 x 60 bit words
- Column driver only mode to have 60 column outputs
- No busy states
- No external components needed
- Blank function for LCD blanking
- Bit mapped
- Wide V_{DD} voltage supply range, 2 to 6 V
- Wide V_{LCD} voltage supply range, 2 to 8.5 V
- -40 to + 85 °C temperature range

Description

The V6123 is a low multiplex LCD driver. The 2, 4 and 8 way multiplex is digitally programmable by the command byte. The display refresh is handled on chip by an internal RC oscillator via 1 selectable 8 x 60 RAM which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 8 x 60 bit RAM (a set bit corresponds to an activated LCD pixel).
The V6123 has a very low dynamic current consumption, typically 175 μA at V_{DD} = 5 V, V_{LCD} = 7 V, making it particularly attractive for portable and battery powered products. The wide operating range on supply voltages and temperature offers much application flexibility. The LCD bias generation and frame frequency are generated on chip. The clock signal can be used to shift and to latch the data into the RAM.

Applications

- Automotive displays
- Telephones
- Pagers
- Portable, battery operated products
- Large displays (public information panels, etc.)
- Balances and scales
- Utility meters

Typical Operating Conditions

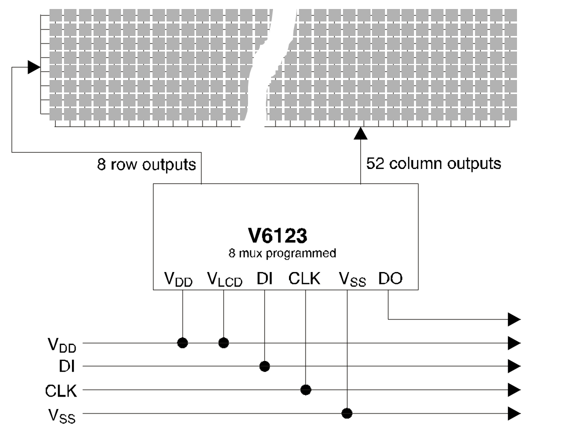


Fig. 1

Pad Assignment

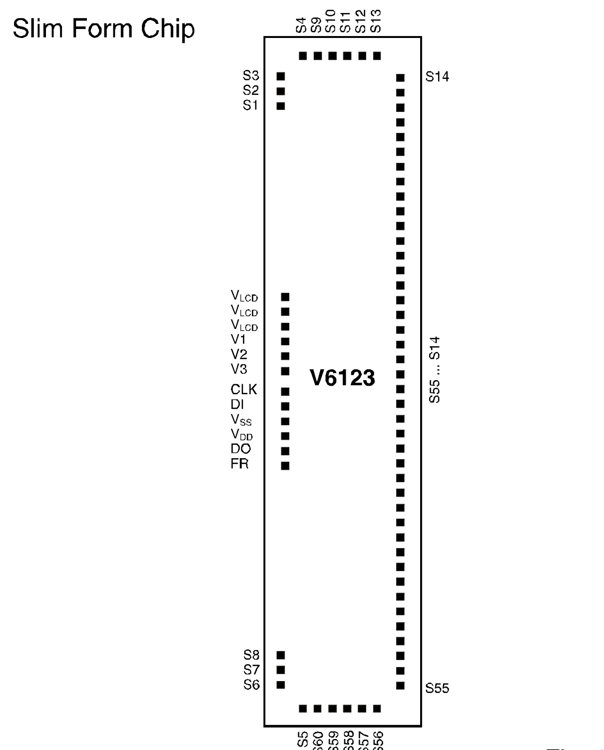


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	V_{DD}	-0.3 V to 9 V
LCD supply voltage range	V_{LCD}	-0.3 V to 10 V
Voltage at DI, DO, CLK, FR	V_{LOGIC}	-0.3 V to V_{DD} +0.3 V
Voltage at V1 to V3, S1 to S60	V_{DISP}	-0.3 V to V_{LCD} +0.3 V
Storage temperature range	T_{STO}	-65 to +150 °C
PElectrostatic discharge max. to MIL-STD-883C method 3015	V_{Smax}	1000 V
Maximum soldering conditions	T_{Smax}	250 °C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	T_A	-40		+85	°C
Logic supply voltage	V_{DD}	2	5	6	V
LCD supply voltage	V_{LCD}	2	5	8.5	V

Table 2

Electrical Characteristics

V_{DD} = 5 V ± 10%, V_{LCD} = 2 to 8.5 V and T_A = -40 to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Dynamic supply current	I_{LCD}	See note 1)		175	250	µA
Dynamic supply current	I_{DD}	See note 1) at T_A = 25 °C		29	35	µA
Dynamic supply current	I_{DD}	See note 1)		29	50	µA
Dynamic supply current	I_{DD}	See note 2)		285	350	µA
Control Signals DI, CLK, FR						
Input leakage	I_{IN}	$0 < V_{IN} < V_{DD}$		1	100	nA
Input capacitance	C_{IN}	at T_A = 25 °C		8		pF
Low level input voltage	V_{IL}		0		0.8	V
High level input voltage	V_{IH}		2.0		V_{DD}	V
Data Output DO						
High level output voltage	V_{OH}	I_H = 2 mA	2.4			V
Low level output voltage	V_{OL}	I_L = 2 mA			0.4	V
Driver Outputs S1 … S60						
Driver impedance 4)	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 7 V		1	1.5	kΩ
Driver impedance 4)	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 3 V		2.6	3.5	kΩ
Driver impedance 4)	R_{OUT}	I_{OUT} = 10 µA, V_{LCD} = 2 V		7		kΩ
Bias impedance V1, V2, V3 5)	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 7 V		18	24	kΩ
Bias impedance V1, V2, V3 5)	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 3 V		20	27	kΩ
Bias impedance V1, V2, V3 5)	R_{BIAS}	I_{OUT} = 10 µA, V_{LCD} = 2 V		24		kΩ
DC output component	± VDC	see Tables 4a and 4b, V_{LCD} = 5 V		15	50	mV

Table 3

1) All outputs open, DI and CLK at V_{SS}, FR = 400 Hz, all other inputs at V_{DD}
2) All outputs open, DI at V_{SS}, FR = 400 Hz, f_{CLK} = 1 MHz
3) All outputs open, all inputs at V_{DD}
4) This is the impedance between of the voltage bias level pins (V1, V2 or V3) and the output pins S1 to S60 when a given voltage bias level is driving the outputs (S1 to S60)
5) This is the impedance seen at the segment pin. Outputs measured one at a time

Column Drivers

Outputs	FR Polarity	Column Data	Measured	Guaranteed
S1 to S60	logic 1	logic 1	$\mid Sx^* - V_{SS} \mid$	
S1 to S60	logic 0	logic 1	$\mid V_{LCD} - Sx^* \mid$	$\mid V_{LCD} - Sx^* \mid = \mid Sx^* - V_{SS} \mid \pm 25$ mV
S1 to S60	logic 1	logic 0	$\mid V_{LCD} - Sx^* \mid$	
S1 to S60	logic 0	logic 0	$\mid Sx^* - V_{SS} \mid$	$\mid V_{LCD} - Sx^* \mid = \mid Sx^* - V_{SS} \mid \pm 25$ mV

*Sx = the output number (I.e. S1 to S60)

Table 4a

Row Drivers

Outputs	FR Polarity	Row Data	Measured	Guaranteed
S1 to Sn*	logic 1	logic 1	$\mid V_{LCD} - Sx \mid$	
S1 to Sn*	logic 0	logic 1	$\mid Sx - V_{ss} \mid$	$\mid V_{LCD} - Sx \mid = \mid Sx - V_{SS} \mid \pm 25$ mV
S1 to Sn*	logic 1	logic 0	$\mid Sx - V_{SS} \mid$	
S1 to Sn*	logic 0	logic 0	$\mid V_{LCD} - Sx \mid$	$\mid V_{LCD} - Sx \mid = \mid Sx - V_{SS} \mid \pm 25$ mV

*n= the V6123 mux programme number (i.e. 2, 4 or 8)

Table 4b

Timing Characteristics

V_{DD} = 5 V ± 10%, V_{LCD} = 2 to 8.5 V, and T_A = -40 °C to +85 °C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		120			ns
Clock low pulse width	t_{CL}		120		2000	ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20[1)]			ns
Data input hold time	t_{DH}		30[1)]			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF			200	ns
STR pulse width	t_{STR}		6		∞	µs
FR (internal frame frequency)	f_{FR}[2)]	T_A = 25 °C	45	55	65	Hz

1) $t_{DS} + t_{DH}$ minimum must be ≥ 100 ns. If t_{DS} = 20 ns then $t_{DH} \geq$ 80 ns.

Table 5a

2) V6123 n, FR = n times the desired LCD refresh rate where n is the V6123 mux mode number.
See fig. 14, 15 for more details concerning frame frequency.

V_{DD} = 2 to 6V, V_{LCD} = 2 to 8.5 V, and T_A = -40 °C to +85 °C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		0.5			µs
Clock low pulse width	t_{CL}		0.5		1.5	µs
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		100[1)]			NS
Data input hold time	t_{DH}		150[1)]			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF			500	ns
STR pulse width	t_{STR}		16		∞	µs

1) $t_{DS} + t_{DH}$ minimum must be ≥ 500 ns. If t_{DS} = 100 ns then $t_{DH} \geq$ 400 ns.

Table 5b

Timing Waveforms

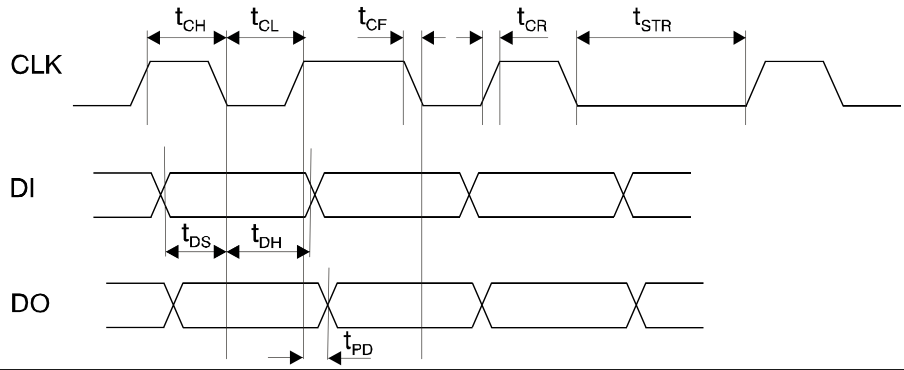


Fig. 3

Clock Definition

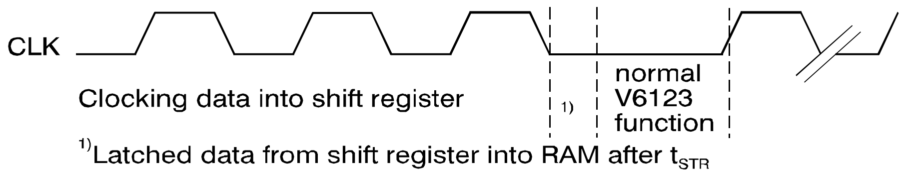
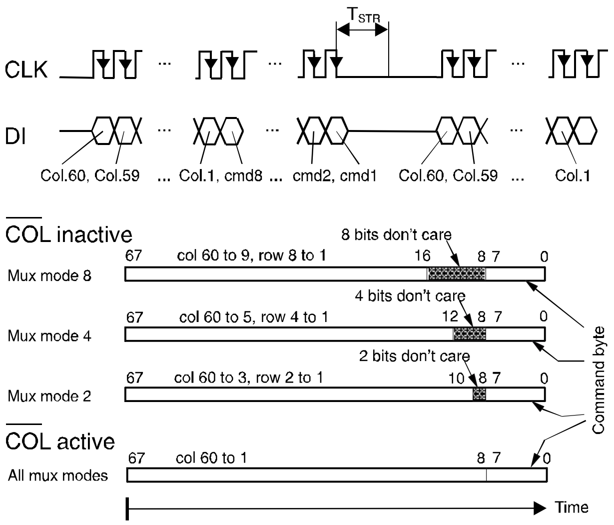


Fig. 4

Programmation Data Bits and Data Transfer Cycle

Command Bits 0 to 7							
0	1	2	3	4	5	6	7
Multiplex Ratio		$\overline{COL}$	RAM Address			Blank	SET

Bit2: $\overline{COL}$ bit configure the V6123 function as row and column driver or column driver only.
Bit 6: Blank bit forces all column outputs OFF.
Bit 7: SET bit forces all column outputs ON.
Note: **If bit 6 and 7 are both to 1L the chip is synchronized to row 1**.



Mux Ratio (bit 0, 1)		
0	1	Mux Mode
0	0	2
0	1	4
1	0	-
1	1	8

V6123 as a row and column driver, 68 bit load cycle, RAM address arising from command bits 3 to 5

Display RAM Address

Command Bits 3 to 5			LCD Row
Mux prog. 2	**Mux prog. 4**	**Mux prog. 8**	
000	000	000	Row 1
001	001	001	Row 2
	010	010	Row 3
	011	011	Row 4
		100	Row 5
		101	Row 6
		110	Row 7
		111	Row 8

All mux mode programmation or $\overline{COL}$ states need 68 bit load cycles.

Fig. 5

Block Diagram

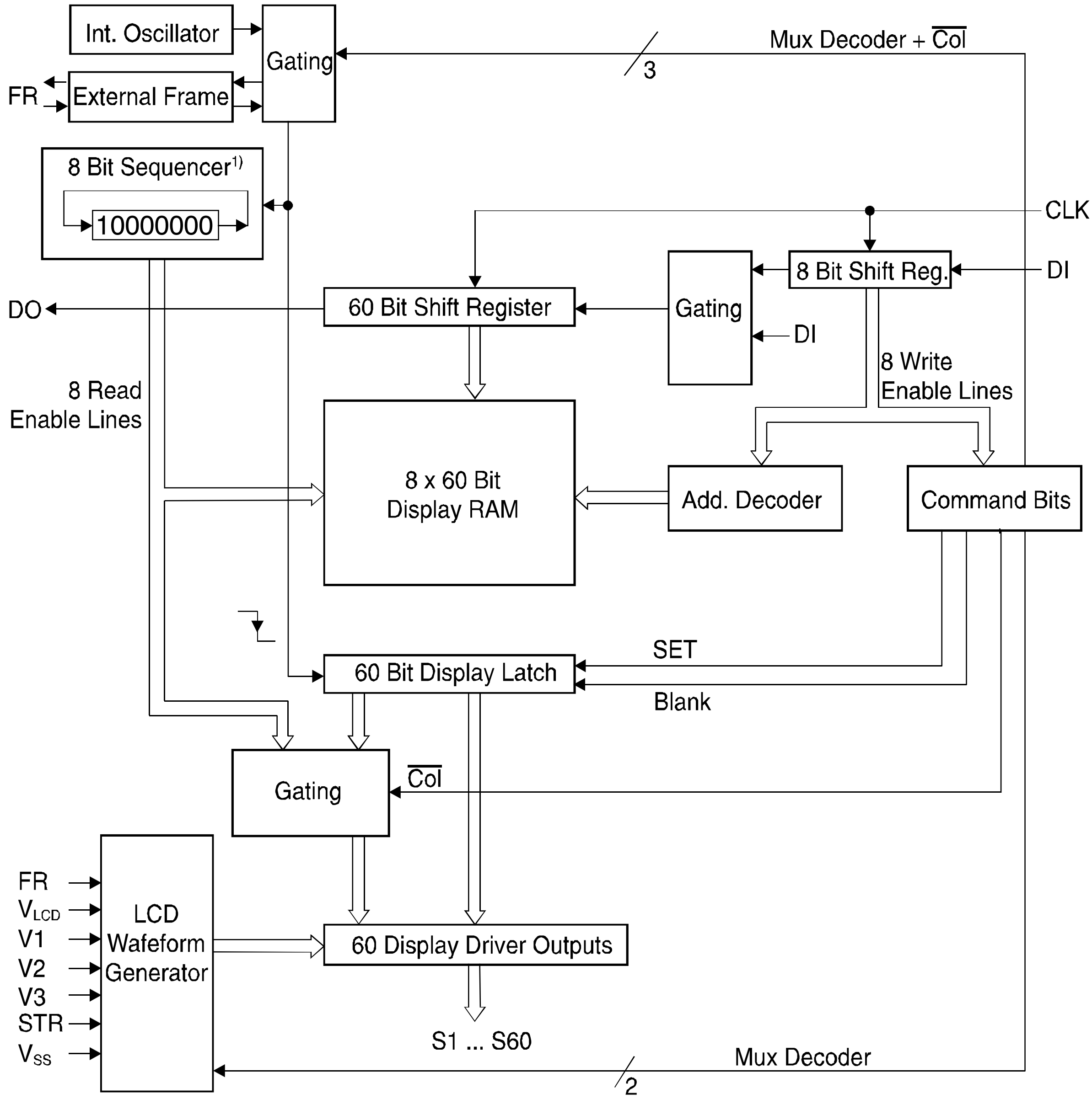


Fig. 6

Pin Assignment

Name	Function
S1 ... S60	LCD outputs, see Table 7
V3	LCD voltage bias level 3 [1][2]
V2	LCD voltage bias level 2 [1]
V1	LCD voltage bias level 1 [1]
V_{LCD}	Power supply for the LCD
FR	AC I/O signal for LCD driver output
DI	Serial data input
DO	Serial data output
CLK	Data clock input
V_{DD}	Power supply for logic
V_{SS}	Supply GND

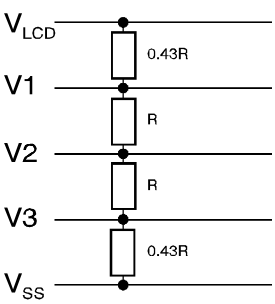
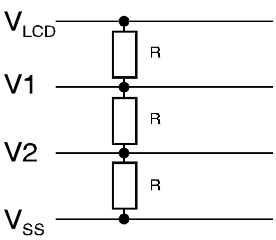
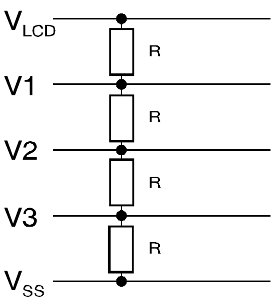
Table 6

[1] The V6123 has internal voltage bias level generation. When driving large pixels, an external resistor divider chain can be connnected to the voltage bias level inputs to obtain enhanced display contrast. See Fig. 11, 12 and 13. The external resistor divider ratio should be in accordance with the internal resistor ratio (see Table 8).
[2] V3 is connected internally to V_{SS} on the V6123 mux mode 4.

Name	$\overline{COL}$ inactive			$\overline{COL}$ active
	V6123 (2)	V6123 (4)	V6123 (8)	
S1	Row1	Row1	Row1	Col1
S2	Row2	Row2	Row2	Col2
S3	Col1	Row3	Row3	Col3
S4	Col2	Row4	Row4	Col4
S5	Col3	Col1	Row5	Col5
S6	Col4	Col2	Row6	Col6
S7	Col5	Col3	Row7	Col7
S8	Col6	Col4	Row8	Col8
S9...S60	Col7...58	Col5...56	Col1...52	Col9...60

Table 7

LCD Voltage Bias Levels

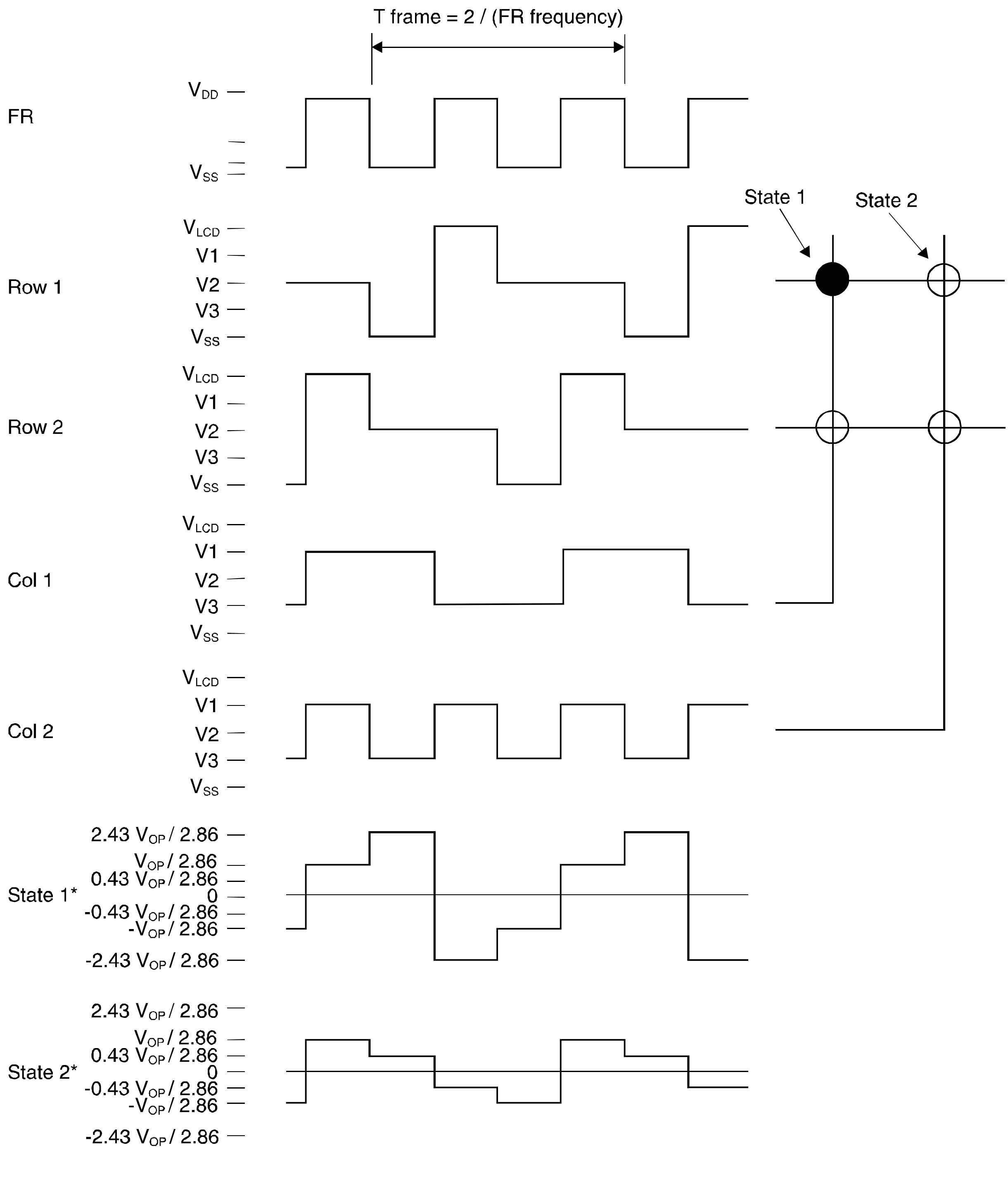
	LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}{}^{3)}}{V_{OFF}\text{ (rms)}}$	$\frac{V_{ON}\text{ (rms)}}{V_{OFF}\text{ (rms)}}$
	V6123 (2) n=2 1:2 MUX	5 Levels	$\sqrt{\frac{2n}{1-\sqrt{\frac{1}{n}}}} = 3.69$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 2.41$
	V6123 (4) n=4 1:4 MUX	1/3 Bias 4 Levels	3	$\sqrt{1+\frac{8}{n}} = 1.73$
	V6123 (8) n=8 1:8 MUX	1/4 Bias 5 Levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n+15}{n+3}} = 1.446$

[3] $V_{OP} = V_{LCD} - V_{SS}$

Table 8

Row and Column Multiplexing Waveform V6123 (2)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

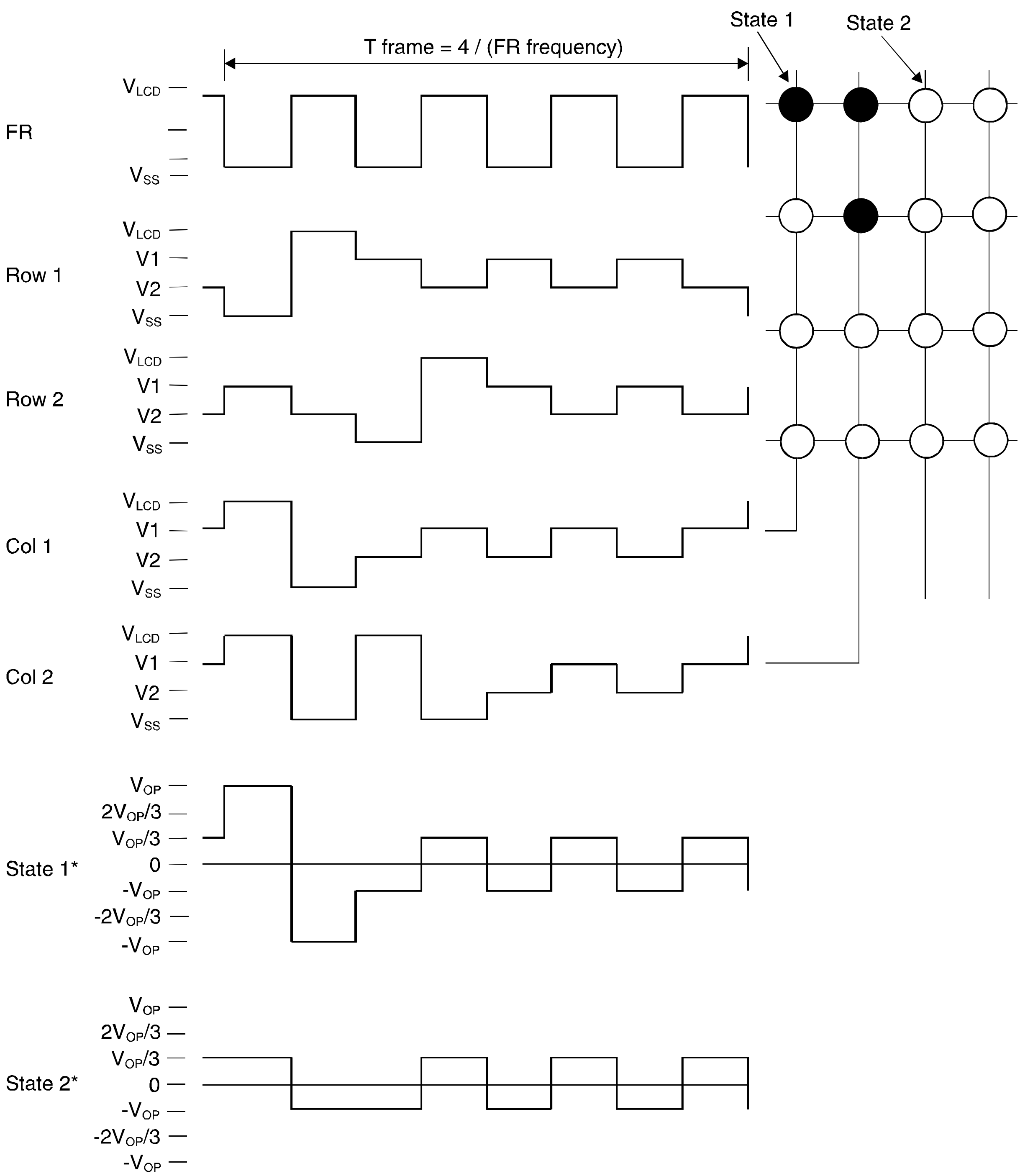


* See table 8

Fig. 7

Row and Column Multiplexing Waveform V6123 (4)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

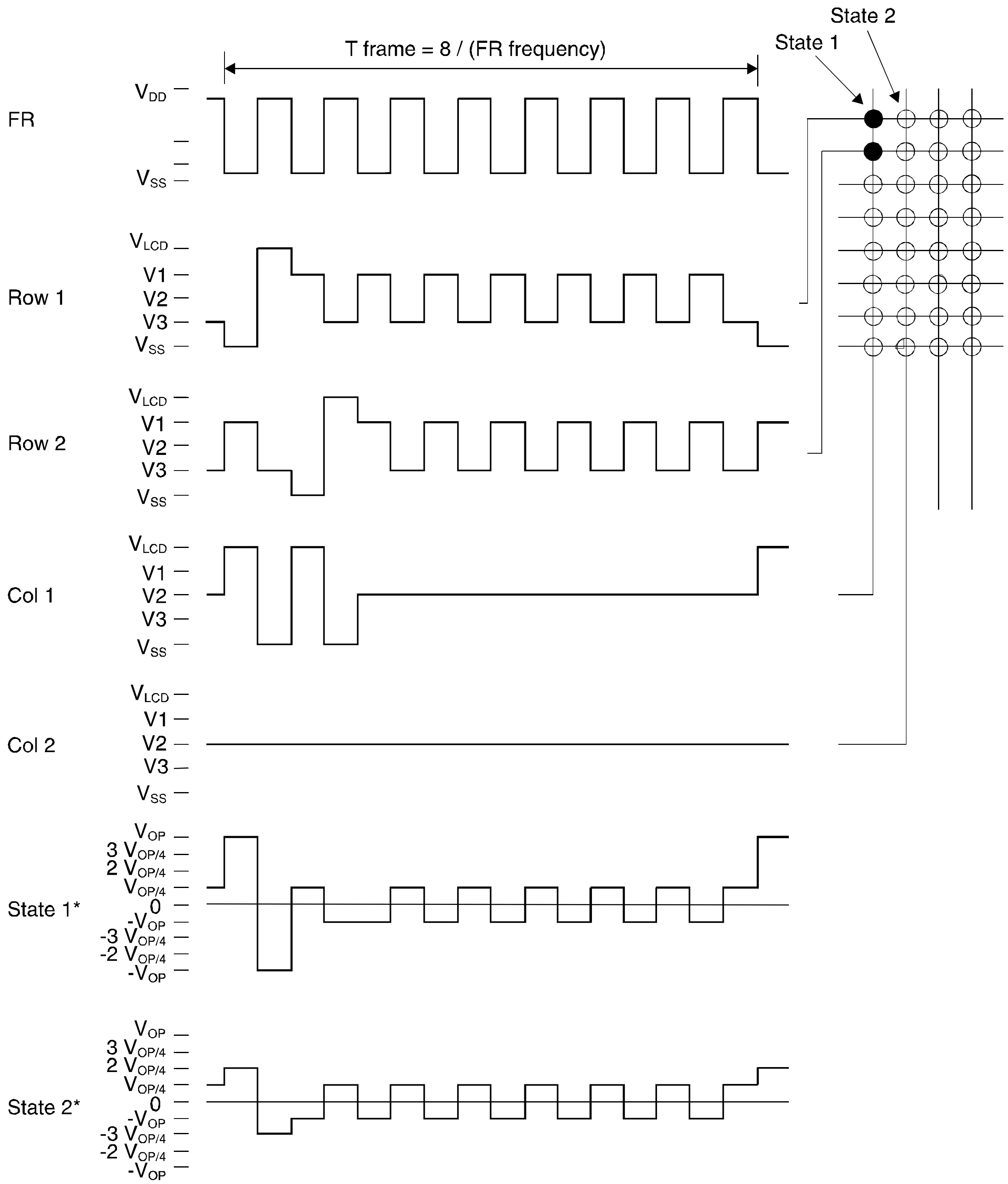


* See table 8

Fig. 8

Row and Column Multiplexing Waveform V6123 (8)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$



* See table 8

Fig. 9

Functional Description

Supply Voltage V_{LCD}, V_{DD}, V_{SS}

The voltage between V_{DD} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{LCD} and V_{SS} is the supply voltage for the LCD and is used for the generation of the internal LCD bias level which have a maximum impedance of 30 kΩ for a voltage from 3 to 8.5 V. Without external connections to the V1, V2, V3 bias level inputs, the V6123 can drive most medium sized LCD (pixel aera up to 4'000 mm^2).

For displays with a wide variation in pixel sizes, the configuration shown in Fig. 12 can give enhanced contrast by giving faster pixel switching times. On changing the row polarity (see Fig. 7, 8 and 9) the parallel capacitors lower the impedance of the bias level generation to the peak current, giving faster pixel charge times and thus a higher RMS "on" value. A higher RMS "on" value can give better contrast. If for a given LCD size and operating voltage, the "off" pixels appear "on", or there is poor contrast, then an external bias level generation circuit can be used with the V6123. An external bias generation circuit can lower the bias level impedance and hence improve the LCD contrast (see Fig. 11). The optimum values of R, Rx and C, vary according to the LCD size used and V_{LCD}. They are best determined through actual experimentation with the LCD.

For LCD with very large average pixel area (eg. up to 10'000 mm^2), the bias level configuration shown in Fig. 13 should be used.

When V6123 are cascaded, connect the V1, V2 and V3 bias inputs as shown in Fig. 10. The pixel load is averaged across all the cascaded drivers. This will give enhanced display contrast as the effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V6123 are cascaded as shown in Fig. 10, then the maximum bias level impedance becomes 15 kΩ for a V_{LCD} voltage from 3 to 8.5 V.

Table 8 shows the relationship between V1, V2 and V3 for the multiplex rates 2, 4 and 8. Note that $V_{LCD} > V1 > V2 > V3$ for the V6123 2 and 8 mux programmed, and for the V6123 4 mux programmed, $V_{LCD} > V1 > V2$, and $V3 = V_{SS}$.

Data Input / Output

The data input pin, DI, is used to load serial data into the V6123. The serial data word length is 68 bits. Data is loaded in inverse numerical order, the data for bit 68 is loaded first, the data for bit 1 last. The column data bits are loaded first and then the command byte (see Fig. 5).

The data output pin, DO, is used in cascaded application (see Fig. 10). DO transfers the data to the next cascaded chip. The data at DO is equal to the data at DI delayed by 68 clock periods. In order to cascade V6123s, the DO of one chip must be connected to DI of the following chip (see Fig. 10).

In cascaded applications the data for the last V6123 (the one that does not have DO connected) must be loaded first and the data for the first V6123 (it is DI connected to the processor) loaded last.

The display RAM word length is 60 bits (see Fig. 6). Each LCD row has a corresponding display RAM address which provides the column data (on or off) when the row is selected (on). When down loading data to the V6123, any display RAM address can be chosen. Display RAM address is given by command bits 3 to 5. Bit 6 forces all column outputs at 0L (display OFF). Bit 7 forces all column outputs at 1L (display ON). If bit 7 (SET) and bit 6 (BLANK) are both active, the initialization function is activated. This function is used to synchronize the chip at row one. The command bit 2 ($\overline{COL}$) defines the V6123 as a row and column driver or column driver only. The V6123 functions as row and column driver while the bit 2 ($\overline{COL}$) is inactive. When active, the bit 2 configures the V6123 to function as column driver only. The former row outputs function as column outputs. In cascaded applications, one V6123 should be used in the row and column configuration ($\overline{COL}$ inactive) and the rest as pure column drivers ($\overline{COL}$ active) (see Fig. 10). Note when cascading V6123s never cascade one mux mode number with another. If a V6123 8 mux programmed is used to drive the rows, then only V6123 8 mux programmed can be cascaded with it.

The command bits, bit 1 and bit 0, define the mux mode (see Fig. 5).

CLK Input

The clock input is used to clock the DI serial data into the shift register, to latch the data from the shift register into the RAM .

After loading data into the shift register, the clock has to stay 0 logic during T_{STR}.

After T_{STR} pulse, the data are latched into the RAM.

FR Input / Output

The frame frequency is realized by an internal RC oscillator with a typical value of 55 Hz. The internal row frequency changes with the number of rows (F_{row} = 55 x n, where n = 2, 4 or 8).

When bit 2 ($\overline{COL}$) is inactive (row and column driver), the frame frequency is given by the internal oscillator. This frequency can also be used at FR output to drive casecaded V6123.

When bit 2 ($\overline{COL}$) is active (column driver only), the frame frequency is external then the frequency is given by the row and column driver directly to the FR input. In cascaded applications, the row and column driver (FR, output) give the frame frequency to all the cascaded chip (FR, input).

Driver Outputs S1 to S60

There are 60 LCD driver outputs on the V6123. When bit 2 ($\overline{COL}$) is inactive, the outputs S1 to Sn function as row drivers and the outputs S(n+1) to S60 function as column drivers. Where n is the V6123 mux mode number (2, 4 or 8).

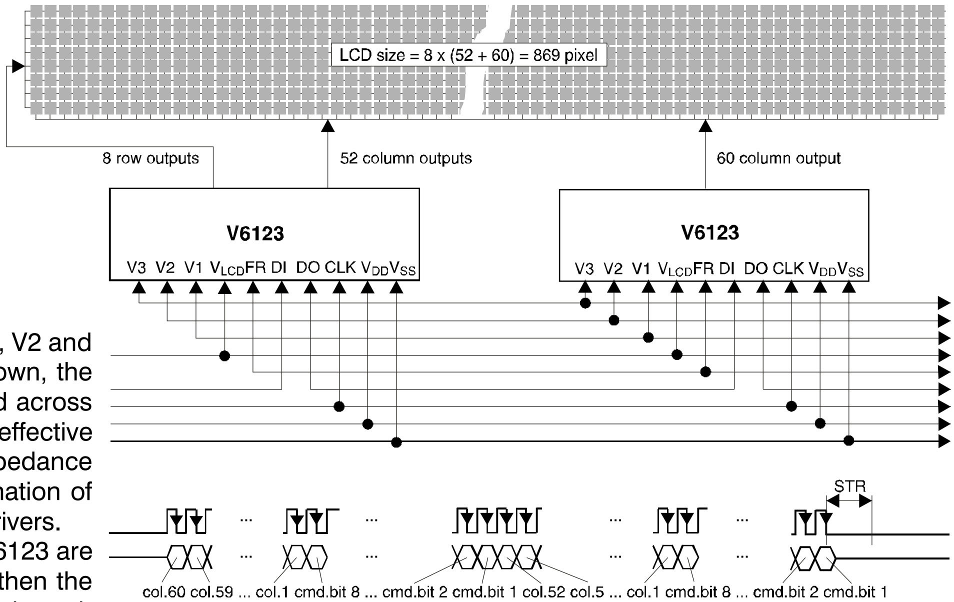
When bit 2 ($\overline{COL}$) is active, all 60 outputs function as column drivers (see Table 6). There is a one to one relationship between the display RAM and the LCD driver outputs. Each pixel (segment) driven by the V6123 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the segment "on" and clearing it turns it "off".

Power-Up

On power up the data in the shift registers, the display RAM, the sequencer driving the 2/4/8 rows and the 60 bit display latches are undefined.

Applications

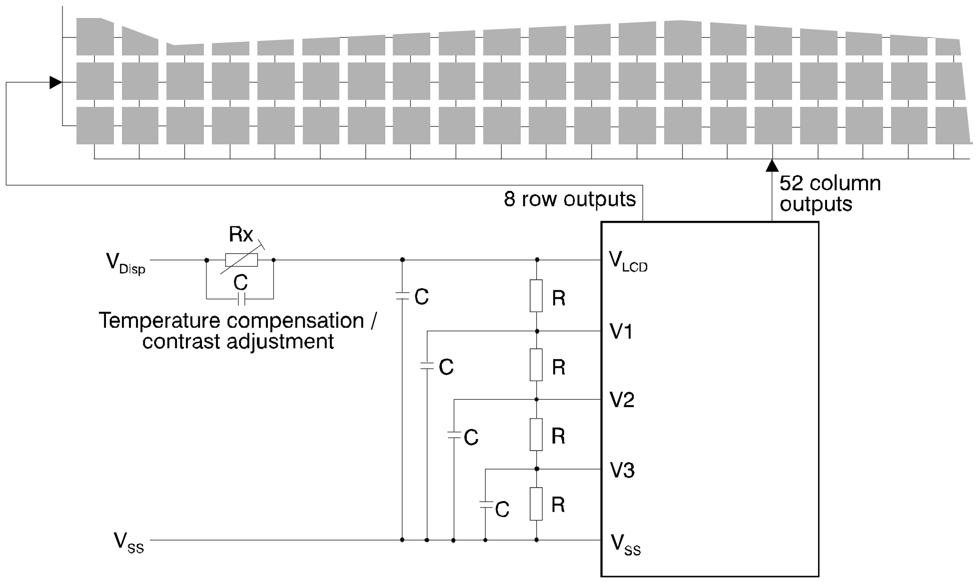
Two V6123 8 Mux Programmed Cascaded



By connecting the V1, V2 and V3 bias inputs as shown, the pixel load is averaged across all the drivers. The effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V6123 are cascaded as above, then the maximum bias level impedance becomes 15 kΩ.

Fig. 10

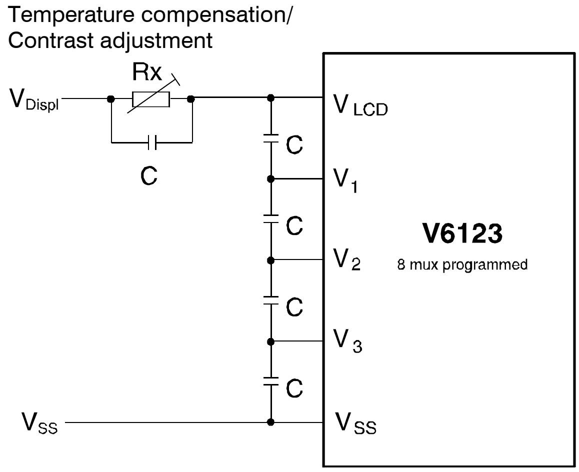
V6123 8 Mux Programmed with External Resistor Divider Bias Generation



Example set values:
R = 3.3 - 10 kΩ
C = 2.2 - 47 nF
Rx is given by the formula:
$Rx = 4R ((V_{DISP}/V_{LCD})-1) = 10 - 30\ k\Omega$

Fig. 11

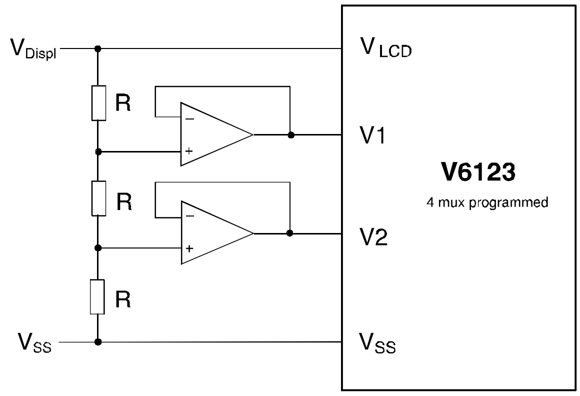
Enhanced Switching from the V6123



C = 1 μF
Rx is given by the formula:
$Rx = 4(24\ k\Omega)\left((V_{DISP}/V_{LCD}) - 1\right)$

Fig. 12

Bias Configuration for Large LCD



Large LCD example:
V_{OP} = 5 V, average pixel active area = up to 10'000 mm², displasy refresh rate = 55 Hz

For a single V6123 4 mux programmed driving such an LCD, the voltage follower buffer (opamp) requirement is:
peak current 1.8 mA
steady state current typically 150 μA

Fig. 13

Frame Frequency vs. Temperature at V_{DD} = 4.5 V

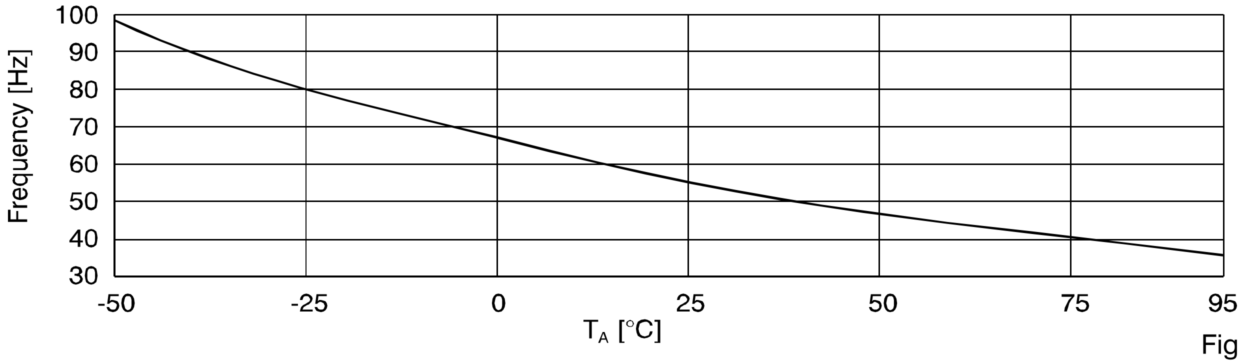


Fig. 14

Frame Frequency vs. V_{DD} at T_A = 25°C

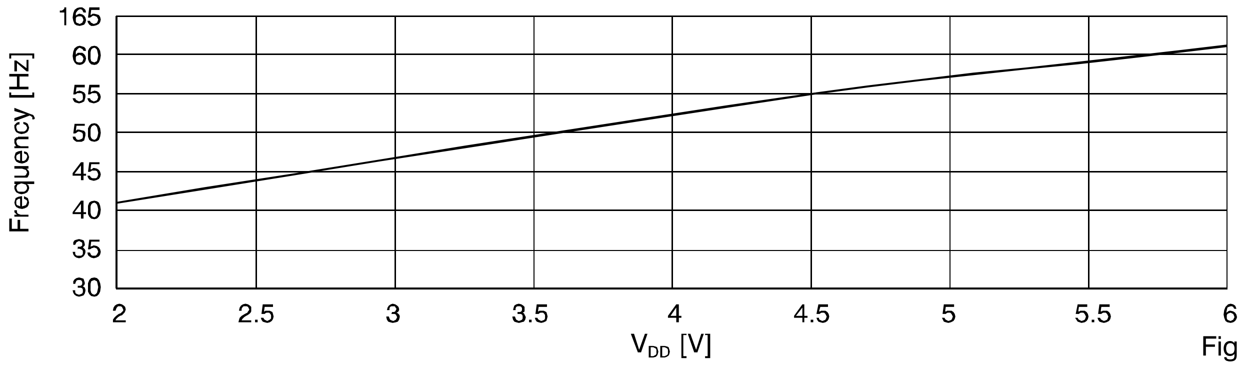


Fig. 15

Application Example

This table shows how to use the V6123 with a given initialization for **Chip-on-Glas**. Rows “Data” show the logical value to affect pad DI for each falling edge of pad CLK. After loading data into the shift register, the clock has to stay logic 0 during t_{STR}. After the t_{STR} pulse the data are latched into the RAM.

Display Data	8 Bits “don’t care”

Write Row 1 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	1	1	0	0	0	1	0	1	1	1	0	1	1	1	0			0	0	1	0	1	X	X	X	X	X	X	X	X

Command Byte								
7	6	5	4	3	2	1	0	
0	0	0	0	0	1	1	1	← Last send

Description:

Bit 7,6 = 0,0:	no set, no blank
Bit 3 to 5 = 0,0,0:	data sent to row 1 of the RAM
Bit 2 = 1:	row and column driver configuration
Bit 0,1 = 1,1:	mux 8

Result:

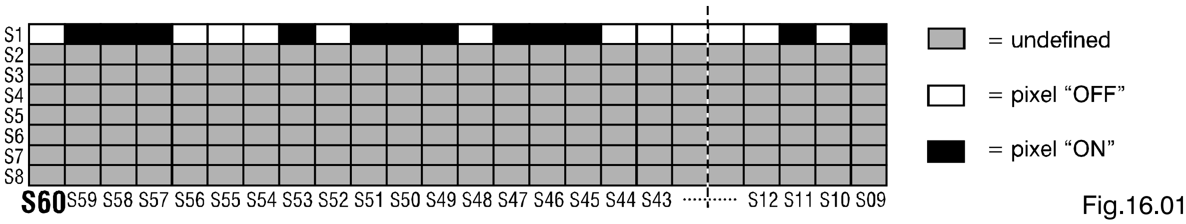


Fig.16.01

Write Row 2 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	0	0	0	1	1	0	0	0	1	0	0	0	1	0			0	0	1	0	1	X	X	X	X	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	1	0	0	1	1	1

Description:

Bit 7,6 = 0,0:	no set, no blank
Bit 3 to 5 = 0,0,1:	data sent to row 2 of the RAM
Bit 2 = 1:	row and column driver configuration
Bit 0,1 = 1,1:	mux 8

Result:

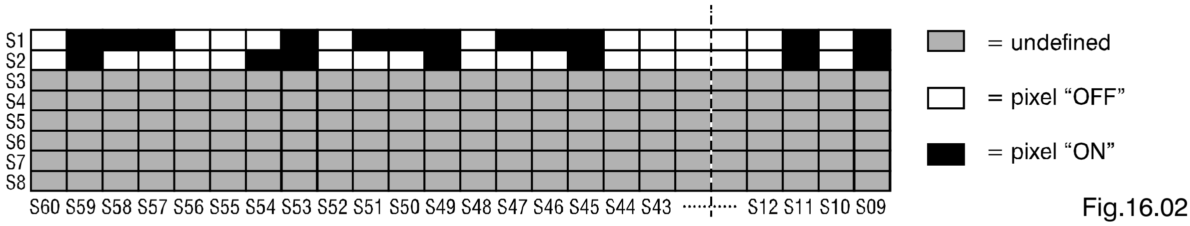


Fig.16.02

Write Row 3 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0			0	0	1	0	1	X	X	X	X	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	1

Description:

Bit 7,6 = 0,0:	no set, no blank
Bit 3 to 5 = 0,1,0:	data sent to row 3 of the RAM
Bit 2 = 1:	row and column driver configuration
Bit 0,1 = 1,1:	mux 8

Result:

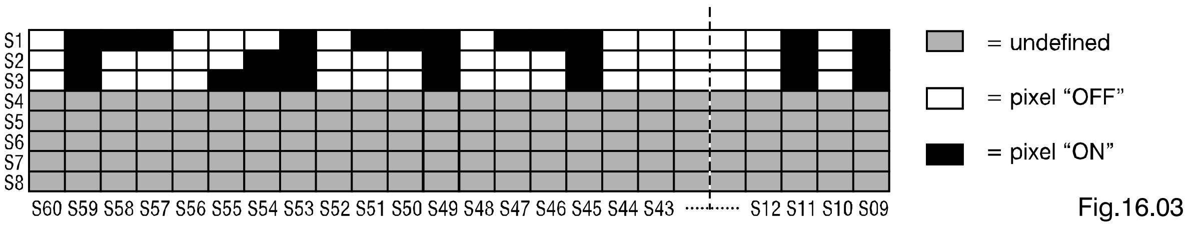


Fig.16.03

Table 9 (continued on following pages)

Table 9 continued

	Display Data	8 Bits "don't care"

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1	0			0	0	1	0	1	X	X	X	X	X	X	X	X

Command Byte

7	6	5	4	3	2	1	0
0	0	1	1	0	1	1	1

Description

Bit 7,6 = 0,0:	no set, no blank
Bit 3 to 5 = 0,1,1:	data sent to row 4 of the RAM
Bit 2 = 1:	row and column driver configuration
Bit 0,1 = 1,1:	mux 8

Result

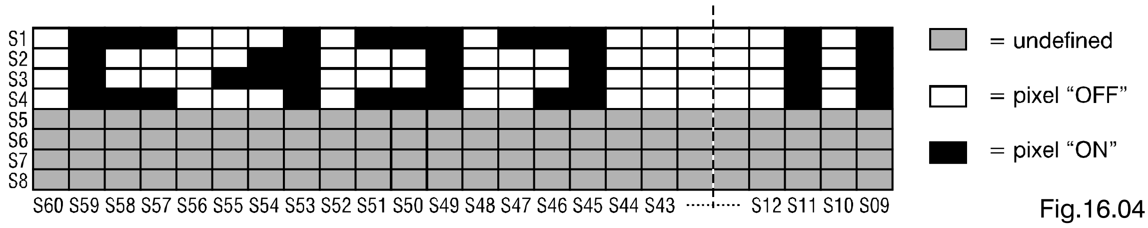


Fig.16.04

Write Row 4 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0			0	0	1	0	1	X	X	X	X	X	X	X	X

Command Byte

7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1

Description

Bit 7,6 = 0,0:	no set, no blank
Bit 3 to 5 =1,0,0:	data sent to row 5 of the RAM
Bit 2 = 1:	row and column driver configuration
Bit 0,1 = 1,1:	mux 8

Result

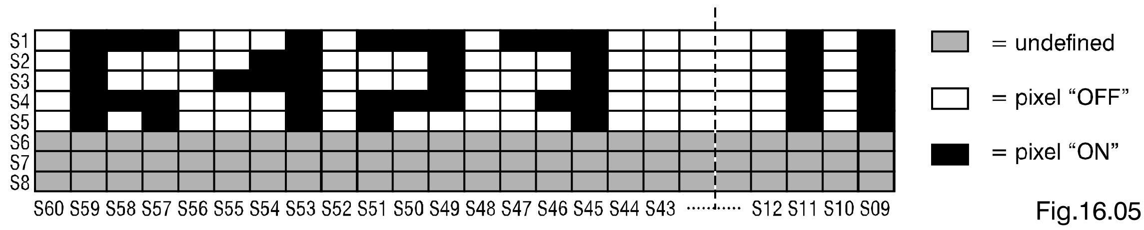


Fig.16.05

Write Row 5 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0			0	0	1	0	1	X	X	X	X	X	X	X	X

Command Byte

7	6	5	4	3	2	1	0
0	0	1	0	1	1	1	1

Description

Bit 7,6 = 0,0:	no set, no blank
Bit 3 to 5 = 1,0,1:	data sent to row 6 of the RAM
Bit 2 = 1:	row and column driver configuration
Bit 0,1 = 1,1:	mux 8

Result

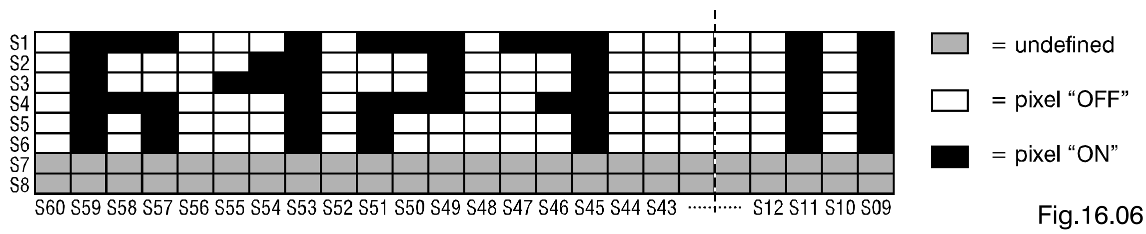


Fig.16.06

Write Row 6 Mux 8

Table 9 (continued on next pages)

Table 9 continued

Write Row 7 Mux 8

	Display Data																								8 Bits "don't care"							
Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	1	1	0	0	0	1	0	1	1	1	0	1	1	1	0			0	0	0	1	0	X	X	X	X	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1

Description:

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 1,1,0: data sent to row 7 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 1,1: mux 8

Result:

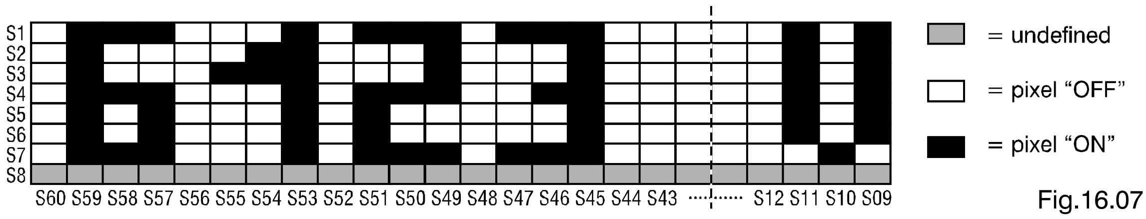


Fig.16.07

Write Row 8 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	X	X	X	X	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1

Description:

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 1,1,1: data sent to row 8 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 1,1: mux 8

Result:

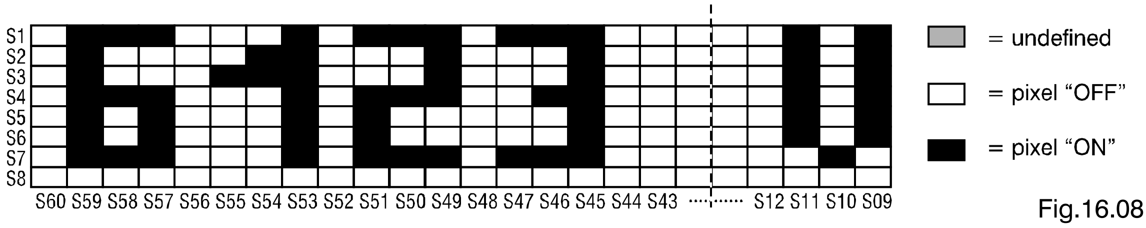


Fig.16.08

Command Byte only: Set

	Command Byte							
Bit No	7	6	5	4	3	2	1	0
DATA	1	0	1	1	1	1	1	1

Description:

Bit 7,6 = 1,0: SET, no blank
Bit 3 to 5 = 1,1,1: **data sent to row 8 of the RAM**
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 1,1: mux 8

Result:

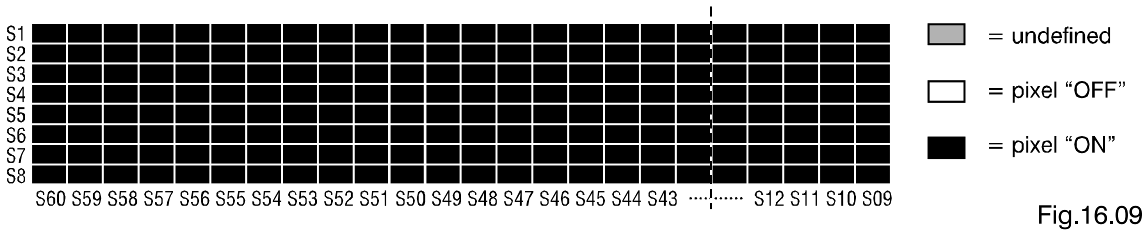


Fig.16.09

Table 9 (continued on next pages)

Table 9 continued

Display Data	8 Bits "don't care"

Command Byte only: Blank

Bit No	7	6	5	4	3	2	1	0
Data	0	1	1	1	1	1	1	1

Description:

Bit 7,6 = 0,1: no set, BLANK
Bit 3 to 5 = 1,1,1: **data sent to row 8 of the RAM**
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 1,1: mux 8

Result:

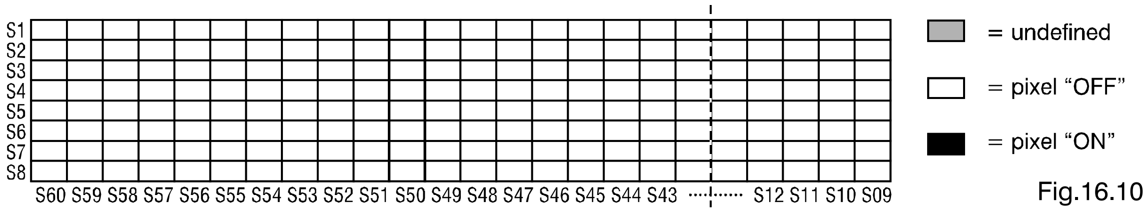


Fig.16.10

Command Byte only: Syncro

Bit No	7	6	5	4	3	2	1	0
Data	1	1	0	0	0	1	1	1

Description:

Bit 7,6 = 1,1: no set, no blank ⇒ **Synchronize the chip at row 1**
Bit 3 to 5 = 0,0,0: **data sent to row 8 of the RAM, you have to rewrite row 8 of the RAM**
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 1,1: mux 8

Result:

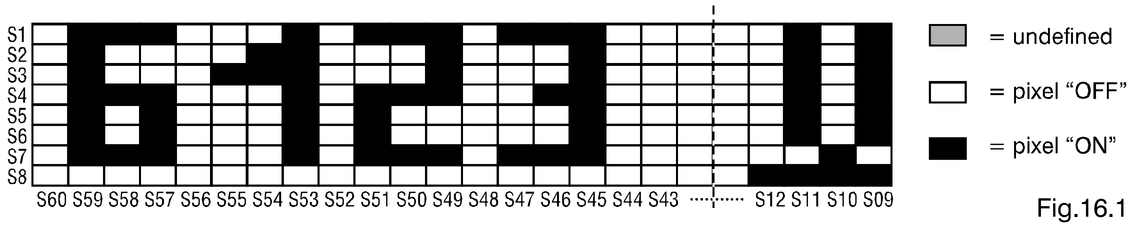


Fig.16.11

Syncro Rewrite Row 8 Mux 8

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	X	X	X	X	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

Description:

Bit 7,6 = 1,1: no set, no blank ⇒ **Synchronize the chip at row 1**
Bit 3 to 5 = 1,1,1: data sent to row 3 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 1,1: mux 8

Result:

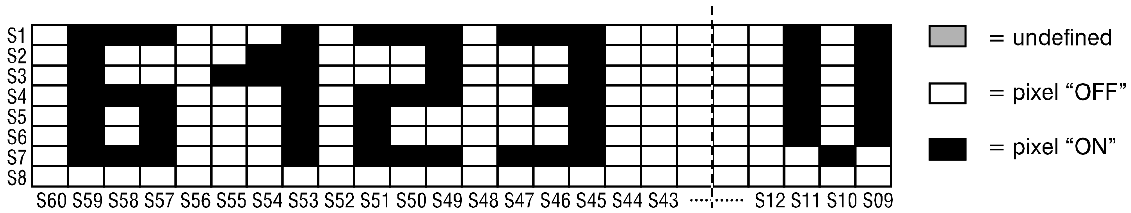


Fig.16.12

Table 9 (continued on next pages)

Table 9 continued

Display Data	8 Bits "don't care"

Write Row 1 Mux 4

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0			1	0	1	0	1	0	1	0	1	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0

Description

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 0,0,0: data sent to row 1 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 0,1: mux 4

Result

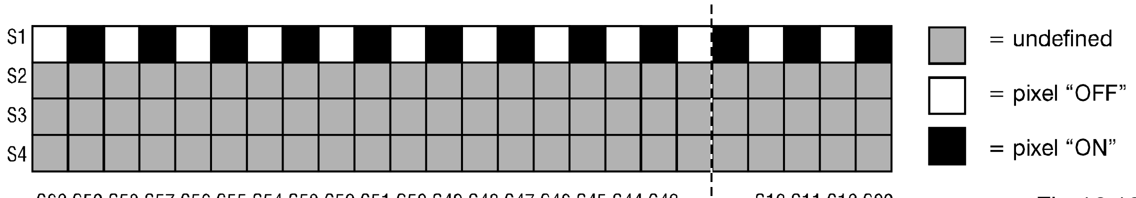


Fig.16.13

Write Row 2 Mux 4

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			0	1	0	1	0	1	0	1	0	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	0

Description

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 0,0,1: data sent to row 2 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 0,1: mux 4

Result

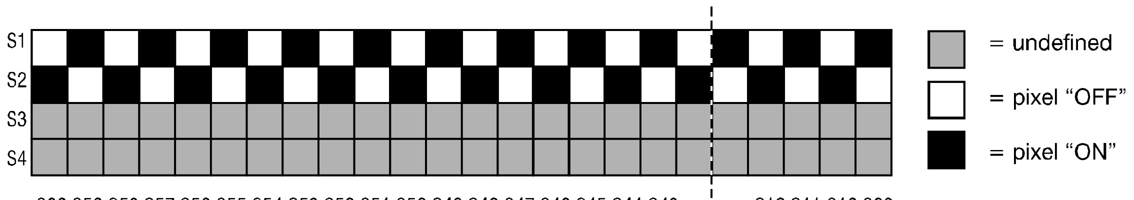


Fig.16.14

Write Row 3 Mux 4

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			0	1	0	1	0	1	0	1	0	X	X	X	X

Command Byte							
7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	0

Description

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 0,1,0: data sent to row 3 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 0,1: mux 4

Result

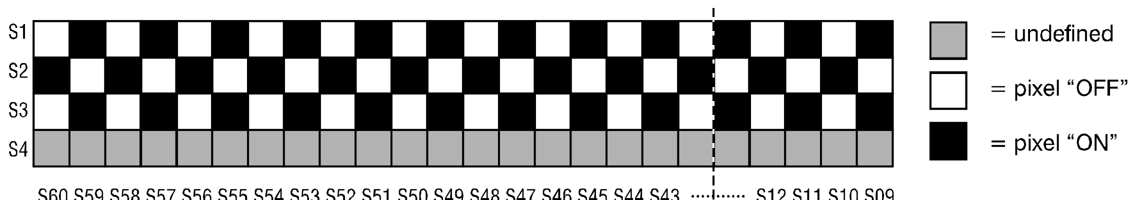


Fig.16.15

Table 9 (continued on next page)

Table 9 continued

	Display Data	8 Bits "don't care"

Write Row 4 Mux 4

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			0	1	0	1	0	1	0	1	0	X	X	X	X

Command Byte

7	6	5	4	3	2	1	0
0	0	1	1	0	1	1	0

Description

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 0,1,1: data sent to row 4 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 0,1: mux 4

Result

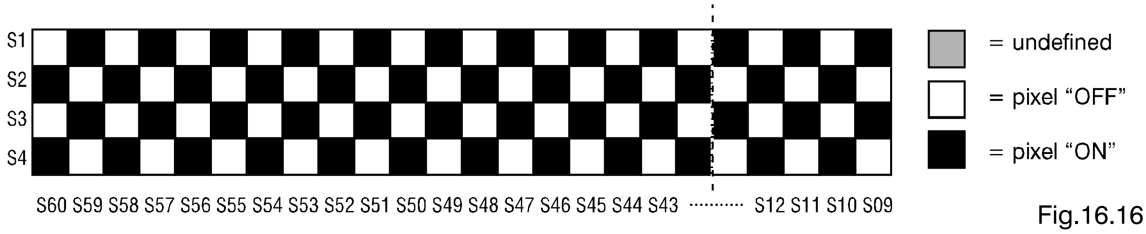


Fig.16.16

Write Row 1 Mux 2

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0			1	0	1	0	1	0	1	0	1	0	1	X	X

Command Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0

Description

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 0,0,0: data sent to row 1 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 0,0: mux 2

Result

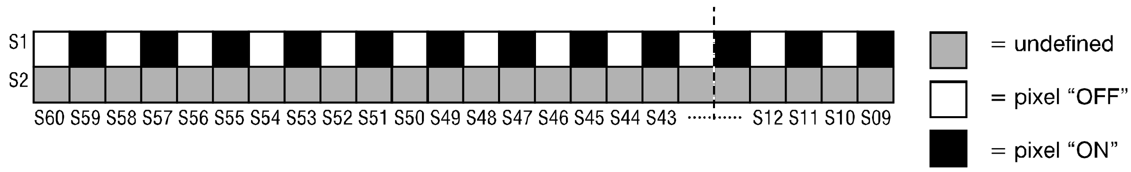


Fig.16.17

Write Row 2 Mux 2

Bit No	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	...	...	20	19	18	17	16	15	14	13	12	11	10	9	8
DATA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0			1	0	1	0	1	0	1	0	1	0	1	X	X

Command Byte

7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	0

Description

Bit 7,6 = 0,0: no set, no blank
Bit 3 to 5 = 0,0,1: data sent to row 2 of the RAM
Bit 2 = 1: row and column driver configuration
Bit 0,1 = 0,0: mux 2

Result

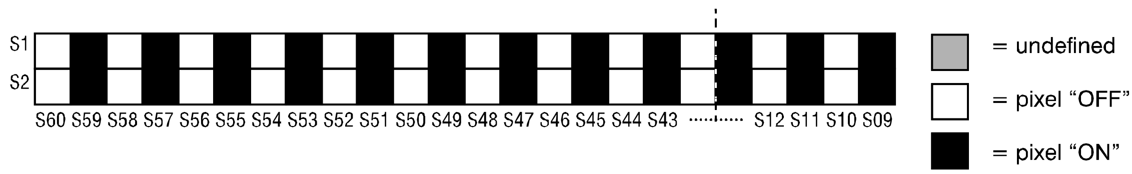
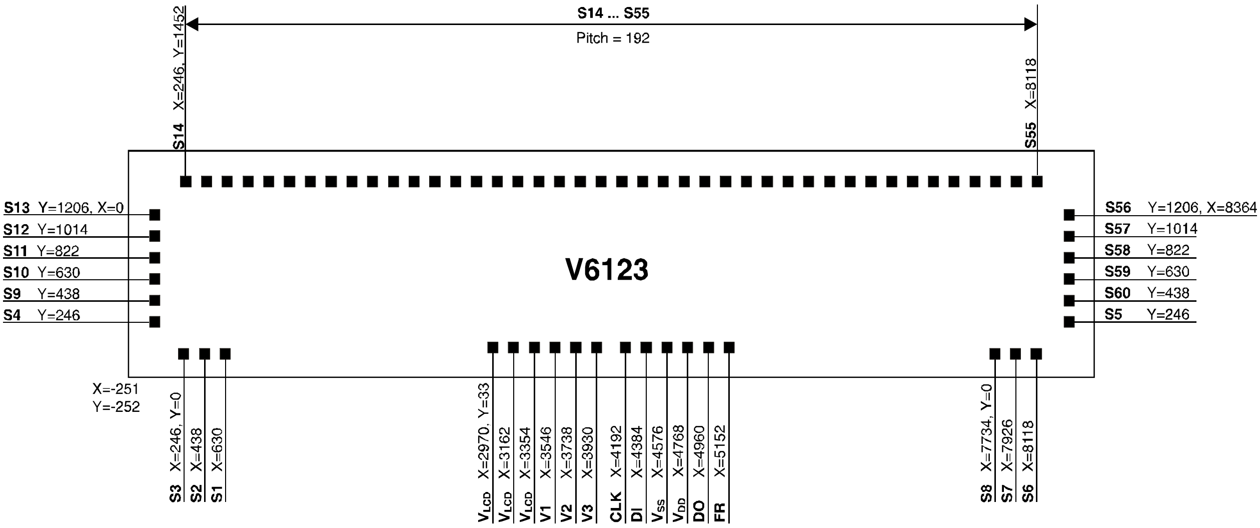


Fig.16.18

Table 9

Package and Ordering Information

Dimensions of Chip Form



All dimensions in µm

Thickness: 11 mils typ.
Bump size: Output pad = 110 x 110 micron, Input pad = 120 x 120 micron
Chip size: [X x Y] 8864 x 1981 micron or 349 x 78 mils
Note: The origin (0,0) is the lower left coordinate of center pads.
The lower left corner of the chip shows distances to origin.

Fig. 17

Ordering Information

The V6123 is available in the following packages:

Chip form	V6123 Chip
Bumped form	V6123 Bumped

When ordering please specify the complete part number and package.

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