M1010-01

VCSO Based Clock Jitter Attenuator

General Description

The M1010-01 is a VCSO (Voltage Controlled SAW Oscillator) based clock jitter attenuator PLL designed for clock jitter attenuation and frequency translation. The device is ideal for generating the transmit reference clock for OC-12 and OC-48 optical network systems supporting 622 - 2,488 MHz rates. It can serve to jitter attenuate a stratum reference clock or a recovered clock in loop timing mode. The M1010-01 module includes a proprietary SAW (surface acoustic wave) delay line as part of the VCSO. This results in a high frequency, high-Q, low phase noise oscillator that assures low intrinsic output jitter.

Features

- **Ideal for OC-12/48 data clock**
- **Integrated SAW delay line**
- **Output frequencies from 150 to 175 MHz (Specify VCSO output frequency at time of order)**
- **Low phase jitter of 0.5 ps rms, typical (12kHz to 20MHz)**
- **LVPECL clock output**
- **Pin-selectable feedback and reference divider ratios, no programming required**
- **Scalable dividers provide further adjustment of loop bandwidth as well as jitter tolerance**
- **Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

Pin Assignment (9 x 9 mm SMT)

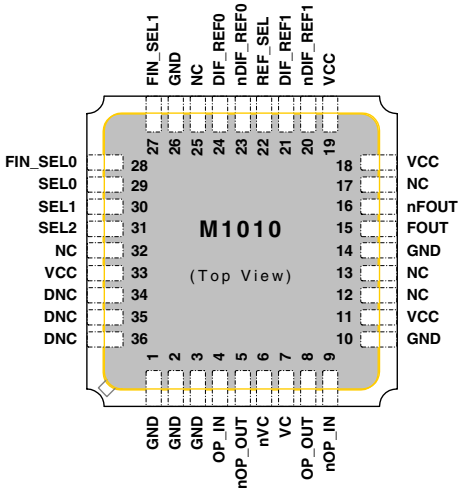

Figure 1: Pin Assignment

Example I/O Clock Frequency Combinations Using M1010-01-155.5200

Frequency Input (Mfin) Ratio	Input Reference Clock (MHz)	Output Clock MHz
8	19.44	155.52
2	77.76	
1	155.52	

Table 1: Example I/O Clock Frequency Combinations

Simplified Block Diagram

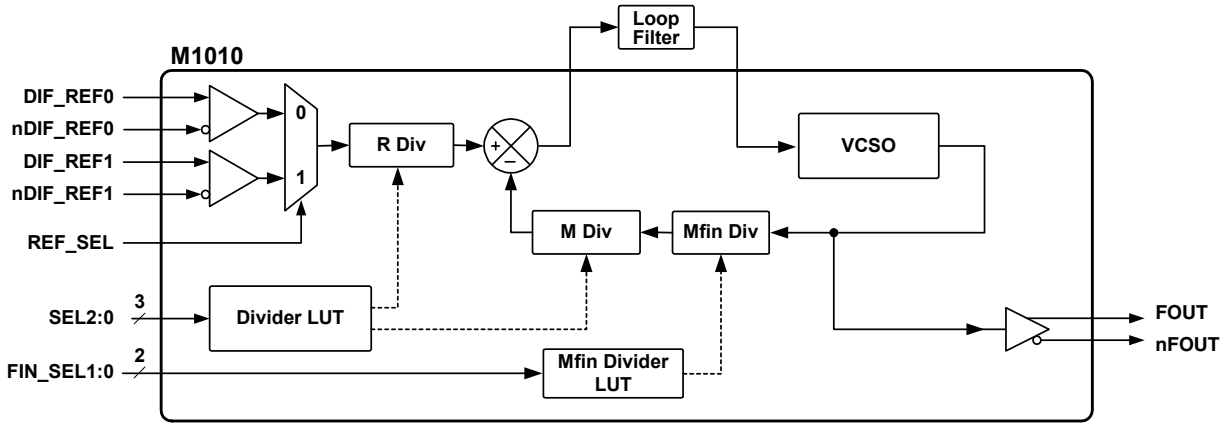

Figure 2: Simplified Block Diagram

DETAILED BLOCK DIAGRAM

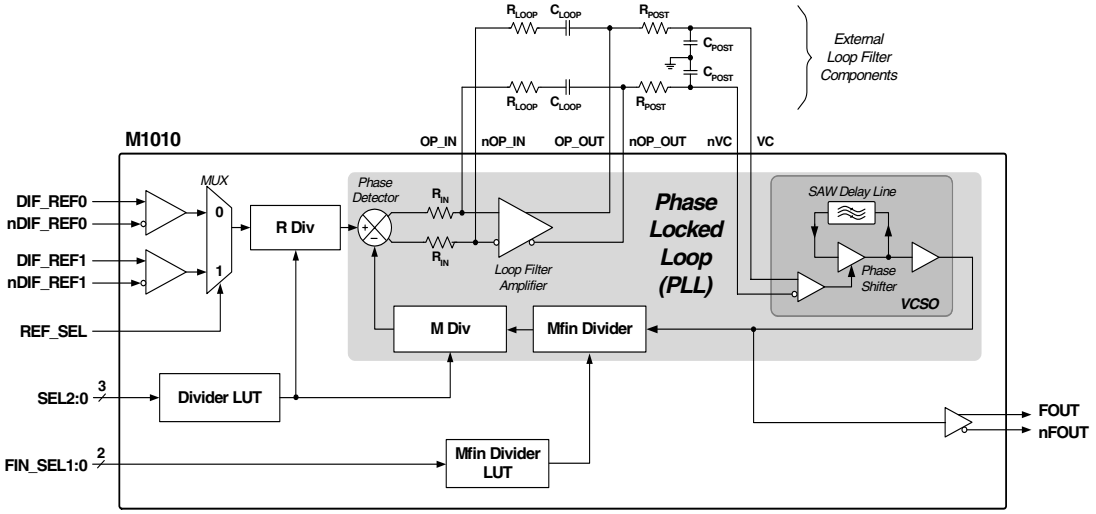

Figure 3: Detailed Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 4, External Loop Filter, on pg. 4.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 18, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12, 13, 17, 25, 32	NC			No internal connection.
15 16	FOUT nFOUT	Output	No internal terminator	Clock output pairs. Differential LVPECL.
20	nDIF_REF1	Input	Internal pull-UP resistor[1]	Reference clock input pair. Differential LVPECL or LVDS.
21	DIF_REF1		Internal pull-down resistor[1]	
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL: Logic 1 selects DIF_REF1, nDIF_REF1. Logic 0 selects DIF_REF0, nDIF_REF0.
23	nDIF_REF0	Input	Internal pull-UP resistor[1]	Reference clock input pair. Differential LVPECL or LVDS.
24	DIF_REF0		Internal pull-down resistor[1]	
27 28	FIN_SEL1 FIN_SEL0	Input	Internal pull-down resistor[1]	Input clock frequency selection. LVCMOS/LVTTL. See Table 3, Mfin (Frequency Input) Divider Look-Up Table (LUT) on pg. 3.
29 30 31	SEL0 SEL1 SEL2	Input	Internal pull-UP resistor[1]	M and R divider value selection. LVCMOS/ LVTTL. See Table 4, SEL2:0 Look-up Table (LUT) on pg. 3.
34, 35, 36	DNC		Do Not Connect.	

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see “Inputs with Pull-down” and “Inputs with Pull-up” in Table 8, DC Characteristics, on pg. 6.

PLL DIVIDER LOOK-UP TABLES

Mfin (Frequency Input) Divider Look-Up Table (LUT)

The FIN_SEL1:0 pins select the feedback divider value ("Mfin").

FIN_SEL1:0	Mfin Value	M1010-01-155.5200 Sample Ref. Freq. (MHz) [1]
0 0	8	19.44
0 1	2	77.76
1 0	1	155.52
1 1	x	Test mode. Do not use.

Table 3: Mfin (Frequency Input) Divider Look-Up Table (LUT)

Note 1: Example with M1010-01-155.5200.

SEL2:0 Look-up Table (LUT)

The SEL2:0 pins select the feedback and reference divider values M and R to enable adjustment of loop bandwidth and jitter tolerance.

SEL2:0	M	R	Description
0 0 0	236	236	Various divider values to adjust bandwidth and jitter tolerance
0 0 1	79	79	
0 1 0	14	14	
0 1 1	239	239	
1 0 0	1	1	
1 0 1	2	2	
1 1 0	4	4	
1 1 1	8	8	

Table 4: SEL2:0 Look-up Table (LUT)

FUNCTIONAL DESCRIPTION

The M1010-01 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW filter provides low jitter signal performance and controls the output frequency of the VCSO (Voltage Controlled SAW Oscillator).

A configurable frequency divider (labeled "Mfin Divider") provides the division options to accomodate various reference clock frequencies.

In addition, configurable feedback and reference dividers (the "M Divider" and "R Divider") provide divider value options to enable adjustment of loop bandwidth and jitter tolerance.

For example, the **M1010-01-155.5200** *(see "Ordering Information"* on pg. 8*)* has a 155.52MHz VCSO frequency:

The Mfin feedback divider allows an input frequency to be the VCSO output frequency divided by 1, 2, or 8. Therefore, for the base input frequency of 155.52MHz, the actual input reference clock frequencies can be: 155.52, 77.76, and 19.44MHz. (See Table 3 on pg. 3.)

The PLL

The PLL uses a phase detector and configurable dividers to synchronize the output of the VCSO with selected reference clock.

The "Mfin Divider" and "M Divider" divide the VCSO frequency, feeding the result into the phase detector.

The selected input reference clock is divided by the "R Divider". The result is fed into the other input of the phase detector.

The phase detector compares its two inputs. It then outputs pulses to the loop filter as needed to increase or decrease the VCSO frequency and thereby match and lock the divider output's frequency and phase to those of the input reference clock.

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

Relationship Among Frequencies and Dividers

The VCSO center frequency must be specified at time of order. The relationship between the VCSO (Fvcso) frequency, the Mfin divider, the M divider, the R divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times Mfin \times \frac{M}{R}$$

Clock Output

The M1010-01 provides one differential LVPECL output pair FOUT. PECL and LVDS product options are available; consult factory.

External Loop Filter

To provide stable PLL operation, the M1010-01 requires the use of an external loop filter. This is implemented by connecting passive external components to the device as shown in Figure 4 below.

The M1010-01 utilizes a differential analog signal path to minimize noise coupling from the system. Because of this, the loop filter implementation requires two identical complementary RC filters as shown here.

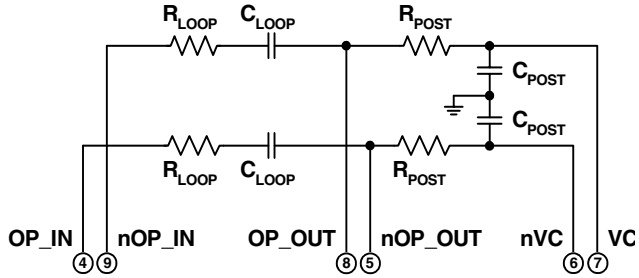

Figure 4: External Loop Filter

PLL bandwidth is affected by the "M" value and the "Mfin" value, as well as the VCSO frequency.

The various SEL1:0 settings can be used to actively change PLL loop bandwidth in a given application. See "SEL2:0 Look-up Table (LUT)" on pg. 3.

See Table 5, Example Loop Filter Component Values for M1010-01-155.5200, on pg. 4.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Example Loop Filter Component Values for M1010-01-155.5200[1]

VCSO Parameters: K_{VCO} = 200kHz/V, R_{IN} = 2050kΩ, VCSO Bandwidth = 700kHz.

Device Configuration				Example External Loop Filter Component Value				Nominal Performance Using These Values			
F_{Ref} (MHz)	**F_{VCSO} (MHz)**	**Mfin**	**M, R Value[2]**	**R loop**	**C loop**	**R post**	**C post**	**PLL Loop Bandwidth**	**Damping Factor**	**Passband Peak Amplitude (dB)**	**@ Center Freq.**
19.44	155.52	8	1	118.0kΩ	1.0µF	100kΩ	1000pF	270Hz	6.5	0.05	10Hz
			2	118.0kΩ	22.0µF	200kΩ	1000pF	134Hz	6.8	0.04	4Hz
77.76	155.52	2	1	59.0kΩ	1.0µF	100kΩ	1000pF	610Hz	6.5	0.05	20Hz
			2	59.0kΩ	2.2µF	100kΩ	1000pF	267Hz	6.8	0.04	10Hz
			8	118.0kΩ	2.2µF	200kΩ	1000pF	134Hz	6.8	0.04	10Hz
155.52	155.52	1	1	40.2kΩ	1.0µF	40.2kΩ	1000pF	740Hz	6.3	0.05	20Hz
			4	59.0kΩ	1.0µF	100kΩ	1000pF	267Hz	6.8	0.04	10Hz
			8	76.8kΩ	2.0µF	200kΩ	1000pF	180Hz	6.3	0.05	8Hz

Table 5: Example Loop Filter Component Values for M1010-01-155.5200

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

Note 2: For loop timing applications, the recommended value for the product of "Mfin" x "M" is 8 or higher.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 6: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 7: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 150-175MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			162		mA	
Differential Inputs	I_{IH}	Input High Current	DIF_REF0, DIF_REF1			150	µA	
			nDIF_REF0, nDIF_REF1			5	µA	
	I_{IL}	Input Low Current	DIF_REF0, DIF_REF1	-5			µA	
			nDIF_REF0, nDIF_REF1	-150			µA	
	V_{P-P}	Peak to Peak Input	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V	
	V_{CMR}	Common Mode Input		0.5		V_{CC} -	V	
LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	REF_SEL, FIN_SEL1, FIN_SEL0, SEL2, SEL1, SEL0	2		V_{CC} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
	C_{IN}	Input Capacitance				4	pF	
Inputs with Pull-down	I_{IH}	Input High Current	All Inputs *except* nDIF_REF1:0, SEL2:0			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ	
Inputs with Pull-up	I_{IH}	Input High Current	nDIF_REF1, nDIF_REF0, SEL2, SEL1, SEL0			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current		-150			µA	
	R_{pullup}	Internal Pull-up Resistor			51		kΩ	
All Inputs	C_{IN}	Input Capacitance	All Inputs			4	pF	
Differential Outputs	V_{OH}	Output High Voltage	FOUT, nFOUT	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [1]		0.4		0.85	V	

Note 1: Single-ended measurement. See Figure 5, Output Rise and Fall Time on pg. 7.

Table 8: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 150-175MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	18.75		175	MHz	
						50	MHz	
	F_{OUT}	Output Frequency	FOUT, nFOUT	150		175	MHz	
	APR	VCSO Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			200		kHz/V	
	R_{IN}	Internal Loop Resistor			2050		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @155.52MHz	1kHz Offset		-72		dBc/Hz	Fin=19.44_MHz Mfin=8, M=x, R=x
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms) @155.52MHz	12kHz to 20MHz		0.5		ps	
			50kHz to 80MHz		0.5		ps	
	odc	Output Duty Cycle [2]		45	50	55	%	
	t_R	Output Rise Time [2] for FOUT, nFOUT		325	450	500	ps	20% to 80%
	t_F	Output Fall Time [2] for FOUT, nFOUT		325	450	500	ps	20% to 80%

Table 9: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 5, Example Loop Filter Component Values for M1010-01-155.5200 on pg. 4.
Note 2: See Parameter Measurement Information on pg. 7.

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

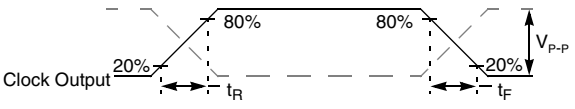

Figure 5: Output Rise and Fall Time

Output Duty Cycle

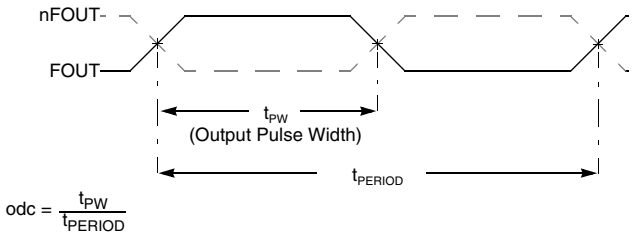

Figure 6: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

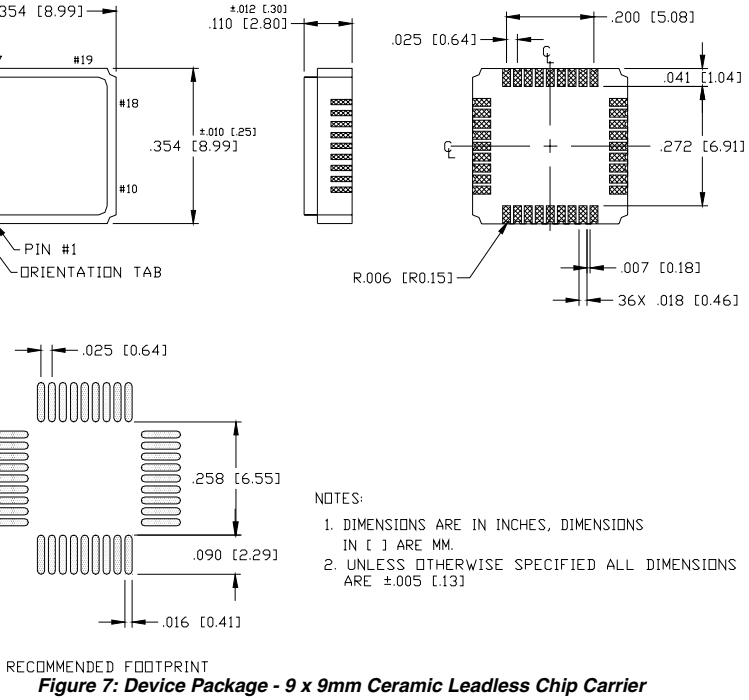

Figure 7: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

VCSO Freq (MHz)	Temperature	Order Part Number
155.52	commercial	**M1010-01-155.5200**
	industrial	**M1010-01I155.5200**
156.25	commercial	**M1010-01-156.2500**
	industrial	**M1010-01I156.2500**

Table 10: Ordering Information

Consult ICS for the availability of other VCSO frequencies.

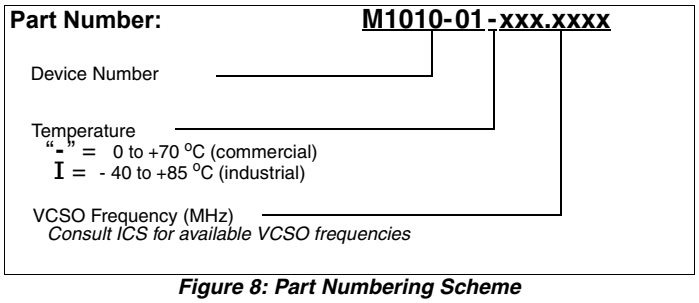

Figure 8: Part Numbering Scheme