DATA SHEET

UJA1061
Low speed CAN/LIN system basis chip

Objective specification

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Philips
Semiconductors

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CONTENTS

1 FEATURES

1.1 General

- Excellent EMC performance
- ± 8 kV ESD protection (human body model) for the outside module pins
- CAN/LIN-bus pins are short-circuit proof to the battery (up to 60 V) and to ground
- Battery and CAN/LIN-bus pins are protected against transients that occur in an automotive environment (ISO7637)
- Software Development mode partly disabling of fail-safe and watchdog functionality to ease software development
- Unique SPI readable device type identification
- Small footprint HTSSOP32 package (body 6 × 11 mm) with low thermal resistance.

1.2 System features

- 12 V, 24 V and 42 V system support with low sleep current (typical 50 μA)
- Support of 2.5, 3.0, 3.3 and 5.0 V microcontrollers with automatic adaption of interface levels to microcontrollers
- Flexible, independent external regulator extension via 14 V battery related pin INH (enables fail-safe scalable supply system)
- Smart operating and power management modes
- In-field Flash Programming mode
- Cyclic wake-up capability in Standby and Sleep mode
- Remote wake-up capability via CAN and LIN buses
- Local WAKE port with cyclic supply feature
- 42 V battery related local wake-up input
- 42 V battery related high-side switch output to drive external loads such as relays and wake-up switches
- Interrupt output with 12 maskable interrupt sources:
  - Interrupt service monitor
  - One interrupt per watchdog period to prevent microcontroller overloading; ensures predictable software behaviour
- Extensive set of SPI-readable system diagnostics:
  - Detection and detailed error reporting on CAN and LIN bus failures (e.g. shorts to GND/BAT, open bus wires, etc.)
  - TxD dominant and RxD recessive clamping as well as RxD to TxD short detection to prevent bus deadlocks
  - Local ECU ground-shift detection with two selectable thresholds
  - Over-temperature warning
  - Battery monitoring to detect battery interrupt or a chattering battery contact to store data before microcontroller power down (e.g. to store seat position)
  - Signalling of potential RAM-retention errors due to low microcontroller V_{CC}.

1.3 Fail-safe features

- Programmable fail-safe coded window and time-out watchdog with on-chip oscillator, guaranteeing autonomous fail-safe system supervision
- Fail-safe coded 16-bit SPI interface to microcontroller, including chip-select pin for multiple SPI devices on the same bus
- Integrated fail-safe and system features:
  - Rigorous error handling based on diagnostics
  - 12 dedicated reset sources supporting different, history dependent, software start-up and diagnosis
  - Global enable pin for control of safety critical hardware
  - Limp home output signal for activating application hardware in case system enters Fail-safe mode (e.g. switch on parking lights)
  - Single SPI message; no assembly of multiple SPI frames
  - Programmable active-low system reset with detection of both clamped and open reset line to prevent system deadlocks
  - Fail-safe coded activation of Software Development mode and Flash mode
  - 24-bit access-protected RAM can be used, for instance, for logging of cyclic problems.

1.4 CAN physical layer

- ISO11898-3 compliant fault-tolerant CAN transceiver
- Downwards compatible with TJA1054/TJA1054A
- Enhanced error signalling and reporting
- Separated low-drop-out voltage regulator for CAN bus:
  - Microcontroller supply independent, autonomous physical layer bus failure management
  - Significantly improves EMC performance
- Partial networking capability:
  - Completely passive behaviour to the bus when unpowered
  - Selective Sleep option with global wake-up allowing selected CAN bus communication without waking-up sleeping nodes.

1.5 LIN physical layer

- LIN2.0 compatible LIN transceiver
- Enhanced error signalling and reporting.

2 GENERAL DESCRIPTION

The UJA1061 is a System Basis Chip (SBC), replacing basic discrete components that are commonly used in Electronic Control Units (ECUs) for automotive body multiplexing. The UJA1061 supports any body application which controls various power peripherals by using the fault-tolerant CAN as the main physical layer and the LIN physical layer as local sub-bus. The UJA1061 contains the following integrated devices:

- Low speed, fault-tolerant CAN transceiver, inter-operable and downwards compatible with CAN transceivers TJA1054 and TJA1054A, and compatible with ISO11898-3 standard
- LIN transceiver compatible with LIN specification, revision 2.0
- Watchdog
- Separate voltage regulators for both host controller and CAN transceiver
- Serial peripheral interface (full duplex)
- Local wake-up input port
- Inhibit output port.

In addition to the cost advantages compared with conventional multi-chip solutions, the UJA1061 offers an intelligent combination of system-specific functions such as:

- Advanced low power concept
- Safe and controlled system start-up behaviour
- Advanced fail-safe system behaviour that prevents any deadlock
- Detailed status reporting on system and sub-system (for example, CAN) levels.

The UJA1061 is intended to be used in combination with a microcontroller and a CAN controller. The microcontroller is the first to come and the last to go in an ECU designed with the UJA1061. In failure situations, the UJA1061 maintains the microcontroller function as long as possible in order to provide full monitoring and software driven fall-back operation.

The UJA1061 can be operated in:

- Single 42 V power supply architecture when combined with an external step-down converter
- Single 14 V power supply architecture
- Dual 14 V and 42 V power supply architecture.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
UJA1061TW/*	HTSSOP32	plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-1

Note

1. Add suffix to indicate version:
   * = 5V0 for 5 V version
   * = 3V3 for 3.3 V version
   * = 3V0 for 3 V version
   * = 2V5 for 2.5 V version.

4 BLOCK DIAGRAM

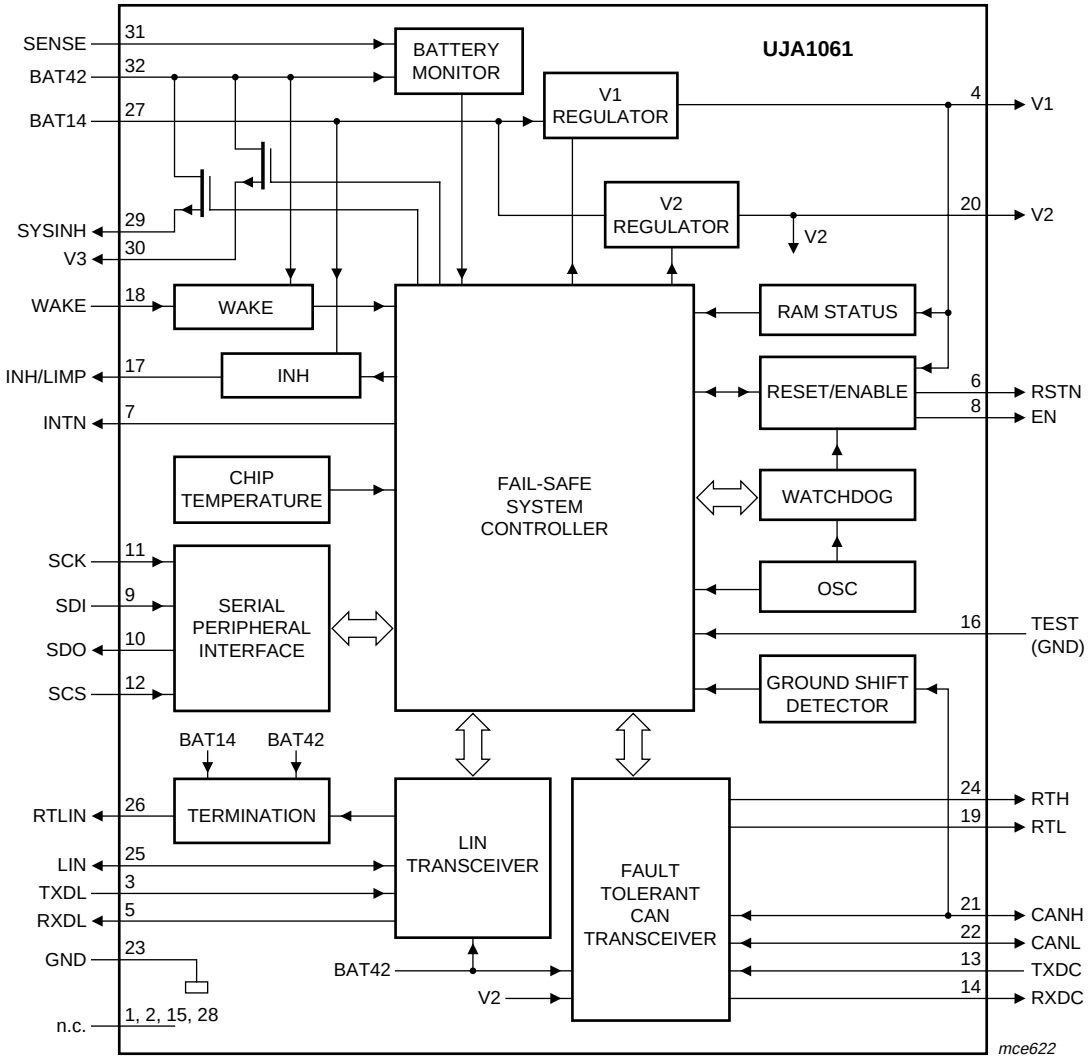


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
TXDL	3	transmit data input to activate the LIN output drive; LOW = LIN-bus dominant; HIGH = LIN-bus recessive
V1	4	regulated supply voltage output for microcontroller; voltage is 5 V, 3.3 V, 3 V or 2.5 V according to version
RXDL	5	receive data output for reading data from the LIN-bus; LOW when LIN-bus is dominant; HIGH when LIN-bus is recessive
RSTN	6	active LOW push-pull output used to reset the microcontroller; the UJA1061 also monitors the voltage on pin RSTN for any clamping situation (fail-safe)
INTN	7	active LOW open-drain output used to interrupt the microcontroller; pin INTN is to be wire-ANDed with other interrupt outputs within the ECU
EN	8	push-pull enable output related to voltage regulator V1; active HIGH if the watchdog is triggered successfully and a control bit is set; immediately pulled LOW with any reset event (e.g. a watchdog overflow); full set/clear application access via SPI while watchdog is served properly
SDI	9	SPI data input
SDO	10	SPI data output
SCK	11	SPI clock input
SCS	12	active LOW select input used to enable an SPI access
TXDC	13	transmit data input that activates the CAN output driver; LOW = CAN-bus dominant; HIGH = CAN-bus recessive
RXDC	14	receive data output for reading data from the CAN-bus; LOW when CAN-bus is dominant; HIGH when CAN-bus is recessive; output is continuously LOW upon a wake-up event received via the CAN-bus
n.c.	15	not connected
TEST	16	test pin; connect to ground in application
INH/LIMP	17	14 V battery related inhibit output for system extension, or ‘limp home’ output, activated in Fail-safe mode (default floating)
WAKE	18	42 V battery related local wake-up input
RTL	19	CAN termination resistor connection; in case of a CANL bus wire error this line is terminated with a selectable impedance
V2	20	regulated 5 V supply output reserved for CAN transceiver; an external buffer capacitor connects to this pin
CANH	21	CAN-bus line; HIGH in dominant state and LOW in recessive state
CANL	22	CAN-bus line; LOW in dominant state and HIGH in recessive state
GND	23	ground
RTH	24	CAN termination resistor connection; in case of a CANH bus wire error this line is terminated with a selectable impedance
LIN	25	LIN-bus line; LOW when LIN-bus is dominant, HIGH when LIN-bus is recessive
RTLIN	26	LIN-bus termination resistor connection
BAT14	27	14 V battery supply input
n.c.	28	not connected

SYMBOL	PIN	DESCRIPTION
SYSINH	29	42 V inhibit (controlling an external 42 V to 14 V DC-to-DC converter, for example)
V3	30	unregulated 42 V supply output, Continuous and Cyclic modes for supply of wake-up switches, Cyclic mode synchronized with local WAKE input ports
SENSE	31	fast battery interrupt/chatter detector input
BAT42	32	42 V battery supply input; protected up to 60 V

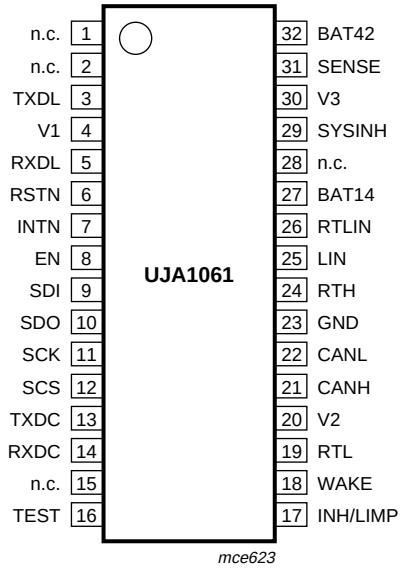


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Introduction

The UJA1061 combines all peripheral functions around a microcontroller within typical automotive body multiplexing applications into one dedicated chip. The functions are:

- Power supply for host microcontroller
- Power supply for CAN physical layer
- Switched BAT42 output
- System reset
- Watchdog with Window and Time-out modes
- On-chip oscillator
- Fault-tolerant CAN and LIN physical layers for serial communication suitable for 12 and 42 V applications
- SPI control interface
- Local wake-up input
- Inhibit output, or ‘limp home’ output
- System Inhibit output port
- Compatibility with 42 V power supply systems
- Fail-safe behaviour.

6.2 Fail-safe system controller

The fail-safe system controller is the ‘heart’ of the UJA1061 and is controlled mainly by the watchdog, which is clocked directly via a dedicated, on-chip oscillator. It handles the register configuration and controls all internal functions of the UJA1061. The device status information is collected and reflected to the microcontroller. Also the reset and interrupt signals are provided by the system controller.

The system controller is a state machine. The different levels of operation provided are represented in Fig.3.

6.2.1 Fail-safe mode

During severe fault situations the UJA1061 always enters its Fail-safe mode (see also Fig.3). This mode has the lowest possible system power consumption. These fault situations are:

- On-chip oscillator failure (frequency too low). Fail-safe mode is entered from any other mode immediately after this failure is detected
- Pin RSTN is clamped HIGH for more than 128 ms while the UJA1061 tries to drive pin RSTN LOW. The Fail-safe mode will be entered immediately out of any other mode in which the UJA1061 tries to drive pin RSTN LOW (Start-up, Standby or Sleep mode) after detecting this failure
- Pin RSTN is clamped LOW for more than 256 ms after the UJA1061 has released the pin RSTN internally in Start-up or in Restart mode
- A falling edge on pin RSTN during the initialization phase in Restart mode
- No successful initialization of Normal mode within 256 ms after pin RSTN has become HIGH in Restart mode whereby that the software-controlled Software Development mode is not active
- Wrong mode register code within Restart mode
- Wrong SPI count within Restart mode
- Low V1 regulator output for more than 256 ms due to a too-high load or a short-circuit of V1 to ground in Start-up mode
- Low V1 regulator output directly after an already-released pin RSTN in Restart mode.

The following events cause the system to exit the Fail-safe mode if the on-chip oscillator is running correctly:

- Activity on the CAN-bus
- Activity on the LIN-bus
- Activity on pin WAKE.

The UJA1061 restarts out of Fail-safe mode and enters Start-up mode to give the application a new opportunity to start. Regulator V1 starts again and the reset pulse will be set to the long period (see Section 6.5.1).

6.2.2 Start-up mode

Start-up mode is entered after a number of events that result in a system reset (see Fig.3) and is the first opportunity for the system to start-up. These events are:

- The first battery and ground connection of the module whereby the power supply V1 for the host microcontroller becomes active for the first time. The UJA1061 provides a Power-on reset for the system. As this is the first connection of the battery, the UJA1061 has no indication of the reset length required by the host microcontroller, therefore the long reset sequence is chosen as default

- An external reset event is applied to the reset input of the UJA1061. Here, if pin RSTN was already HIGH before the event (as in Normal, Standby or Flash mode), any other operating mode of the UJA1061 is left immediately and the external reset pulse is lengthened by the UJA1061 to the user-defined reset period. An external reset event does not allow the UJA1061 to be forced back to Start-up mode out of Restart or Fail-safe mode to deal with a chattering and/or a clamped reset line. In such a case, the system has to end within Fail-safe mode with the lowest possible power consumption.
- An undervoltage is detected at the V1 supply. In this case any other operating mode of the UJA1061 in which V1 was active (Normal, Start-up or Flash mode) is left immediately and the external reset pulse is lengthened by the UJA1061 to the user-defined reset period. Further undervoltage conditions do not allow the UJA1061 to be forced out of Restart or Fail-safe mode in order to deal with continuous undervoltages on V1.
- The system has left the fail-safe condition due to a wake-up event with a running oscillator. Here again the long reset period is applied in order to guarantee a proper system start.

When the reset period is finished (pin RSTN is released and goes HIGH) the watchdog waits for initialization. If the watchdog initialization is correct, the selected operating mode is entered. The only correct watchdog initialization out of start-up is a successful SPI access of the mode register, whereby the init Normal mode or init Flash mode is selected.

As Start-up mode is the ‘home page’ of the UJA1061, below a mode-oriented overview of the events, which result in a mode transition towards Start-up mode.

Being in Sleep mode, Start-up mode will be entered using the user-defined reset pulse if:

- Activity on the CAN-bus or LIN-bus is detected
- A falling edge on the local input port is detected
- A watchdog time-out occurs (used for cyclic wake-up of the module)
- A failure at the V3 power supply pin occurs (only if V3 is active).

Being in Fail-safe mode, Start-up mode will be entered using the long reset pulse if:

- Activity on the CAN-bus or the LIN-bus and the oscillator functions correctly again
- A falling edge on the local input port is detected and the oscillator functions correctly again.

Being in Normal, Standby or Flash mode, Start-up mode will be entered if:

- A falling edge on pin RSTN is detected. If pin RSTN is held LOW externally for a long period, Fail-safe mode will be entered directly since a serious ECU problem exists
- An unwanted undervoltage condition at V1. In the case where V1 is active and then falls below the undervoltage detection threshold the UJA1061 immediately enters Start-up mode forcing pin RSTN LOW. If V1 keeps within the undervoltage condition for a long time, this again is an indication of a malfunctioning application and the UJA1061 enters Fail-safe mode without first entering Restart mode. A reset as a result of this condition can occur only when V1 was already active with a HIGH level on pin RSTN

Start-up mode also will be entered out of Standby mode on the following events (restarting a continuously powered microcontroller with a user-defined reset pulse):

- A wrong mode register code access occurs
- The microcontroller supply current increases as a result of an externally activated microcontroller in the Watchdog OFF mode if the reset option is selected
- A watchdog time-out did occur if the reset option is selected
- Activity on the CAN-bus or LIN-bus is detected if the reset option is selected, even if the microcontroller did request a change to Sleep mode during a pending wake-up
- A falling edge on the local input port is detected if the reset option is selected, even if the microcontroller did request a change to Sleep mode during a pending wake-up
- After an ignored interrupt. Depending on the application software, certain events can force an interrupt or a reset event. In the case of interrupts, these interrupt events have to be served by the application software within 256 ms. If the software does not react within this time, the UJA1061 will force a transition into Start-up mode with a defined reset behaviour.

Being in Normal mode, Start-up mode will be entered if:

- A wrong mode register code access occurs
- On too-late or too-early watchdog triggering
- After an ignored interrupt (same as an ignored interrupt in Standby mode)
- Flash mode entry sequence is written to the mode register
- During a pending wake-up when the microcontroller did request a mode change to Sleep mode.

Being in Flash mode, Start-up mode will be entered if:

- A wrong mode register code access occurs
- On a watchdog trigger overflow (too late)
- After an ignored interrupt (same as an ignored interrupt in Standby mode).

When entering Start-up mode, the reset source information is provided by the UJA1061 in order to support different software initialization cycles that depend on the reset event.

6.2.3 RESTART MODE

The intention of the Restart mode is to give the application a second opportunity to start-up, if the first start-up has failed due to a certain failure. Restart mode will be entered out of the start-up as shown in the state diagram (see Fig.3). The events are as follows:

- A watchdog initialization failure occurs (wrong mode register code or start-up time-out
- An SPI failure (SPI count other than 16) occurs
- A falling edge on pin RSTN occurs during the initialization phase in Start-up mode
- A falling edge on pin RSTN occurs during start-up.

Entering Restart mode will always lengthen the reset pulse to the long period in order to guarantee a proper reset length independent from history.

If one of these failures still occurs after entering this mode; pin RSTN stays LOW or if the UJA1061 detects an undervoltage on V1 after an already released pin RSTN, Fail Safe mode will be entered. If the failure has been removed during Restart mode and the watchdog initialization has been successful, the selected operating mode will be entered. The only correct watchdog initialization out of Restart mode is the SPI access of the Mode register, whereby the init Normal mode has been selected.

6.2.4 NORMAL MODE

The Normal mode is entered after the following events (see Fig.3):

- Watchdog initialization has been executed successfully after an init Normal mode access of the mode register out of Start-up or Restart mode
- Out of Standby mode via an SPI command.

In this mode the UJA1061 allows access to all system resources such as CAN, LIN, INH and EN and therefore requires accurate watchdog triggering using the Window mode with programmable windows. Upon any false watchdog trigger, a system reset is performed.

Interrupts to the host microcontroller initiated by the UJA1061 are also observed. A system reset is performed if the host microcontroller does not react within 256 ms.

Entering Normal mode does not activate the CAN physical layer automatically. A certain bit (CAN mode) is used to activate the CAN medium if desired, enabling local cyclic wake-up scenarios to be implemented without affecting the CAN physical layer.

6.2.5 STANDBY MODE

Standby mode sets the system into a state with reduced current consumption. Entering Standby mode will automatically clear the CAN mode bit, thus allowing the CAN physical layer to enter the Low-power mode autonomously. However, the watchdog still monitors the microcontroller (Time-out mode) since it is powered via pin V1.

In case the host microcontroller can provide a Low-power mode with reduced current consumption in its standby or stop mode, the watchdog can be switched-off entirely within Standby mode of the UJA1061. The UJA1061 monitors the microcontroller supply current to make sure that there is no unobserved phase with disabled watchdog and running microcontroller. The watchdog will keep active until the supply current drops below a certain limit. Below this current limit the watchdog is disabled. If the current increases again, e.g. caused by a microcontroller wake-up from application-specific hardware, the watchdog starts operation again with the previously-used time-out period. A system reset can be performed if programmed accordingly, in this case Start-up mode is entered.

If Standby mode is entered out of Normal mode with selected watchdog-off option, the watchdog uses the maximum time-out defined for Standby mode until the supply current drops below the current detection threshold. Now the watchdog is off. If the current increases again the watchdog will become active immediately using the maximum watchdog time-out period again.

Generally, the microcontroller can be activated out of Standby mode via a system reset or via an interrupt without reset. This allows different start-up behaviours out of Standby mode to be implemented, depending on application needs:

- If the watchdog is still running during Standby mode, the watchdog can be used for cyclic wake-up behaviour of the system. A dedicated Watchdog Time-out interrupt Enable (WTE) bit allows a decision whether the microcontroller should receive an interrupt or a hardware reset upon overflow. The interrupt option will be cleared in hardware automatically with each watchdog overflow to make sure that a failing main routine is detected while the interrupt service still operates. Therefore the application software must set the interrupt behaviour again before the next standby cycle is entered.
- Any wake-up via the CAN or the LIN bus as well as a local wake-up event will force a system reset event or an interrupt to the microcontroller. So it is possible to leave Standby mode without any system reset if desired.

Upon an interrupt event the application software has to read the interrupt register within 256 ms. If this is not executed, the fail-safe system reset is forced and Start-up mode is entered. If the application has read out the interrupt register in time, it can decide to switch into Normal mode via SPI access or to stay in Standby mode.

The following operations are possible within Standby mode:

- Cyclic wake-up by the watchdog via an interrupt signal to the microcontroller (the microcontroller is triggered periodically and checked for the correct response)
- Cyclic wake-up by the watchdog via a reset signal (a reset is performed periodically; the UJA1061 provides information about the reset source in order to allow different start sequences after reset)
- Wake-up by bus activity on CAN or LIN via an interrupt signal to the microcontroller
- Wake-up by bus activity on CAN or LIN via a reset signal
- Wake-up by increasing microcontroller supply current without a reset signal (where a stable supply is needed for the microcontroller RAM contents to remain valid and wake-up comes from an external application not connected to the UJA1061)
- Wake-up by increasing microcontroller supply current with reset signal
- Wake-up due to an edge at pin WAKE forcing an interrupt to the microcontroller
- Wake-up due to an edge at pin WAKE forcing a reset signal.

6.2.6 SLEEP MODE

Within Sleep mode the microcontroller power supply (V1) and the INH controlled external supplies are switched off entirely thus resulting in minimum system power consumption. In this mode, the watchdog runs in Time-out mode or is completely OFF.

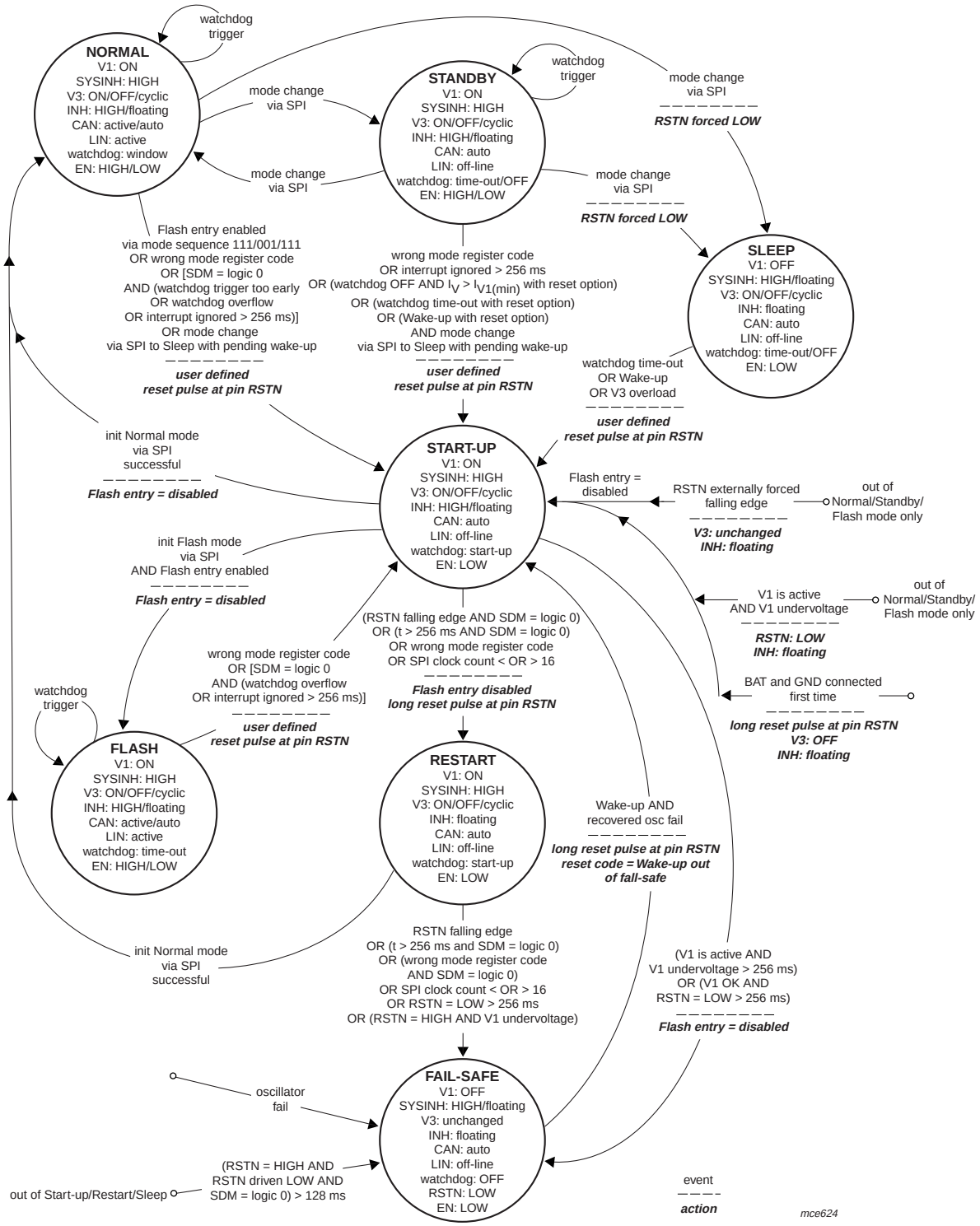
Entering Sleep mode results in an immediate LOW level on pin RSTN, thus stopping any operation of the microcontroller. In parallel, the INH output is floating and pin V1 is disabled. Only SYSINH could remain active to support the V2 voltage supply; this depends on CAN programming. It is also possible for V3 to be ON, OFF or in Cyclic mode in order to supply external wake-up switches.

If the watchdog is not disabled in software, the watchdog keeps running and forces a system reset upon overflow of the programmed period time. The UJA1061 enters Start-up mode and pin V1 becomes active again. This behaviour could be used for a cyclic wake-up out of Sleep mode.

Entering Sleep mode can be done only from Normal mode or from Standby mode with a mode change via the SPI.

Depending on the application, the following operations are selectable within Sleep mode:

- Cyclic wake-up by the watchdog (only in Time-out mode); a reset is performed periodically, the UJA1061 provides information about the reset source in order to allow different start sequences after reset
- Wake-up by bus activity on CAN or LIN
- Wake-up due to a falling edge at pin WAKE
- An overload on V3, only if V3 is in a cyclic or in continuously-on mode.



SDM = logic 0 represents the normal watchdog behaviour.

Fig.3 Main state diagram UJA1061.

6.2.7 FLASH MODE

Flash mode can be entered only from Start-up mode if a certain fail-safe mode control sequence has been applied to the UJA1061 within Normal mode. This control sequence comprises three consecutive write accesses to the mode register within the legal windows of the watchdog using the mode codes ‘111’, ‘001’ and ‘111’ respectively. As a result of this sequence, the UJA1061 enters Start-up mode providing a system reset and the related reset source information.

Within Start-up mode, the application software has the 256 ms start-up time available to enter Flash mode, using the init Flash code ‘011’ within the mode register thus feeding back a successfully received hardware reset (handshake between UJA1061 and microcontroller). This transition towards Flash mode is possible only once after the above fail-safe entry sequence.

The application can also decide not to enter Flash mode but switch over to Normal mode again using the init Normal mode code ‘101’ for handshaking. This again clears the prepared Fail-safe Flash mode entry. So if the Flash mode should be entered again, the fail-safe sequence has to be applied again.

The watchdog behaviour within Flash mode is similar to its time-out behaviour within Standby mode, however the mode code ‘111’ has to be used for serving the watchdog. If this code is not used or the watchdog overflows, the UJA1061 immediately forces a reset and enters Start-up mode again. This allows leaving Flash mode very quickly with a defined reset and without waiting for a watchdog overflow.

6.3 On-chip oscillator

The on-chip oscillator provides the clock signal for all digital functions and is the time reference for the on-chip watchdog and the internal timers.

If the on-chip oscillator frequency is too low or the oscillator is not running there is an immediate transition to Fail-safe mode. The UJA1061 will stay within Fail-safe mode until the oscillator has recovered to its normal frequency and the system receives a wake-up event. There is no possibility to have a system running without watchdog supervision or with erroneous watchdog supervision.

6.4 Watchdog

The watchdog fulfils the following basic tasks:

- Verifies proper microcontroller start-up
- Continuously monitors the microcontroller and performs a reset whenever the microcontroller fails to trigger the watchdog in time (according to the selected mode)
- Applies a cyclic wake-up to the sleeping microcontroller.

The watchdog is clocked directly by an independent on-chip oscillator.

In order to guarantee fail-safe control of the watchdog via the SPI, all watchdog accesses are coded with redundant bits. Therefore only certain codes are allowed for a proper watchdog service.

The following corrupted watchdog accesses are detected and result in an immediate system reset:

- Illegal watchdog period coding; only ten different codes are valid
- Illegal operating mode coding; only six different codes are valid
- A mode other than init Normal mode or init Flash mode is selected during the watchdog initialization phase.

Furthermore, any SPI access is monitored with respect to the number of clock (SCK) cycles. If enabled, an interrupt is forced whenever the clock count differs from 16 clock periods. Within Start-up and Restart mode a system reset instead of an interrupt is forced immediately in the event of an incorrect number of clock counts.

Any microcontroller-driven mode change is synchronized with a watchdog access by reading the mode information and the watchdog period information within the same register. This allows an easy software flow control with defined watchdog behaviour when switching between different software modules.

The watchdog, as an independent observation medium of the microcontroller, provides the following timing functions:

- Start-up mode; needed to give the software an opportunity to initialize the system
- Window mode; detects too early and too late accesses within Normal mode
- Time-out mode; detects a too late access; can also be used to restart or interrupt the microcontroller from time to time
- OFF mode; fail-safe shut-down during operation thus preventing any blind-spots in system supervision.

6.4.1 WATCHDOG START-UP BEHAVIOUR

Within Start-up and Restart mode of the UJA1061, the watchdog offers its start-up behaviour. In this mode the watchdog monitors pin RSTN (input) to check whether it becomes released or is clamped externally. Any time pin RSTN stays LOW longer than the reset monitoring period, this is interpreted as a clamping situation and the corresponding mode change of the UJA1061 is performed.

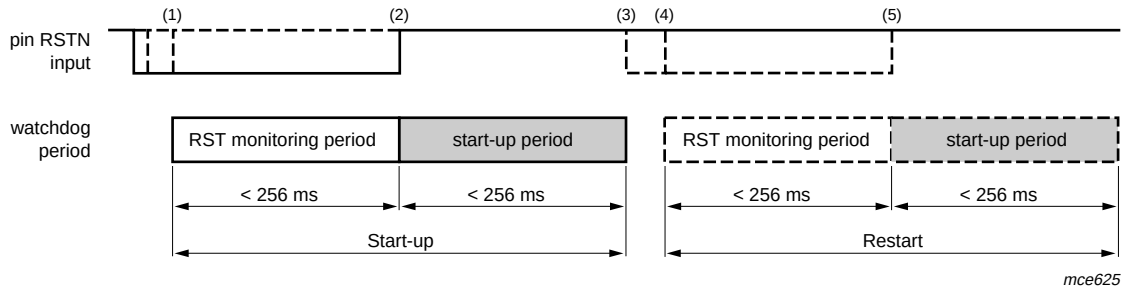
Once the reset pin has been released within the reset monitoring period the start-up period begins (see Fig.4). If the microcontroller does not initialize the watchdog within this time frame, the watchdog restarts the system via the reset output and enters Restart mode. The whole procedure with the reset monitoring period and the start-up period repeats. If pin RSTN is LOW for too long, or the microcontroller did not initialize the watchdog within the time, Fail-safe mode will be entered.

If pin RSTN has been released and the initialization phase is entered, a falling edge on pin RSTN results immediately in a transition from Start-up to Restart mode, or from Restart to Fail-safe mode (fail-safe behaviour in case of chattering reset events).

If pin RSTN is held LOW internally by the UJA1061, due to a low voltage situation at pin V1 caused, for example, by a short-circuit, the watchdog again monitors this time. After the reset monitoring period, Fail-safe mode is entered and pin V1 is disabled.

So, independently from the cause of a reset event, the watchdog starts the reset monitoring period whenever pin RSTN is pulled LOW.

During the start-up period, the UJA1061 accepts write access to the General Purpose registers, the Special Mode register (once after the first supply connection only) and the Mode register only.



(1) UJA1061 releases pin RSTN after 1 ms or 20 ms.
(2) External hardware releases pin RSTN.
(3) Watchdog initialization fails.
(4) 20 ms reset period.
(5) External hardware releases pin RSTN.

Fig.4 Reset monitoring and start-up period.

6.4.2 WATCHDOG WINDOW BEHAVIOUR

Whenever the UJA1061 has entered Normal mode as a result of a successful watchdog initialization, the Window mode of the watchdog has been activated. This makes sure that the microcontroller operates within the desired speed. Too fast as well as too slow operation will be detected. See Fig.5 for watchdog triggering using the Window mode.

The UJA1061 provides ten different period timings in this mode (with an accuracy of ±10 %).

The watchdog window has been defined to be between 50 and 100 % of the nominal programmed watchdog period.

The period can be changed on the fly with any valid SPI mode register access. Whenever the watchdog is triggered within the window time, the timer is reset in order to start a new period.

Any too early or too late watchdog access or wrong mode register code access results in an immediate system reset, entering Start-up mode.

In the background, any enabled interrupt event will be monitored by the watchdog. If the microcontroller does not react upon receipt of an interrupt within the interrupt response time (265 ms), a system reset will be performed.

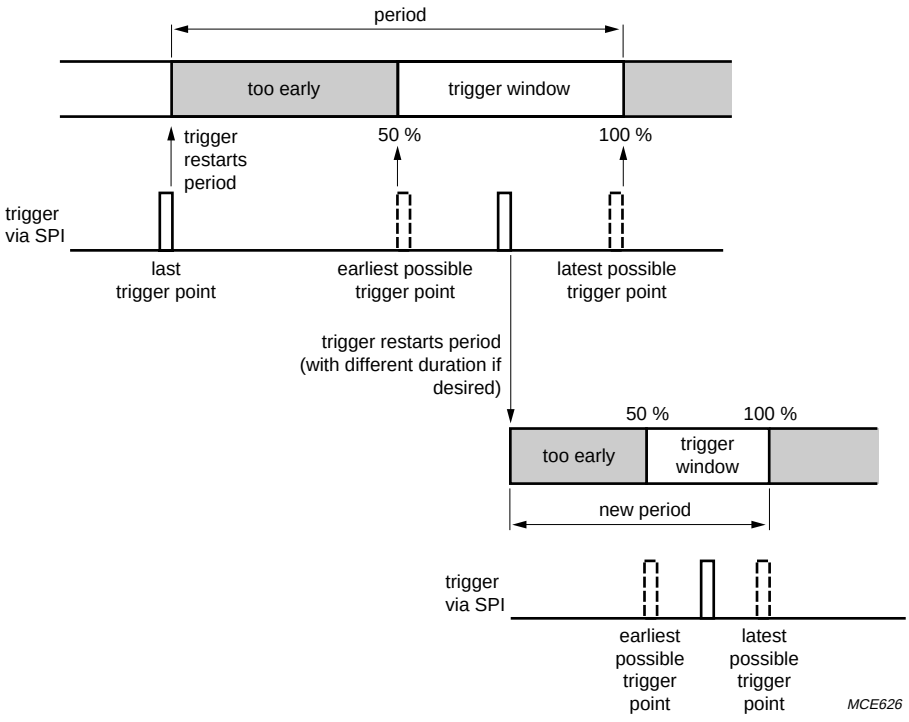


Fig.5 Watchdog triggering using Window mode.

6.4.3 WATCHDOG TIME-OUT BEHAVIOUR

Whenever the UJA1061 operates in Standby mode, in Sleep mode or in Flash mode, the watchdog is operated in Time-out mode. The watchdog has to be triggered within the actual programmed period time (see Fig.6). The Time-out mode can be used to provide cyclic wake-up events to the host microcontroller during Low-power modes.

In Standby and in Flash mode the nominal periods can be changed with any SPI access to the mode register. Since in Sleep mode regulator V1 is off and the microcontroller is not powered, no further change of the time-out period is possible.

Any wrong mode register code access results in an immediate system reset, entering Start-up mode.

6.4.4 WATCHDOG OFF BEHAVIOUR

Within Standby and Sleep mode, the watchdog OFF behaviour can be selected in order to disable the watchdog entirely.

If the watchdog is triggered with the watchdog OFF code while the UJA1061 is in Standby Mode, or while the UJA1061 enters Standby mode, the V1 current monitoring function stays disabled for a period of time equal to the previous or the default (4096 ms) watchdog period. The default period is selected if the Standby mode is entered directly with Watchdog OFF mode. After that period the current monitoring is enabled. Then the behaviour of the UJA1061 upon a too-high V1 current depends on the setting of the V1CMC bit within the System Configuration register. If bit V1CMC is set (reset option) a too-high V1 current causes immediately a reset. If bit V1CMC is not set (watchdog restart option), the watchdog starts a new period without the possibility to disable it except by triggering it again with the watchdog OFF code. If the watchdog OFF code is chosen the watchdog time-out interrupt has no function. If the watchdog off behaviour has been entered successfully and later on pin V1 current increases again, the watchdog starts operating with the previously programmed time-out period.

In case Standby mode is entered directly out of Normal mode with watchdog off behaviour coding, the watchdog keeps running with its maximum time period until pin V1 current falls below the threshold. If the current increases again, the maximum period is used again.

If Sleep mode is entered together with the watchdog OFF behaviour, the UJA1061 immediately forces pin RSTN to LOW level. In parallel, pin V1 is disabled and the watchdog is stopped.

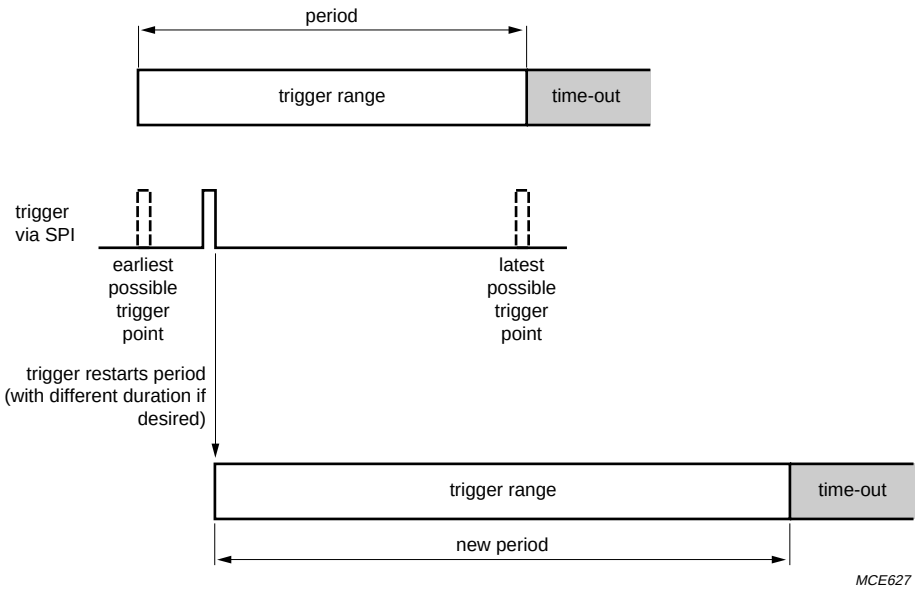


Fig.6 Watchdog triggering using Time-out mode.

6.5 System reset

The reset function of the UJA1061 offers two signals to deal with reset events:

- RSTN; the global ECU system reset
- EN; a fail-safe global enable signal.

6.5.1 System reset pin RSTN

The system reset pin RSTN is a push-pull bidirectional input/output. Pin RSTN is active LOW with selectable pulse length upon the following events (see Fig.3):

- Power ON (first battery connection) or BAT42 below Power-on reset threshold voltage
- V1 Power ON (wake-up out of Sleep mode), indicated as cyclic wake-up out of sleep
- Low V1 supply
- V1 current above threshold during Standby mode while watchdog OFF behaviour is selected
- V3 is down due to short-circuit condition during Sleep mode
- RSTN externally forced LOW, falling edge event
- Successful preparation for Flash mode completed; Flash mode can be entered now
- Wake-up out of Standby mode via CAN, LIN or WAKE while reset behaviour is selected; or wake-up out of Sleep mode via CAN, LIN or WAKE
- Wake-up event out of Fail-safe mode
- Watchdog trigger failures (too early, too late, overflow, time-out/not initialized in time, wrong code)
- Illegal mode code via SPI applied
- Interrupt not served within 256 ms.

All these events resulting in a reset have dedicated flags in order to distinguish between the different events. The only exception is the combination of the following two different reset sources: the Power ON (first battery connection), or pin BAT42 below Power-on reset threshold voltage and pin RSTN externally forced LOW, falling edge event. The reason is to have the same situation of the reset source code after a Power-on reset and an external reset as an emulator usually starts with a system reset. So during development of the UJA1061 software with an emulator, the UJA1061 will usually start-up with an external reset. If the emulator is not used, the software starts-up with the power-on code. Since the power-on code is a separate bit (PWONS; Power-ON Status) in the System Status register the microcontroller can distinguish between the Power-on reset and the external reset. The UJA1061 will be reset actively if pin RSTN is pulled LOW from external circuitry.

The UJA1061 will lengthen any reset event to 1 or 20 ms in order to make sure that external hardware is reset properly. After the first battery connection, a long Power-on reset of 20 ms is provided after voltage V1 is present. When started, the microcontroller can set the Reset Length Control (RLC) flag within the UJA1061; this allows the reset pulse to be shortened to 1 ms for future reset events. With this flag set, all reset events are shortened to 1 ms. Due to fail-safe behaviour, this flag will be reset automatically (to the longer one) within Restart mode, the first battery connection or with an externally-applied falling edge at pin RSTN. With this mechanism it is guaranteed that an erroneously-shortened reset pulse will restart any microcontroller at least within the second trial using the long reset pulse.

The behaviour of pin RSTN is shown in Fig.7. The duration of t_{RSTL} depends on the setting of the RLC flag (defining the reset length). Once an external reset event has occurred the system controller enters Start-up mode. Now the watchdog starts monitoring pin RSTN to check whether it is clamped or chattering. Finally Fail-safe mode is entered in case pin RSTN is not properly released. The reset state diagram is given in Fig.8.

If pin RSTN is released by the UJA1061 and the externally lengthening is shorter than 256 ms, the watchdog initialization starts with a time-out of 256 ms (start-up time). If the watchdog initialization has been successful within this start-up time, Normal or Flash mode will be entered. If the start-up time expires, Restart mode is entered providing a long reset pulse and resetting the V1 undervoltage threshold to the HIGH level. Now with a second system start and another 256 ms start-up time it is possible to enter Normal mode. If this fails again, Fail-safe mode is entered.

Furthermore, pin RSTN is monitored for a continuously LOW clamping situation. Once the UJA1061 pulls pin RSTN HIGH but pin RSTN level remains LOW for more than 256 ms, the UJA1061 immediately enters Fail-safe mode since this points to an application failure.

In order to prevent a continuously running microcontroller, the UJA1061 also detects HIGH-level clamping at pin RSTN. If the HIGH-level remains on the pin for more than 128 ms while pin RSTN is driven internally to a LOW level by the UJA1061, the UJA1061 falls back immediately to Fail-safe mode since the microcontroller cannot be reset any more. By entering Fail-safe mode, the V1 voltage regulator shuts down and the microcontroller stops.

Additionally, chattering reset signals are handled by the UJA1061 in such a way that the system safely falls back to Fail-safe mode with lowest power consumption. Externally applied reset signals force a mode change of the UJA1061 only within Normal, Standby and Flash mode. Within Start-up, Restart and Fail-safe mode, any externally applied reset signals are only monitored by the UJA1061 for clamping situations. In this way, no deadlock of the system is possible in the case of the reset line being affected by external disturbances.

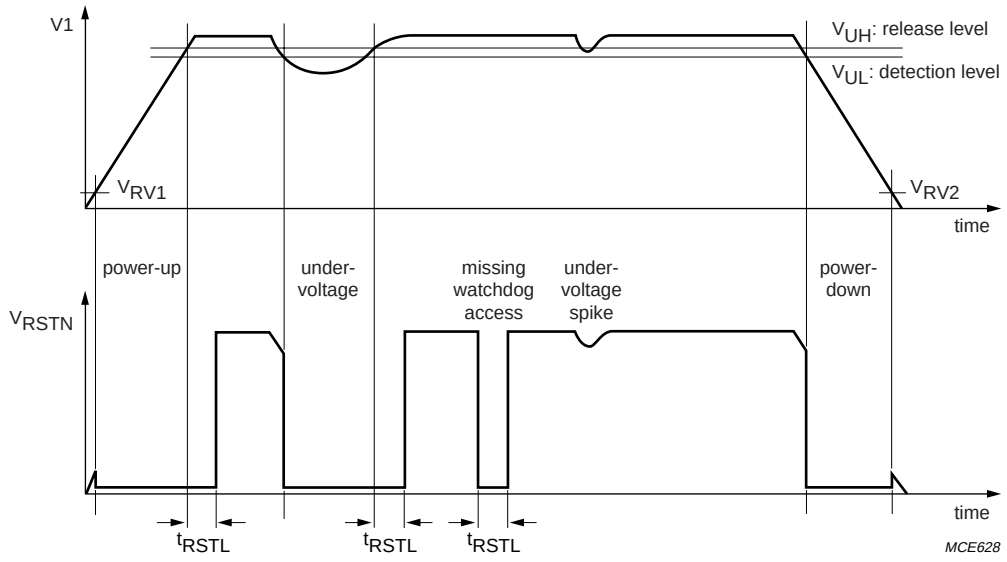


Fig.7 Reset pin behaviour.

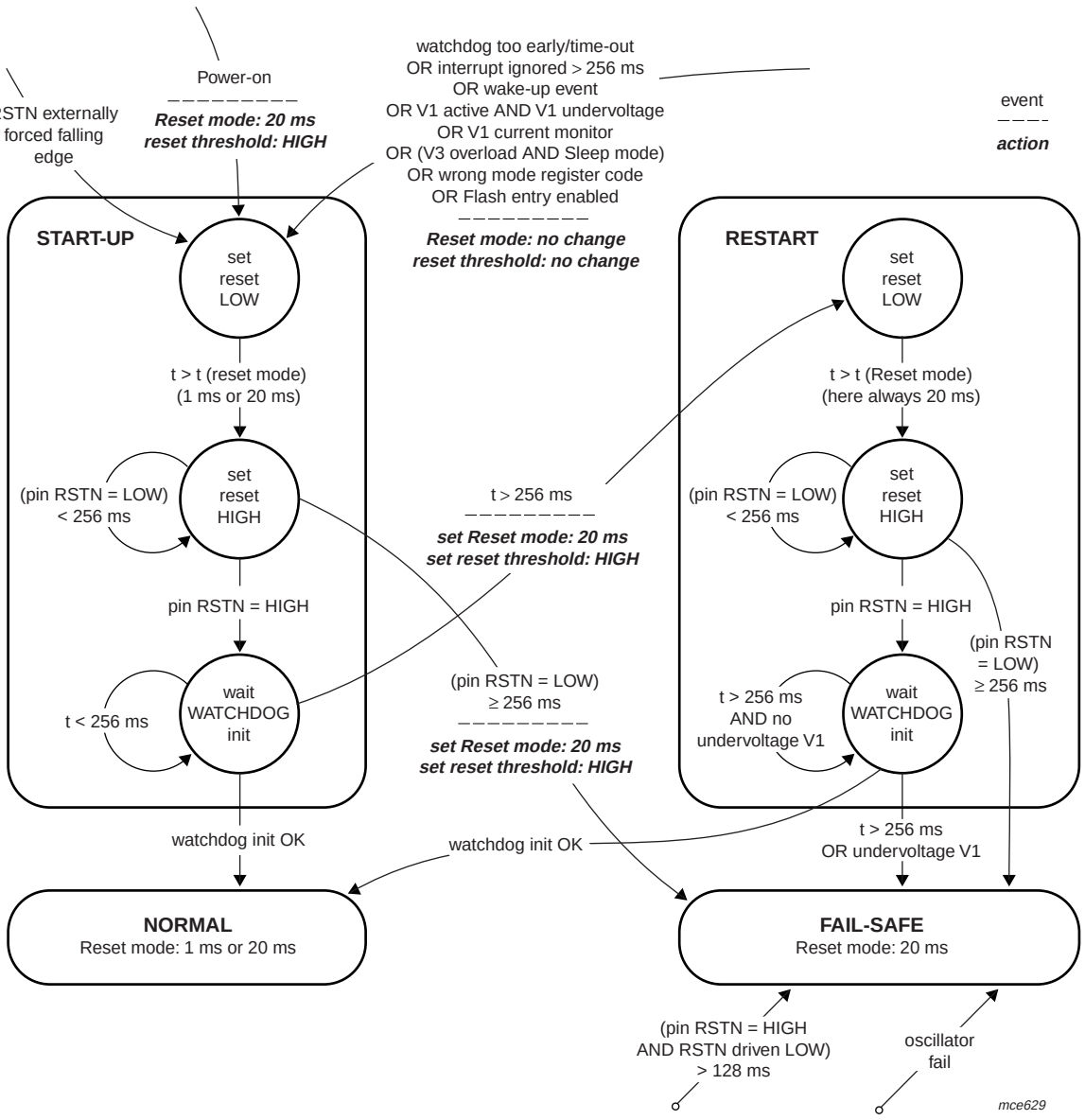


Fig.8 Reset state description.

6.5.2 Enable output pin EN

The functionality of the pin EN is almost identical to that of pin RSTN. The differences are:

- Output functionality only, not an input/output
- EN output can only be released by the microcontroller via an SPI access.

Pin EN, active LOW, is used for emergency shut-down of items such as external power components. During all reset events when pin RSTN is pulled LOW the EN control bit will be reset, pin EN will be pulled LOW and will stay LOW after pin RSTN is released, Within the Normal mode and Flash mode of the UJA1061, the microcontroller can set the EN control bit via SPI again. This results in releasing pin EN which then returns to HIGH-level. Based on this, the EN signal also can be used as a general purpose output when the system is running properly.

6.6 Power supplies

6.6.1 Supported battery systems

Besides the BAT14 supply pin (14 V), which is used to supply voltage regulators V1 and V2, the UJA1061 provides a BAT42 supply pin (42 V) in order to support 42 V systems. The UJA1061 supports three power supply architectures:

- Single 42 V battery system
  - pin BAT42 has to be connected to the 42 V battery
  - pin BAT14 has to be connected to, for example, a DC/DC converter (42 to 14 V or lower)
- Single 14 V battery system
  - both pins BAT14 and BAT42 have to be connected to the 14 V battery
- Two batteries (14 and 42 V) system
  - BAT42 has to be connected to the 42 V battery
  - BAT14 has to be connected to the 14 V battery.

To be able to control the external DC/DC converter for a single 42 V architecture or for connecting pin BAT 14 to a voltage lower than 12 V (in order to achieve a higher output current source capability of V1), SYSINH is HIGH when V1 and/or V2 is present, and is floating in all other cases.

In Sleep mode the SYSINH signal allows the external DC/DC converter to be disabled if both voltage supply outputs V1 and V2 are no longer needed. In this case the UJA1061 is powered only via pin BAT42 and pin SYSINH will float. In this situation, no input voltage is required at pin BAT14.

Whenever V1 and/or V2 is needed for the application, pin SYSINH will be set HIGH again, providing the BAT42 voltage to the external DC/DC converter or any other dedicated hardware.

6.6.2 Static and dynamic battery monitoring

Static battery monitoring is available at pin BAT42. With prolonged low voltages on pin BAT42, the UJA1061 forces a system reset and sets a dedicated Power-on reset flag in the reset source code register. Fail-safe mode will be entered, even if BAT14 is still connected.

The UJA1061 has a dedicated SENSE pin for dynamic monitoring the battery contact of an electronic control unit. As this SENSE pin is connected at the electronic control unit input before the connection to the external reverse current protection diode for pin BAT42, a fast detection of a power-down, e.g. caused by a loose battery connector, can be executed. The advantage is in the extra time for the microcontroller to shut down properly before a system reset occurs as a result of an undervoltage at V1.

6.6.3 Voltage regulators V1 and V2

The UJA1061 has two independent voltage regulators that are supplied through the external BAT14 input pin. One regulator (V1) is for the microcontroller and one regulator (V2) is for the fault tolerant CAN-transceiver. This dual regulator concept offers the following advantages:

- All noise coming from the microcontroller load is decoupled from the bus lines
- The UJA1061 can always support the complete fault-tolerant physical layer, including the biasing, even if the microcontroller is not present (V1 short-circuited or load is too high)
- The possibility of choosing a supply voltage for the microcontroller that is lower than 5,V, i.e. 3.3, 3 or 2.5 V according to version.

6.6.3.1 V1 voltage regulator

The V1 voltage regulator is targeted to supply the application microcontroller. As well as this primary function, the accuracy of this regulator makes it suitable to supply the reference voltage for the analog-to-digital converter of the microcontroller.

V1 voltage is monitored continuously in order to provide the system reset signal when undervoltage situations occur. Whenever V1 voltage falls below one of the two programmable thresholds, a hardware reset will be forced.

The RAM status monitor monitors the V1 voltage. If V1 voltage is lower than the minimum voltage needed for the microcontroller RAM while V1 is active, then the corresponding SPI bit will be set. This bit can be read by the microcontroller when V1 has recovered (no reset is generated).

Depending on the version-dependent output voltage of V1, the undervoltage reset threshold as well as the RAM status monitor threshold are adapted accordingly.

The V1 regulator is protected against overload. The maximum output current allowed at pin V1 depends on the input voltage connected to pin BAT14. The closer the input voltage comes to the V1 output voltage, the more output current can be sourced by the regulator. This feature is very useful in combination with an external DC/DC converter in providing a BAT14 voltage close to V1 (7 V, for example).

6.6.3.2 V2 voltage regulator

The second independent voltage regulator V2 provides a 5 V supply for the CAN transmitter. The pin V2 is intended for the connection of external buffering capacitors.

V2 is controlled autonomously by the CAN physical layer and is activated upon any detected CAN-bus activity, or is activated if the CAN physical layer is enabled by the application microcontroller. This supply is short-circuit protected and will be disabled in case of an overload situation. The status of V2 will be reflected to the application via dedicated interrupt and status flags.

6.6.4 SWITCHED BATTERY OUTPUT (V3)

V3 is a high-side switched BAT42-related output to drive external loads such as wake-up switches or relays. The features of V3 are as follows:

- Supports three application controlled modes of operation; On, Off or Cyclic mode
- Two different Cyclic modes allow the supply of external wake-up switches; these switches are powered intermittently (for 384 µs every 16 ms or for 384 µs every 32 ms) thus reducing the systems' power consumption in case a switch is continuously active; the wake-up input of the UJA1061 is synchronized with the V3 cycle time.
- The switch is protected against short-circuits to ground and current overloads. In case regulator V3 is overloaded, pin V3 is automatically disabled, the corresponding mode bit is reset and an interrupt is forced, if enabled. If the UJA1061 was in Sleep mode (V1 off), a wake-up is forced and the corresponding reset source code becomes available within the reset source register; this signals to the application that the wake-up source via V3-supplied wake-up switches has been lost.

6.7 CAN transceiver

The integrated fault-tolerant CAN transceiver of the UJA1061 is an advanced ISO11898-3 compliant version of the TJA1054/TJA1054A and is fully inter-operable with these two stand-alone transceivers.

The improvements and extensions of the integrated fault-tolerant CAN transceiver-cell compared with the TJA1054/TJA1054A are the following:

- Enhanced error signalling; all bus failures are separately forwarded to the SPI register
- Handling and reporting of clamping situations on CAN and RXD/TXD interface
- Ground shift detection with two selectable warning levels to detect possible local GND problems before the CAN communication is affected
- Supports Selective Sleep mode with global wake-up message filter
- Improved wake-up filtering for CANL
- No recovery of bus failures during mode changes between Normal mode or low power modes
- 42 V system support for CANL low power termination.

6.7.1 MODE CONTROL

Different to existing stand-alone fault-tolerant CAN transceivers, the integrated autonomous controller defines the mode of the CAN transceiver. This implies that the fault-tolerant CAN transceiver, which is supplied by its dedicated V2 supply, supports the bus failure management and bus levels in all modes and independently from the microcontroller. This ensures that even a failing microcontroller (or failing V1 supply) does not influence the communication of the rest of the CAN network. Furthermore fail-safe behaviour is guaranteed in all modes to protect the system against unwanted power consumption.

The controller of the CAN physical layer provides two major modes of operation of the CAN transceiver, the Active mode and the Auto mode (see Fig.9).

Two dedicated CAN status bits (CANMD) are available to indicate to the application whether the transceiver is in Normal, On-line, Selective Sleep or Off-line mode.

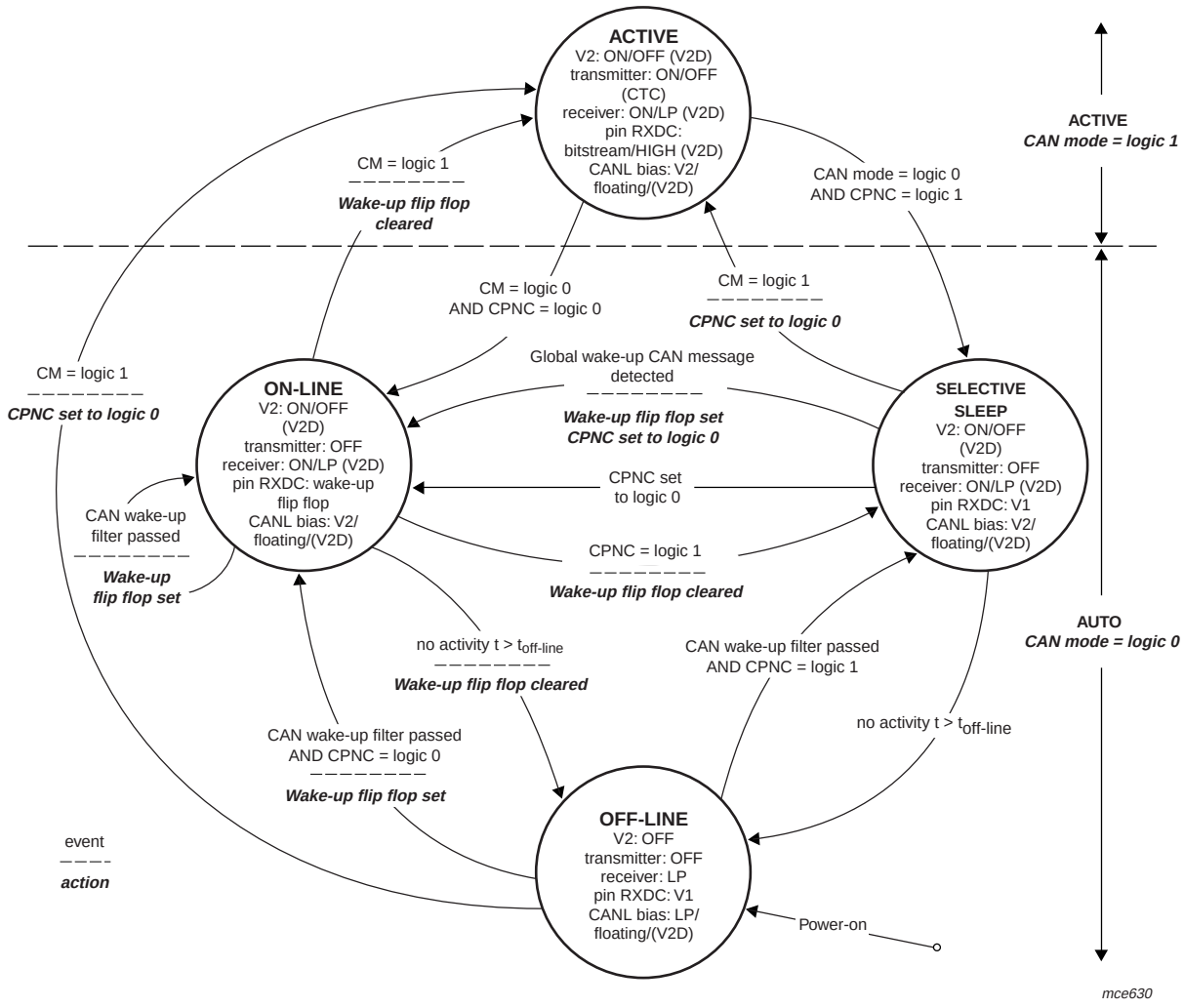


Fig.9 States of the CAN transceiver.

6.7.1.1 Active mode

Within the Active mode the CAN transceiver operates as in the Normal mode of the TJA1054. Here normal communication is possible with pin CANL terminated at the voltage rail V2 (5 V). The Active mode can be entered only using the CAN mode bit if the system controller is within its Normal mode or in Flash mode. Transmission and reception of messages is possible in the Active mode.

If the regulator V2 is not able to start within the V2 clamped LOW time ($>t_{V2(CLT)}$) or a short-circuit has been detected during an already activated V2, regulator V2 becomes disabled (V2D will be reset) and an interrupt is forced to the microcontroller, if enabled. The corresponding fail flag will be set at the same time; also the transmitter and receiver are switched off and any transmission of messages is blocked by the UJA1061. The termination of CANH and CANL will be set to floating.

If the microcontroller wants to transmit again, it can activate the transmitter, the corresponding termination and the receiver again by a falling edge of the CAN Transmitter Control (CTC) bit. If this continues to fail (V2 cannot start; V2D will be reset) an interrupt is forced again (if enabled) and V2, the transmitter, the receiver and the termination will be switched off again. This makes sure that a short-circuited V2 does not result in high power consumption.

A CAN transmitter OFF bit is available to set the CAN transceiver to a Listen-only mode. In this mode the transmitter output stage is disabled.

Within Active mode, a wake-up via CAN will never result in a reset.

6.7.1.2 Auto mode

The Auto mode is entered if the CAN mode bit is cleared. From now on no active transmission is possible. The transmitter will be switched off.

The Auto mode is also entered whenever the system controller leaves its Normal mode. This clears the CAN mode bit automatically.

Within Auto mode the physical medium is still supported (On-line and Selective Sleep mode) including the bus failure management as long as there is some activity on the bus lines. CANL continues to be terminated strongly towards V2 and V2 is active.

Once the bus becomes recessive or dominant for a certain time ($t_{offline}$) the transceiver goes to Off-line. The Off-line timer is programmable in two steps with the CAN Off-line Timer Control (COTC) bit. Entering Off-line will set the timer to the longest period independently of the COTC bit and will be reset with every CAN wake-up event

Three different states are implemented:

- On-line
- Selective Sleep
- Off-line.

6.7.1.3 On-line

On-line will be entered after the UJA1061 has detected some activity on CANL and/or CANH, while the transceiver was Off-line and the CAN Partial Networking Control (CPNC) bit was LOW. A CAN message containing a dominant phase, followed by a recessive phase and followed again by a dominant phase, results in a wake-up of the UJA1061, after having passed the CAN wake-up filter. Pin RXDC is forced LOW upon wake-up towards On-line and keeps LOW until the CAN mode bit is set (Active mode) or the CPNC bit is set to logic 1, entering Selective Sleep. Additionally a reset or interrupt is forced, if programmed accordingly.

On-line also can be entered by resetting the CAN mode bit, CM (Auto mode) during Normal mode of the UJA1061 with the CPNC bit set to LOW. After some bus activity, the wake-up flip flop will be set again, together with a LOW signal on RXDC. If the bus stays continuously dominant or recessive for the Off-line time ($t_{offline}$), Off-line will be entered, clearing the wake-up flip flop. Leaving On-line, the wake-up flip flop will be cleared in order to be ready for the next wake-up event.

6.7.1.4 Selective Sleep

Selective Sleep is selectable with the CAN Partial Networking Control (CPNC) bit. In contrast with On-line, in Selective Sleep any wake-up, with the exception of the Global Wake-up CAN message, due to CAN-bus activity is ignored but the physical medium, including bus failure management and strong termination, continues to be supported in order to support partial networking. In this mode, RXDC stays continuously at V1 level.

Entering Selective Sleep out of Off-line is possible when the CAN wake-up filter has been passed and the CPNC bit has been set previously to logic 1. In contrast with entering On-line out of Off-line, the wake-up flag is not set, so not resulting in any activity of V1 and the microcontroller.

Selective Sleep mode will also be entered out of On-line in case bit CPNC becomes logic 1. If the wake-up flag was set, it will be cleared.

Another possibility for entering Selective Sleep mode is resetting the CM bit in Active mode with bit CPNC set logic 1.

If the CAN-bus has been dominant or recessive continuously for the off-line time ($t_{offline}$), Off-line will be entered.

The second possibility to leave Selective Sleep and enter Active mode is by software control, possible by setting the CAN mode bit logic 1.

A third possibility to leave Selective Sleep is by entering On-line, possible only after detection of a dedicated Global Wake-up CAN message. This comprises two messages using any CAN identifier but a dedicated data pattern, first the CAN wake-up message pattern and second the Confirmation message pattern:

- CAN wake-up message: 0xC6 EE EE EE EE EE EE EF
- Confirmation message: 0xC6 EE EE EE EE EE EE 37.

There may be any other CAN message frame between the two message patterns.

The maximum message separation time period has to be less than $t_{timeout}$. If Selective Sleep was entered out of Off-line due to bus activity, the message separation timer will start directly without waiting for the first wake-up message data pattern. The Confirmation message data pattern, received before the overflow of the timer, is then sufficient to go to On-line. Whenever Selective Sleep is left, the Selective Sleep control bit is cleared again automatically.

Within Sleep mode, any wake-up event is automatically forwarded to the system reset due to power-up on V1.

6.7.1.5 Off-line

Within Off-line the CAN physical layer becomes automatically terminated towards an internal power supply, supplied out of BAT42. V2 is disabled in order to save supply current. Any CAN wake-up event automatically restarts V2, entering On-line or Selective Sleep. Wake-up is signalled via RXDC (LOW) and RSTN (LOW) or INTN (LOW) if programmed accordingly.
In On-line, pin RXDC is held LOW until the CAN mode bit is set successfully, or the CAN physical layer enters Selective Sleep by setting the CPNC bit logic 1.

Once the bus becomes recessive or dominant for a certain time ($t_{offline}$) the transceiver enters Off-line. The Off-line timer is programmable in two steps with the CAN Off-line Timer Control (COTC) bit. Entering Off-line will set the timer to the longest period independently of the COTC bit and will be reset with every CAN wake-up event

6.7.2 TERMINATION CONTROL

In Active mode, On-line and Selective Sleep, RTH and RTL are strongly terminated to ground and to V2 respectively. The Normal Bus-Failure Management (BFM) (known from the TJA1054/TJA1054A) is active. During short-circuits at CANL and/or CANH, the corresponding RTL or RTH pin becomes floating. When V2 is OFF or unstable, both pins become floating and the Normal BFM is left. A floating SYSINH results immediately in a switch-over towards floating RTH and RTL and skipping the Normal BFM because V2 level soon can fall.

6.7.3 BUS, RXD AND TXD FAILURE DETECTION

The UJA1061 can distinguish between bus, RXD and TXD failures as indicated in Table 1.

All failures will be signalled separately to a 4-bit register. Any change (detection and recovery) will give an interrupt to the microcontroller, if enabled (limited to only one interrupt per watchdog period). Polling of the SPI register is always possible.

6.7.3.1 GND shift detection

Two different GND shift levels can be detected, programmable by the microcontroller. Any detected or recovered GND shift event results in an interrupt of the microcontroller, if enabled (limited to only one interrupt per watchdog period).

Table 1 CAN-bus, RXD and TXD failure detection

FAILURE	DESCRIPTION	DRIVER AND BIASING CIRCUIT DISABLING
HxVCC	CANH to V_{CC} (5 V) short-circuit	CANH off, weak RTH
HxBAT	CANH to BAT (14 and 42 V) short-circuit	CANH off, weak RTH
HxGND	CANH to GND short-circuit	none
LxBAT	CANL to BAT (14 and 42 V) short-circuit	CANL off, weak RTL; note 1
LxGND	CANL to GND short-circuit	CANL off, weak RTL
LxVCC	CANL to V_{CC} (5 V) short-circuit	none
HxL	CANH to CANL short-circuit	CANL off, weak RTL
H//	CANH interrupted	none
L//	CANL interrupted	none
Bus Dom	bus is continuously clamped dominant (double failure); even within Single-wire mode the receiver remains dominant	CANL off, weak RTL
Bus Rec	bus is continuously clamped recessive (double failure); driving messages to the bus is not possible even while the driver is active	none
TxDC Dom	pin TXDC is continuously clamped dominant (handles also RXDC to TXDC short-circuits)	transmitter disabled but no change in biasing
RxDC Rec	pin RXDC is continuously clamped recessive	transmitter disabled but no change in biasing
RxDC Dom	pin RXDC is continuously clamped dominant	none

Note

1. CANL stays active with weak short-circuits to BAT due to wake-up requirements within large networks.

6.8 LIN transceiver

The integrated LIN transceiver of the UJA1061 has the following features:

- LIN specification revision 2.0 compatible
- 42 V system handling compatibility
- Disabling of the termination switch during a short-circuit from LIN to GND
- No reverse currents are possible from RTLIN to the battery
- Supports two different LIN-recessive levels; related to BAT42 or to BAT14.

The master and slave termination can be connected externally between pins LIN and RTLIN.

6.8.1 MODE CONTROL

The first state of the LIN transceiver following power-on is Off-line (see Fig.10). The transmitter and receiver both consume no current but wake-up events will be recognised by the separate wake-up receiver.

Pin RXDL reflects the status of the wake-up flip flop: HIGH after power-on; LOW after a wake-up event via the LIN-bus.

Any LIN event with a dominant LIN level longer than the specified wake-up time ($t_{BUS(LIN)}$) followed by a recessive level will wake-up the UJA1061, resulting in a LOW signal at pin RXDL and, if enabled, a LOW signal at pin RSTN or at pin INTN. When the UJA1061 enters Normal or Flash mode, the LIN transceiver automatically enters On-line and the wake-up flip flop will be cleared. The wake-up flip flop will be cleared also when the UJA1061 falls into Fail-safe mode as the result of a microcontroller wake-up failure. A remote LIN wake-up out of Standby or Flash mode will wake-up the system via a dedicated hardware reset or via an interrupt, depending on the LIN Interrupt Enable (LINIE) bit. With bit LINIE set to logic 1, pin INTN remains LOW until the interrupt register has been read and cleared.

A remote LIN wake-up out of Sleep or Fail-safe mode always happens with a reset independent of the programming due to the unpowered situation of the microcontroller. The differences between On-line and Off-line are as follows:

- **Off-line.** The transmitter is always off and pin RXDL continuously reflects the wake-up event at the LIN-bus
- **On-line.** The status of the transmitter is software controlled by the microcontroller via the LIN Transmitter Control bit (LTC) while pin RXDL reflects the data bit stream on the LIN-bus

Bit L42 determines whether the pin RTLIN is supplied by the BAT14 voltage source or by an internal 12 V supply generated from the BAT42 regulator, in order to support the future 42 V LIN standard. Pin RTLIN has to be applied via a buffer capacitor in case bit L42 is set. Default operating mode is BAT14 related. During On-line, with no short-circuit between the LIN bus and GND, pin RTLIN provides an internal switch to select BAT14 or the internal 12 V voltage, depending on the L42 bit. For master and slave operation an external resistor, respectively 1 kΩ or 30 kΩ, can be applied between pins RTLIN and LIN. An external diode in series with the termination resistor is not needed because an internal diode is incorporated.

If the LIN wire becomes short-circuited to GND, pin RTLIN will switch to a current source of approximately 75 μA to prevent significant battery discharge (some current is needed for failure recovery). A recessive level on the LIN wire activates the normal termination again. The 75 μA current source is also present in Off-line with no clamped dominant LIN-bus. Pin RTLIN floats in Off-line in case there is a short-circuit to GND.

Entering Active mode out of Off-line always results in switching on the strong switch at pin RTLIN, independent of a previously detected short-circuit on LIN to ground. If the short-circuit still exists, the switch will be substituted by the 75 μA current source after the dominant time-out at pin LIN. The different states of pin RTLIN are shown in Fig.11.

The receiver comparator levels are battery related to BAT14 in a 14 V system with the L42 bit cleared, and related to the internal 12 V voltage supply in 42 V systems with the L42 bit set.

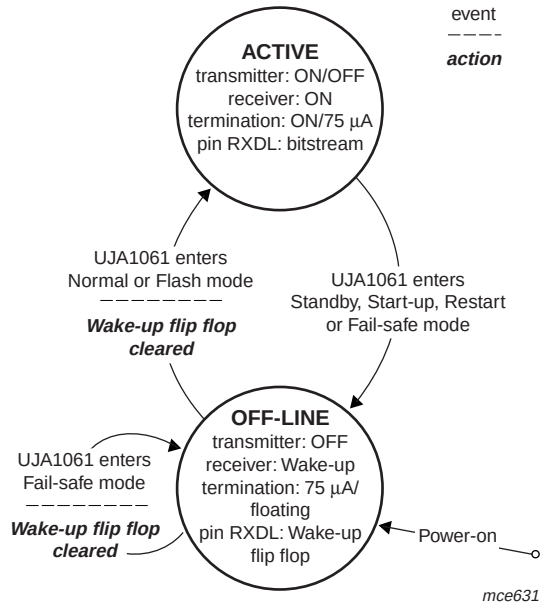


Fig.10 States LIN transceiver.

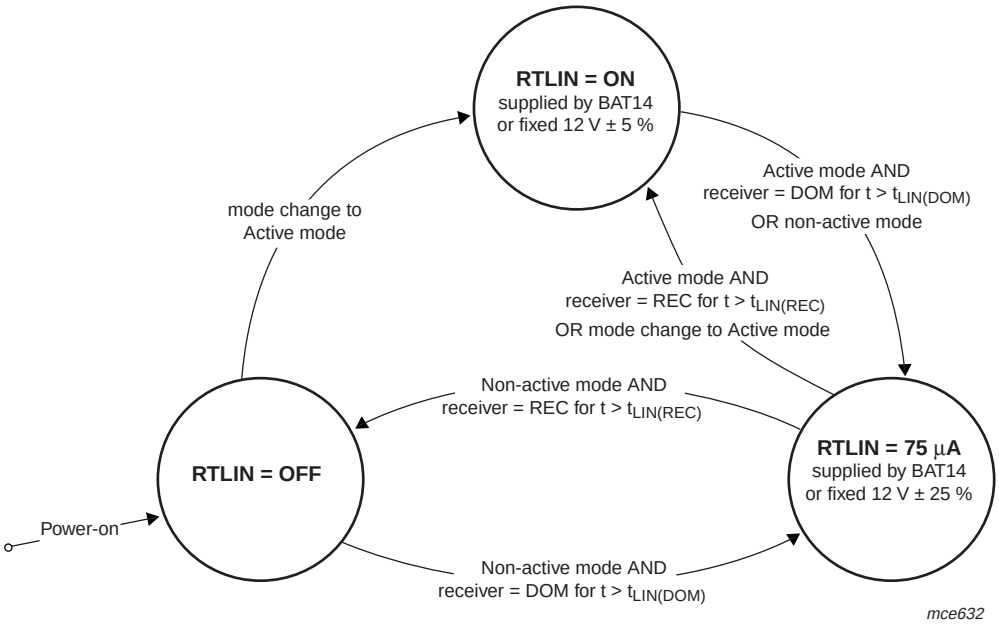


Fig.11 States of the RTLIN pin.

6.8.2 BUS AND TXDL FAILURE DETECTION

The UJA1061 handles and signals the following LIN-bus related failures:

- LIN-bus clamped dominant; within Active mode the termination switch at pin RTLIN is switched to the internal weak current source; within Off-line RTLIN will be floating
- TXDL clamped dominant; the transmitter is disabled
- LIN-bus clamped recessive; the transmitter is switched off and the LIN transmitter off bit (LTO) is set.

These failure events force an interrupt to the microcontroller whenever the status changes and the corresponding interrupt is enabled.

6.9 Inhibit output (pin INH)

The INH output pin, which can be used as inhibit for an extra (external) voltage regulator, is floating after the first powering of the UJA1061. This ensures that yet-to-be connected voltage regulators are switched off. The INH bit in the corresponding SPI register can be accessed in Normal mode, Flash mode and in Standby mode. Whenever Restart, Sleep or Fail-safe mode is entered, the INH bits are reset again, with pin INH floating as the result. This is also true whenever undervoltage of V1 has been detected, or an external reset edge is applied to the UJA1061. Therefore, the application has to reactivate external supplies in a failure situation or in the event of an external reset.

The INH output pin can also be programmed as ‘limp home’ output, which is also floating after power-up but is activated by the UJA1061 in case the UJA1061 enters Fail-safe mode. For fail-safe reasons, this ‘limp home’ behaviour of pin INH can be activated by setting the Limp Home Mode (LHM) bit via the Special mode register. This LHM bit can therefore be set only once after a first battery connection before the watchdog is initialized, that is within the 256 ms start-up period and before the first SPI write access to any other register.

6.10 Wake-up input (pin WAKE)

The behaviour of pin WAKE depends on the sampled level: a pull-down behaviour is activated when the pin is pulled LOW, and a pull-up behaviour towards BAT42 is activated when the pin is pulled HIGH externally.

The setting of the WAKE Sample Control bit (WSC) defines the sample mode of the pin:

- Continuous sampling (with an internal clock) if the bit is set logic 1
- Sampling synchronised to the cyclic behaviour of V3 if the bit is set logic 0 (see Fig.12). This is to save bias current within external switches in low-power operation. Two repetition times are possible: 16 and 32 ms.

If V3 is continuously ON, pin WAKE input will be sampled continuously also, regardless of the level of the bit WSC.

If the interrupt mode is selected, a negative edge on pin WAKE sets pin INTN immediately to LOW. Reading the corresponding interrupt register clears all bits. If the reset mode is selected, the wake-up event forces a hardware reset without interrupt. The reset source bits in the System Status register reflect the source of the reset event, while dedicated status bits, Edge WAKE Status (EWS) and Level WAKE Status (LWS), within the same register, offer information according the actual status of pin WAKE. These two bits can be polled and read out also when the interrupt option instead of the reset option has been chosen.

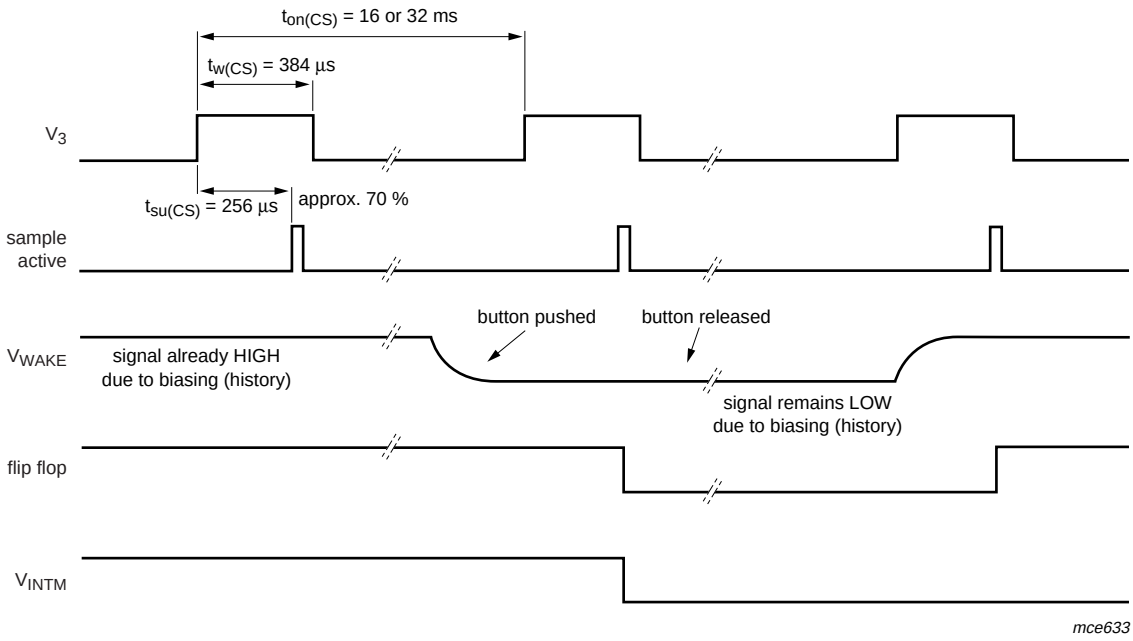


Fig.12 Pin WAKE, cyclic sampling via V3.

6.11 Interrupt output

In order to support multiple interrupt sources within a system, pin INTN provides an open-drain output configuration.

Whenever at least one bit is set within the interrupt register this pin is forced LOW. Reading the interrupt register clears all set bits. Only these bits are cleared as they have definitely been read during that access.

The interrupt register will be cleared also during a system reset (RSTN LOW).

6.12 Temperature protection

The temperature of the UJA1061 chip is monitored as long as the microcontroller voltage regulator V1 is active.
To avoid any unexpected shut-down of the application by the UJA1061, the temperature protection will not switch off any part of the UJA1061 or activate a defined system stop of its own accord. A too-high temperature only generates an interrupt to the microcontroller, if enabled, and the corresponding status bit is set. The microcontroller can now decide whether to switch off parts of the UJA1061 in order to decrease the chip temperature.

6.13 SPI interface

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller and supports multi-slave and multi-master operation. The SPI is configured for full duplex data transfer; while new control data is shifted-in, status information is automatically returned. All registers provide a read-only access option. Thus all status bits can be read back by the application at any time.

The SPI interface with a data rate up to 2 Mbit/s provides four interface signals, including chip select (see Fig.13).

Any bit-sampling is performed with the falling clock edge and the data is shifted with the rising clock edge.

All SPI interface signals are derived from V1 in order to avoid problems with reversed supplies.

Most of the registers are only accessible (read and/or write) during Normal mode or Standby mode. Some other registers, needed for watchdog initialization and entering special modes, are only accessible during the Start-up and/or Restart mode.

The following SPI interface signals are implemented:

- SCS - SPI chip select; active LOW
- SCK - SPI clock; default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output; floating when pin SCS is HIGH.

The SPI interface can be accessed only when pin RSTN (input channel of RSTN) is set HIGH.

Possible SPI failures are:

- SPI clock count failure (wrong number of clock cycles during one SPI access). Within one SCS cycle only 16 clock periods are allowed. Any deviation from the 16 clock cycles results in an SPI failure interrupt, if enabled. The access is ignored by the UJA1061. In Start-up and Restart mode, a reset is forced instead of an interrupt
- Wrong mode register code. The following events result in an immediate system reset without interrupt according to the state diagram of the system controller
  - Mode other than initializing Normal mode selected within mode register in Start-up or Restart mode
  - Initializing Flash mode outside of Start-up mode or within Start-up mode without previous Flash sequence
  - Bit WDD set in the mode register; this bit may only be set via the special mode register
  - Illegal watchdog period coding, see Section 6.14.2.
- Illegal mode register code during Normal or Standby mode of the UJA1061.

With a read-only access to the system status register or the system diagnosis register which, with the mode register, share the same SPI address, the data written to the mode register is ‘don’t care’ and is ignored. Reading these two system registers is allowed at any time independent of watchdog window cycles.

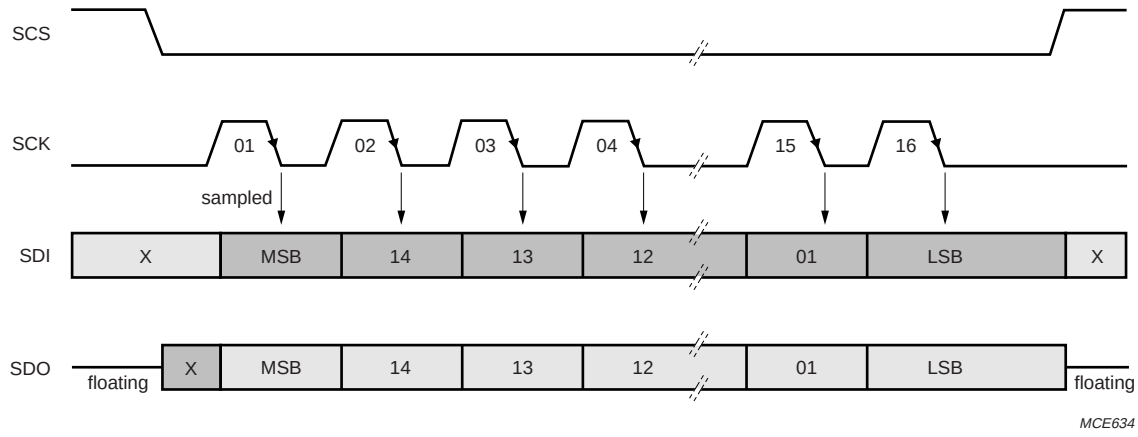


Fig.13 SPI timing protocol.

6.14 SPI register mapping

Any control bit which might be set in software is readable by the application. This allows software debugging as well as control algorithms to be implemented. There is also a read-only access possible without actively writing to an SPI register.

The following constraints are implemented in the register mapping:

- The number of clock cycles during one SPI access has to be 16
- Watchdog period and mode setting is performed within the same access cycle; this allows a mode change of the UJA1061 with simultaneously changing the period and the mode of the watchdog
- Each register carries only 12 functional bits; 4 bits are used for register selection and read/write definition.

6.14.1 Register overview

Since the SPI interface is bidirectional, each write access automatically implies a register read access to one of the internal registers, see Table 2. In order to allow a register to be read without writing data to it, a read-only feature is incorporated.

A 4-bit header defines any SPI access to one of the registers. The first two bits, address bits A1 and A0, define the register address. These are followed by the read register select bit RRS that defines the feedback register for this access. The fourth bit RO allows a ‘read only’ access to one of the feedback registers.

Depending on the mode, some registers can be written to and/or read from, and some not. During the first watchdog initialization phase, directly after the first battery connection, the special mode bits register can be set only once. After this special mode register access, or any other access to the UJA1061, these bits cannot be accessed again. This special mode register is used for entering the Software Development mode. The Software Development mode bit SDM, present in the system configuration register, can be read out and also reset all the time in Normal operating mode and Standby mode.

The UJA1061 has two 12-bit General Purpose registers with no prescribed bit definition. During power-up the bits of General Purpose register 0 (GP0) will be loaded with a ‘Device Identification Code’ consisting of the SBC type and SBC version. The bits of General Purpose register 1 (GP1) will be reset after power-up. All bits of GP0 and GP1 cannot be changed any more by the UJA1061, with the exception of bit 11 of register GP0 which indicates whether the content of register GP0 is the ‘Device Identification Code’ (bit 11 = logic 1), or used already as an extra register by the microcontroller (bit 11 = logic 0). Only the application microcontroller can change the other 23 bits during the Start-up mode, Restart mode or Flash Programming mode. The microcontroller can read these two registers all the time. The purpose of the General Purpose register is to give the microcontroller the possibility of storing certain system status information that cannot be held within the microcontroller memory. This is very useful for applications making use of the Sleep mode (unpowered microcontroller) saving important data bits for the next operating cycle.

Furthermore these two registers can be used for enhanced system diagnosis and fail-safe features. If, for example, a fault in the memory of the microcontroller always causes the same reset due to a software crash, the microcontroller can count these events and write the corresponding information into these register bits. The reset source register bits offer the corresponding information about the root cause of the problem. Thus, the microcontroller can take action depending on the number of identical resets and so prevent an ECU from permanent system crash situations consuming permanently high power. Thus, the general purpose registers offer a kind of ‘non volatile memory’ to the microcontroller since the UJA1061 is always powered from the battery line, independently from the supply of the microcontroller which could possibly be without power from time to time.

Table 2 Register overview

ADDRESS (BINARY BITS 15, 14)	MODE	WRITE ACCESS	NAME	READ ACCESS			
				READ REGISTER SELECT BIT (RRS) = 0	NAME	READ REGISTER SELECT BIT (RRS) = 1	NAME
00	all	Mode register	MOD	System Status register	STAT	System Diagnosis register	DIAG
01	Normal operating mode; Standby mode	Interrupt Enable register	IE	Interrupt Enable Feedback register	IEF	Interrupt register	INT
	Start-up mode due to Power-on	Special Mode register	SPE				
	Start-up mode; no power on; Restart mode; Flash Programming mode	no write access possible	–				
10	Normal operating mode; Standby mode	system configuration register	SC	System Configuration Feedback register	SCF	General Purpose Feedback register 0	GPF0
	Start-up mode; Restart mode; Flash Programming mode	general purpose register 0	GP0				
11	Normal operating model; Standby mode	physical layer control register	PLC	Physical Layer Control Feedback register	PLCF	General Purpose Feedback register 1	GPF1
	Start-up; mode Restart mode; Flash Programming mode	general purpose register 1	GP1				

6.14.2 MODE REGISTER

The mode register has cyclic access during system operation. Here the watchdog is defined and re-triggered as well as the current mode of operation is selected. Furthermore the global enable output (bit EN) as well as the Software Development Mode (bit SDM) control bit are defined here. Depending on the system requirements, the CAN physical medium can be activated with any access to the CAN Mode bit (CM).

This register has to be written during system start-up within 256 ms after RSTN has become released (HIGH-level on RSTN). Any write access is checked for proper watchdog and system mode coding. If an illegal code is detected, this access is ignored by the UJA1061 and a system reset is forced according to the state diagram of the system controller.

Table 3 MOD - Mode register (address 00) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION			
15, 14	A1, A0	register address	00	select Mode register			
13	RRS	Read Register Select	1	read System Diagnosis register (DIAG)			
			0	read System Status register (STAT)			
12	RO	Read Only	1	read selected register without writing to Mode register			
			0	read selected register and write to Mode register			
11 to 6	NWP[5:0]	Nominal Watchdog Period		Normal operating mode (ms)	Standby mode (ms)	Flash Programming mode (ms)	Sleep mode (ms)
			001001	4	20	20	160
			001100	8	40	40	320
			010010	16	80	80	640
			010100	32	160	160	1024
			011011	40	320	320	2048
			100100	48	640	640	3072
			101101	56	1024	1024	4096
			110011	64	2048	2048	6144
			110101	72	4096	4096	8192
			110110	80	OFF(1)	8192	OFF(1)
5 to 3	OM[2:0]	Operating Mode	001	Normal operating mode			
			010	Standby mode			
			100	Sleep mode			
			101	initializing Normal mode			
			111	Flash Programming mode; note 2			
			011	initializing Flash mode 1; note 3			
2	SDM	Software Development Mode(4)	1	no watchdog reset; no interrupt monitoring; no reset monitoring; no transitions to Fail-safe mode; Fail-safe is entered only with a V1-undervoltage condition longer than 256 ms			
			0	Normal watchdog, interrupt, reset monitoring and fail-safe behaviour			

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
1	EN	Enable	1	EN output pin HIGH
			0	EN output pin LOW
0	CM	CAN Mode	1	Active mode selected; CAN active; transmissions possible
			0	Auto mode selected; CAN is allowed to fall into low power

Notes

1. If the watchdog is triggered with the watchdog OFF code while the UJA1061 is in Standby mode or while the UJA1061 enters Standby mode, the V1 current monitoring function stays disabled for a period of time equal to the previous or the default (4096 ms) watchdog period. The default period is selected if the Standby mode is entered directly with Watchdog OFF mode. After that period, the current monitoring is enabled. Then the behaviour of the UJA1061 upon a too-high V1 current depends on the setting of the V1CMC bit within the System Configuration register. If this bit is set (reset option), a too-high V1 current causes an immediate reset. If this bit is not set (Watchdog Restart option), the watchdog starts a new period without the possibility to be disabled except by being triggered again with the watchdog OFF code. If the watchdog OFF code is chosen, the watchdog time-out interrupt has no function.
2. The Flash Programming mode can be entered only with the consecutive watchdog service sequence ‘Normal operating mode/Flash Programming mode/Normal operating mode/Flash Programming mode’ using multiple watchdog period times because access to this register is allowed only while the watchdog is open for write access. Now the UJA1061 forces a system reset and enters Start-up mode in order to prepare the microcontroller for Flash memory download. Also the software has to use the Initializing Flash mode within 256 ms in order to enter the Flash Programming mode of the UJA1061 successfully.
3. The watchdog is immediately disabled entering Sleep mode with watchdog OFF behaviour selected because pin RSTN is pulled LOW immediately with the mode change.
4. Setting of bit SDM is possible only via the Special Mode register and only once after supplying the UJA1061 the first time with BAT42 voltage. Access of the special mode register has to be executed before the watchdog is initialized, that is, before the first write to the mode register. Resetting is possible at any time via the mode register. A set SDM flag disables all reset events caused by the UJA1061 during Normal operating mode (except for wrong mode register code resets), disables the interrupt time monitoring function during Normal operating mode, the watchdog initialization time, the reset monitoring and the transitions to Fail-safe mode with the exception of a V1-undervoltage longer than 256 ms. This bit is set automatically if pin TEST is forced to 7 V or higher during power-on of the UJA1061 (Software Development mode or forced Normal mode). Watchdog trigger failures resulting only in the interrupt if enabled in the Interrupt Enable register.

6.14.3 SYSTEM STATUS REGISTER

This register allows status information to be read-back from the UJA1061.

Table 4 STAT - System Status register (address 00) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	00	read System Status register (STAT)
13	RRS	Read Register Select	0	
12	RO	Read Only	1	read System Status register without writing to Mode register
			0	read System Status register and write to Mode register
11 to 8	RSS[3:0]	Reset Source(1)	0000	Power-on reset; first connection of BAT42 or BAT42 below power-on voltage threshold **or** RSTN was forced LOW externally
			0001	cyclic wake-up out of Sleep mode
			0010	low V1 supply; V1 has dropped below the reset threshold
			0011	V1 current above threshold within Standby mode of the UJA1061 while watchdog OFF behaviour was selected and the RESET option is selected within the System Configuration register
			0100	V3 voltage is down due to short-circuit occurring during Sleep mode
			0101	reserved
			0110	UJA1061 ready to enter Flash Programming mode
			0111	wake-up event via CAN while reset behaviour selected **or** during Sleep mode
			1000	wake-up event via LIN while reset behaviour selected **or** during Sleep mode
			1001	wake-up event via WAKE while reset behaviour selected **or** during Sleep mode
			1010	wake-up event out of Fail-safe mode
			1011	watchdog overflow (Normal operating mode)/time-out (Standby mode/Flash mode); trigger too late
			1100	watchdog not initialized in time; 256 ms exceeded
			1101	watchdog triggered too early; window missed
			1110	illegal Mode Register Code
			1111	interrupt not served in time (within 256 ms)
7	–	reserved	0	reserved for future use; in order to stay compatible with future silicon versions using this bit, software should ignore this bit value
6	LWS	Level Wake Status	1	pin WAKE is above the threshold
			0	pin WAKE is below the threshold
5	–	reserved	0	reserved for future use; in order to stay compatible with future silicon versions using this bit, software should ignore this bit value

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
4	EWS	Edge Wake Status	1	pin WAKE negative edge event detected; cleared upon read
			0	pin WAKE no edge detected
3	TWS	Temperature Warning Status	1	chip temperature exceeds the warning limit
			0	chip temperature is below the warning limit
2	SDMS	Software Development Mode Status	1	no watchdog reset; no interrupt monitoring; no reset monitoring; no transitions to Fail-safe mode; only during a V1 undervoltage longer than 256 ms
			0	normal watchdog interrupt, reset monitoring and fail-safe behaviour
1	EN	Enable status	1	pin EN output activated, a (V1-related) HIGH level is driven
			0	pin EN output released a LOW level is driven
0	PWONS	Power-on reset Status	1	Power-on reset; first connection of BAT42 **or** BAT42 below power-on voltage threshold; cleared after a successfully-entered Normal operating mode or Flash Programming mode
			0	No Power-on reset

Note

1. The Reset Source register is updated with each reset event and not cleared. The last reset event is captured.

6.14.4 SYSTEM DIAGNOSIS REGISTER

This register allows status information to be read back from the UJA1061.

Table 5 DIAG - System Diagnosis register (address 00) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	00	read system diagnosis register (DIAG)
13	RRS	Read Register Select	1	
12	RO	Read Only	1	read System Diagnosis register without writing to Mode register
			0	read System Diagnosis register and write to Mode register
11	GSD	Ground Shift Diagnosis	1	system GND is worse than selected threshold
			0	system GND is better than selected threshold
10 to 7	CANFD	CAN failure diagnosis	1111	TXDC is clamped dominant
			1110	RXDC is clamped dominant
			1101	RXDC is clamped recessive
			1100	BUS is clamped dominant (dual failure situation)
			1011	BUS is clamped recessive (dual failure situation)
			1010	reserved
			1001	CANH is shorted to CANL (failure case 7)
			1000	CANL is shorted to V_{CC} (failure case 6a)
			0111	CANL is shorted to VBAT (failure case 6)
			0110	CANH is shorted to GND (failure case 5)
			0101	CANL is shorted to GND (failure case 4)
			0100	CANH is shorted to V_{CC} (failure case 3a)
			0011	CANH is shorted to VBAT (failure case 3)
			0010	CANL wire is interrupted (failure case 2)
			0001	CANH wire is interrupted (failure case 1)
			0000	no failure
6, 5	LINFD	LIN failure diagnosis	11	TXDL is clamped dominant
			10	LIN is shorted to GND (dominant clamped)
			01	LIN is shorted to VBAT (recessive clamped)
			00	no failure
4	V3D	V3 diagnosis	1	OK; after a detected short-circuit; the bit is set again with activating V3 via the V3C control bits
			0	fail; V3 is disabled due to a short circuit situation
3	V2D	V2 diagnosis	1	OK; note 1
			0	fail; V2 is disabled due to a short-circuit situation
2	V1D	V1 diagnosis	1	OK; V1 always above RAM retention threshold since last read access
			0	fail; V1 was below RAM retention threshold since last read access; bit is set again with read access

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
1, 0	CANMD	CAN mode diagnosis	11	CAN is within Active mode
			10	CAN is within On-line mode
			01	CAN is within Selective Sleep mode
			00	CAN is within Off-line mode

Note

1. V2D becomes cleared upon a short-circuit situation on V2 (overload) while V2 is active. In parallel, V2 becomes disabled in order to protect the system from high current consumption. V2 will be restarted setting V2D with the following events:
   a) By setting CAN mode
   b) During a HIGH-to-LOW transition of the CTC bit (Physical Layer Control register) activating the CAN-transmitter
   c) During a transition from Off-line into On-line
   d) During a transition from Off-line into Selective Sleep mode.

6.14.5 INTERRUPT ENABLE REGISTER

This register, which can be written to only in Normal and Standby modes, allows setting/enabling certain interrupt events for the UJA1061

Table 6 IE - Interrupt Enable register (address 01) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	01	read Interrupt Enable register
13	RRS	Read Register Select	1	read the Interrupt Register (INT)
			0	read the Interrupt Enable Feedback register (IEF)
12	RO	Read Only	1	read the register selected by RRS without writing to Interrupt Enable register
			0	read the register selected by RRS and write to Interrupt Enable register
11	WTIE	Watchdog Time-out Interrupt Enable(1)	1	a watchdog overflow during Standby causes an interrupt instead of a reset event
			0	no interrupt forced upon overflow; a reset is forced instead
10	OTIE	Over-Temperature Interrupt Enable	1	exceeding or dropping below the temperature warning limit causes an interrupt
			0	no interrupt forced
9	GSIE	Ground Shift Interrupt Enable	1	exceeding or dropping below the GND shift limit causes an interrupt
			0	no interrupt forced
8	SPIFIE	SPI clock count Failure Interrupt Enable	1	wrong number of CLK cycles (more than, or less than 16) forces an interrupt; within Start-up and Restart mode, a reset is performed instead of an interrupt
			0	no interrupt forced; SPI access is ignored if wrong number of cycles is applied (more than, or less than 16)
7	BATFIE	BAT Failure Interrupt Enable	1	falling edge at SENSE forces an interrupt
			0	no interrupt forced
6	V2V3FIE	V2/V3 Failure Interrupt Enable(2)	1	detection of a short-circuit at V2 or V3 forces an interrupt
			0	no interrupt forced
5	CANFIE	CAN Failure Interrupt Enable	1	any change of the CAN Failure status forces an interrupt
			0	no interrupt forced
4	LINFIE	LIN Failure Interrupt Enable	1	any change of the LIN Failure status forces an interrupt
			0	no interrupt forced
3	WIE	WAKE Interrupt Enable	1	a negative edge at WAKE generates an interrupt in Normal, Flash or Standby mode
			0	a negative edge at WAKE generates a reset in Standby mode
2	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
1	CANIE	CAN Interrupt Enable	1	CAN-bus event results in a wake-up interrupt
			0	CAN-bus event results in a reset
0	LINIE	LIN Interrupt Enable	1	LIN-bus event results in a wake-up interrupt
			0	LIN-bus event results in a reset

Notes

1. This flag is cleared automatically upon each overflow event. It has to be set in software each time the interrupt behaviour is required (fail-safe behaviour).
2. If V2 or V3 is shut down due to a short-circuit, or activation of V2 or V3 fails due to a short-circuit, the interrupt is forced. V2 can be activated again by clearing CTC (CAN Transmitter Control), setting CAN mode or via a wake-up event on CAN. V3 can be activated setting bit V3C to a value other than ‘00’.

6.14.6 Interrupt Enable Feedback register

This register allows the current setting of the interrupt enable bits to be read back.

Table 7 IEF - Interrupt Enable Feedback register (address 01) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	01	read Interrupt Enable Feedback register
13	RRS	Read Register Select	0	
12	RO	Read Only	1	read the Interrupt Enable Feedback register without writing to Interrupt Enable register
			0	read the Interrupt Enable Feedback register and write to Interrupt Enable (previous content is reflected during read)
11	WTIE	Watchdog Time-out Interrupt Enable	1	a watchdog overflow during Standby mode causes an interrupt instead of a reset
			0	no interrupt forced
10	OTIE	Over-temperature Interrupt Enable	1	exceeding or dropping below the temperature warning limit causes an interrupt
			0	no interrupt forced
9	GSIE	Ground Shift Interrupt Enable	1	exceeding or dropping below the GND shift limit causes an interrupt
			0	no interrupt forced
8	SPIFIE	SPI clock count Failure Interrupt Enable	1	wrong number of CLK cycles (more than, or less than 16) forces an interrupt; within Start-up and Restart mode, a reset is performed instead of an interrupt
			0	no interrupt forced, SPI access simply ignored if wrong number of cycles is applied (more than, or less than 16)
7	BATFIE	BAT Failure Interrupt Enable	1	falling edge at SENSE forces an interrupt
			0	no interrupt forced
6	V2V3FIE	V2/V3 Failure Interrupt Enable	1	detection of a short circuit at V2 or V3 forces an interrupt
			0	no interrupt forced
5	CANFIE	CAN failure Interrupt Enable	1	any change of the CAN failure status forces an interrupt
			0	no interrupt forced
4	LINFIE	LIN Failure Interrupt Enable	1	any change of the LIN failure status forces an interrupt
			0	no interrupt forced
3	WIE	Wake-up Interrupt Enable	1	a negative edge at WAKE generates an interrupt in Normal, Flash or Standby modes
			0	a negative edge at WAKE generates a reset in Standby mode
2	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
1	CANIE	CAN interrupt enable	1	CAN-bus event results in a wake-up interrupt
			0	CAN-bus event results in a reset
0	LINIE	LIN interrupt enable	1	LIN-bus event results in a wake-up interrupt
			0	LIN-bus event results in a reset

6.14.7 INTERRUPT REGISTER

This register allows the cause of an interrupt event to be read. The register is cleared upon read access and upon any reset event. Hardware makes sure that no interrupt event is lost in case there is a new interrupt forced while reading the register. The INTN pin is forced HIGH after reading the interrupt register for a defined period of time in order to make sure that there is always an edge event guaranteed at the INTN pin.

The interrupts can be classified into two classes:

- One in which the UJA1061 must react immediately due to timing-sensitive interrupts (SPI Clock CAN failure which needs an immediate resend of a new SPI command, and BAT failure which needs immediate saving of critical data into the non-volatile memory)
- One which does not need an immediate reaction (OVERTEMP, Ground Shift, CAN and LIN failures, V2 and V3 failures and the wake-ups via CAN, LIN and WAKE. These interrupts will be signalled in Normal Mode and Flash Mode via the INTN pin to the microcontroller once per watchdog period (maximum).

Table 8 INT - Interrupt register (address 01) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	01	read Interrupt register (INT)
13	RRS	Read Register Select	1	
12	RO	Read Only	1	read the Interrupt register without writing to Interrupt Enable register
			0	read the Interrupt register and write to Interrupt Enable register
11	WTI	Watchdog Time-out Interrupt	1	a watchdog overflow has occurred during Standby mode
			0	no interrupt
10	OTI	Over-Temperature Interrupt	1	the temperature warning limit has been exceeded or has dropped below
			0	no interrupt
9	GSI	Ground Shift Interrupt	1	the GND shift limit has been exceeded or has dropped below
			0	no interrupt
8	SPIFI	SPI clock count Failure Interrupt	1	wrong number of CLK cycles (more than, or less than 16) during SPI access; within Start-up and Restart modes, a reset is performed instead of an interrupt
			0	no interrupt; SPI access is ignored if wrong number of cycles is applied (more than, or less than 16)
7	BATFI	BAT Failure Interrupt	1	falling edge at SENSE forces an interrupt
			0	no interrupt
6	V2V3FI	V2/V3 Failure Interrupt	1	short-circuit detected at V2 or V3 (details within system status register 1)
			0	no interrupt
5	CANFI	CAN Failure Interrupt	1	CAN failure status has changed
			0	no interrupt
4	LINFI	LIN Failure Interrupt	1	LIN failure status has changed
			0	no interrupt
3	WI	Wake-up Interrupt	1	a negative edge at WAKE has been detected
			0	no edge

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
2	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
1	CANI	CAN Wake-up Interrupt	1	there was a CAN-bus event resulting in a wake-up interrupt, if enabled
			0	no wake-up via CAN
0	LINI	LIN Wake-up Interrupt	1	there was a LIN-bus event resulting in a wake-up interrupt, if enabled
			0	no wake-up via LIN

6.14.8 SYSTEM CONFIGURATION REGISTER

This register, only accessible in Normal and Standby modes, allows the UJA1061 behaviour to be configured.

Table 9 SC - System Configuration register (address 10) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	10	select System Configuration register
13	RRS	Read Register Select	1	read the General Purpose Feedback register (GPF0)
			0	read the System Configuration Feedback register (SCF)
12	RO	Read Only	1	read register selected by RRS without writing to System Configuration register
			0	read register selected by RRS and write to System Configuration register
11	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
10	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
9	GSTHC	GND Shift Threshold Control	1	–1.5 V; exceeding this level forces an interrupt
			0	–0.75 V; exceeding this level forces an interrupt
8	RLC	Reset Length Control	1[1]	20 ms system reset is selected; default after power-up
			0	1 ms system reset is selected
7, 6	V3C	V3 Control	11	Cyclic mode 2; 350 µs ON/32 ms period
			10	Cyclic mode 1; 350 µs ON/16 ms period
			01	continuously ON
			00	OFF; also reset to 00 in Fail-safe mode, or after a negative edge has been detected at the external RSTN pin, or a short-circuit situation is detected at V3
5	V1RTHC	V1 Reset Threshold Control	1	the reduced V1 undervoltage threshold is selected
			0	the normal V1 undervoltage threshold is selected
4	V1CMC	V1 Current Monitor Control	1	an increasing V1 current causes a reset event if the watchdog was disabled during Standby mode
			0	an increasing V1 current just activates the watchdog again during Standby mode
3	WEN	WAKE Enable	1	wake-up functionality at WAKE pin enabled
			0	wake-up functionality at WAKE pin disabled
2	WSC	WAKE Sample Control	1	WAKE mode cyclic sample
			0	WAKE mode continuous sample
1	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
0	IC	INH control	1	INH/LIMP home pin HIGH
			0	INH/LIMP home pin floating

Note

1. For fail-safe reasons, this bit is set automatically when entering the Reset state.

6.14.9 System Configuration Feedback register

This register allows the settings within the Configuration register to be read back.

Table 10 SCF - System Configuration Feedback register (address 10) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	10	read System Configuration Feedback register (SCF)
13	RRS	Read Register Select	0	
12	RO	Read Only	1	read the System Configuration Feedback register without writing to the System Configuration register
			0	read the System Configuration Feedback register and write to the System Configuration register (previous content reflected)
11	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
10	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
9	GSTHC	GND Shift Threshold Control	1	–1.5 V; exceeding this level may force an interrupt
			0	–0.75 V; exceeding this level may force an interrupt
8	RLC	Reset Length Control	1	20 ms system reset is selected; default after power-up
			0	1 ms system reset is selected
7, 6	V3C	V3 Control	11	Cyclic mode 2; 350 µs ON/32 ms period
			10	Cyclic mode 1; 350 µs ON/16 ms period
			01	continuously ON
			00	OFF
5	V1RTHC	V1 Reset Threshold Control	1	the reduced V1 undervoltage threshold is selected
			0	the normal V1 undervoltage threshold is selected
4	V1CMC	V1 Current Monitor Control	1	an increasing V1 current causes a reset event if the watchdog was disabled
			0	an increasing V1 current just activates the watchdog again
3	WEN	WAKE Enable	1	wake-up functionality at WAKE pin enabled
			0	wake-up functionality at WAKE pin disabled
2	WSC	WAKE Sample Control	1	WAKE mode cyclic sample
			0	WAKE mode continuous sample
1	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
0	IC	INH control	1	INH pin HIGH
			0	INH pin floating

6.14.10 Physical Layer Control register

This register has write access only in Normal and Standby modes; it allows the CAN and the LIN physical layer to be configured.

Table 11 PLC - Physical Layer Control register (address 11) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	11	select Physical Layer Control register
13	RRS	Read Register Select	1	read the General Purpose Feedback register 1 (GPF1)
			0	read the Physical Layer Control Feedback register (PLCF)
12	RO	Read Only	1	read the register selected by RRS without writing to the Physical Layer Control register
			0	read the register selected by RRS and write to Physical Layer Control register
11	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
10	CPNC	CAN Partial Networking Control	1	allows Selective Sleep state to be entered; cleared whenever the UJA1061 enters On-line or Active mode
			0	no Selective Sleep mode allowed (default)
9	COTC	CAN Off-line Time Control	1	256 ms time until CAN falls into Off-line (400 ms after Wake-up)
			0	64 ms time until CAN falls into Off-line (400 ms after Wake-up)
8	CTC	CAN Transmitter Control	1[1]	CAN transmitter is disabled; allows setting ‘listen only’ behaviour; set also due to a detected short at V2 or a RXDC recessive or TXDC dominant clamping failure
			0	CAN transmitter is enabled
7	CRC	CAN Receiver Control	1[2]	TXD signal is forwarded to RXD during CAN transmitter OFF
			0	TXD signal is not forwarded to RXD during CAN transmitter OFF
6	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
5	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
4	LSC	LIN Slope Control	1	up to 10 kbit/s
			0	up to 20 kbit/s
3	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
2	L42C	LIN 42 V Control	1	LIN termination supplied out of BAT42
			0	LIN termination is always related to BAT14

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
1	LWEN	LIN Wake-up Enable	1	Wake-up via the LIN bus enabled
			0	Wake-up via the LIN bus disabled
0	LTC	LIN Transmitter Control	1	LIN transmitter is disabled; allows setting ‘listen only’ behaviour
			0	LIN transmitter is enabled

Notes

1. Setting this bit actively under software control after a detected short-circuit on V2 restarts V2.
2. Setting this bit allows a local self-test of the node without affecting the CAN bus wires. his bit should not be set during normal communication.

6.14.11 PHYSICAL LAYER CONTROL FEEDBACK REGISTER

This register allows the CAN and the LIN physical layer configuration to be read back.

Table 12 PLCF - Physical Layer Control Feedback register (address 11) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	10	read the Physical Layer Control Feedback register (PLCF)
13	RRS	Read Register Select	0	
12	RO	Read Only	1	read the Physical Layer Control Feedback register without writing to Physical Layer Control register
			0	read the Physical Layer Control Feedback register and write to Physical Layer Control register (previous setting will be reflected)
11	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
10	CPCN	CAN Partial Networking Control	1	allows Selective Sleep state to be entered; cleared whenever the UJA1061 enters On-line or Active mode
			0	no Selective Sleep mode allowed (default)
9	COTC	CAN Off-line Time Control	1	256 ms time until CAN falls into Off-line (400 ms after Wake-up)
			0	64 ms time until CAN falls into Off-line (400 ms after Wake-up)
8	CTC	CAN Transmitter Control	1	CAN transmitter is disabled; allows setting ‘listen only’ behaviour; set also due to a detected short at V2
			0	CAN transmitter is enabled
7	CRC	CAN Receiver Control	1	TXD signal is forwarded to RXD during CAN transmitter OFF
			0	TXD signal is not forwarded to RXD during CAN transmitter OFF
6	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
5	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
4	LSC	LIN Slope Control	1	up to 10 kbit/s
			0	up to 20 kbit/s
3	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
2	L42C	LIN 42 V Control	1	LIN termination supplied out of BAT42
			0	LIN termination is always related to BAT14

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
1	LWEN	LIN Wake-up Enable	1	Wake-up via the LIN bus enabled
			0	Wake-up via the LIN bus disabled
0	LTC	LIN Transmitter Control	1	LIN transmitter is disabled; allows setting ‘listen only’ behaviour
			0	LIN transmitter is enabled

6.14.12 SPECIAL MODE REGISTER

This register is only accessible in Start-up mode after the first battery connection (BAT42) and allows special UJA1061 modes to be written only once. Another write access is possible only by removing the power from pin BAT42.

Table 13 SPE - Special Mode register (address 01) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	01	select Special Mode register
13	RRS	Read Register Select	0	read the Interrupt Enable Feedback register (IEF)
			1	read the Interrupt Feedback register (INT)
12	RO	Read Only	1	read the register selected by RRS without writing to the Special Mode register
			0	read the register selected by RRS and write to the Special Mode register
11	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
10	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1
9	ISDM	Initialize Software Development Mode	1	no watchdog reset, no interrupt monitoring, no reset monitoring, no transitions to Fail-safe mode, only during a V1 undervoltage longer than 256 ms; note 1
			0	normal watchdog interrupt, reset monitoring and fail-safe behaviour
8	ERREM	Error-pin Emulation Mode	1	pin EN reflects the content of the CANFD register: logic 1 if CANFD = 0000 (no error) logic 0 if CANFD is not 0000 (error)
			0	pin EN behaves as an enable pin (see Section 6.5.2)
7	LHM	Limp Home Mode	1	IC-bit within System Configuration register is set entering Fail-safe mode (‘limp home’ function)
			0	IC-bit is cleared within System Configuration register when entering Fail-safe mode (INH function)
6 to 0	–	reserved	0	reserved for future use; should always be set to logic 0 in order to secure compatibility with future functions which will be activated by a logic 1

Note

1. Setting of ISDM is possible only via writing to the Special Mode register and is possible only once after supplying the BAT42 voltage to the UJA1061 for the first time. The access of the Special Mode register has to be executed before the watchdog is initialized, that is before the first writing to the Mode register. Resetting is possible at any time via the Mode register. A set ISDM flag disables all reset events caused by the UJA1061 during Normal mode (with the exception of wrong mode register code resets), disables the interrupt time monitoring function during Normal mode, and the Watchdog initialization time, the reset monitoring and the transitions to Fail Safe with the exception of a V1-undervoltage longer than 256 ms. This bit is set automatically if pin TEST is forced to 7 V or higher during power-on of the UJA1061 (Watchdog OFF Test mode or Device Level Test mode). Watchdog trigger failures result only in the interrupt.

6.14.13 General Purpose registers

General Purpose registers 0 and 1 have write access in Start-up, Restart mode and Flash mode only to allow general bits to be written to the UJA1061.

Table 14 GP0 - General Purpose register 0 (address 10) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	10	read the general purpose feedback register 0 (GPF0)
13	RRS	Read Register Select	1	read the General Purpose Feedback register 0 (GPF0)
			0	read the System Configuration Feedback register (SCF)
12	RO	Read Only	1	read the register selected by RRS without writing to the General Purpose register 0 (GP0)
			0	read the register selected by RRS and write to the General Purpose register 0 (GP0)
11 to 0	GP0	General Purpose bits	1	the relevant General Purpose bit has been set; note 1
			0	the relevant General Purpose bit has been cleared; note 1

Note

1. During power-up, the bits of the General Purpose register 0 (GP0) will be loaded with a ‘Device Identification Code’ consisting of the SBC type and SBC version. Bit 11 of GP0 will reflect a logic 0 indicating the content of this register to be the ‘Device Identification Code’ after Power-on of the SBC. Once written to this register, bit 11 will be set to a permanent logic 1 indicating that the device code has been overwritten with application-specific information. Bit 11 cannot be reset any more with software control. Bit 11 will be cleared again with the next Power-on condition at pin BAT42 with reloading the device code into GP0.

Table 15 GP1 - General Purpose register 1 (address 11) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	11	select General Purpose register 1
13	RRS	Read Register Select	1	read the General Purpose Feedback register 1 (GPF1)
			0	read the Physical Layer Control Feedback register 1 (PLCF)
12	RO	Read Only	1	read the register selected by RRS without writing to the General Purpose register 1 (GP1)
			0	read the register selected by RRS and write to the general purpose register (GP1)
11 to 0	GP0	General Purpose bits	1	the relevant General Purpose bit has been set
			0	the relevant General Purpose bit has been cleared

6.14.14 General Purpose Feedback registers

General Purpose Feedback registers 0 and 1 allow the general bits to be read from the UJA1061.

Table 16 GPF0 - General Purpose Feedback register 0 (address 10) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	10	read general purpose feedback register 0 (GPF0)
13	RRS	Read Register Select	1	
12	RO	Read Only	1	read the General Purpose Feedback register 0 (GPF0) without writing to the Physical Layer Control register or the General Purpose register 0
			0	read the general purpose feedback register 0 and write to the system configuration register or the general purpose register 0
11 to 0	GP0	General Purpose bits	1	the relevant General Purpose bit has been set; note 1
			0	the relevant General Purpose bit has been cleared; note 1

Note

1. During power-up, the bits of the General Purpose register 0 (GP0) will be loaded with a ‘Device Identification Code’ consisting of the SBC type and SBC version. Bit 11 of GP0 will reflect a logic 0 indicating the content of this register to be the ‘Device Identification Code’ after Power-on of the SBC. Once written to this register, bit 11 will be set to a permanent logic 1 indicating that the device code has been overwritten with application-specific information. Bit 11 cannot be reset any more with software control. Bit 11 will be cleared again with the next Power-on condition at pin BAT42 with reloading the device code into GP0.

Table 17 GP1 - General Purpose Feedback register 1 (address 11) bit description

BIT	SYMBOL	DESCRIPTION	VALUE	FUNCTION
15, 14	A1, A0	register address	1	read general purpose feedback register 1 (GPF1)
13	RRS	Read Register Select	1	
12	RO	Read Only	1	read the General Purpose Feedback register 1 (GPF1) without writing to the Physical Layer Control register or the General Purpose register 1
			0	read the General Purpose Feedback register 1 and write to the Physical Layer Control register or the General Purpose register 1
11 to 0	GP1	General Purpose bits	1	the relevant General Purpose bit has been set
			0	the relevant General Purpose bit has been cleared

6.15 Register configurations at reset

Many register contents are unaffected by an external reset event (edge at pin RSTN), for example, the CAN physical layer register will not reset the bus failure information. Since an externally-forced reset event sets the UJA1061 into start-up, the same behaviour will occur as in Start-up mode with the exception of the V3 configuration flag V3C and the INH control flags (IC1 and IC2) in the system configuration register.

Table 18 Mode register: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
NWP	Nominal Watchdog Period	256 ms start-up	256 ms start-up	256 ms start-up
OM	Operating Mode	wait on init	wait on init	wait on init
SDM	Software Development Mode	0	0	0
EN	ENable	0 (EN = LOW)	0 (EN = LOW)	0 (EN = LOW)
CM	CAN Mode	0 (auto)	0 (auto)	0 (auto)

Table 19 System status register: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET(1)	RESTART(1)
RSS	Reset Source Status	0000	0001 or 0010 or 0011 or 0100 or 0111 or 1000 or 1001 or 1010 or 1011 or 1101 or 1110 or 1111	0000 or 0110 or 1100 or 1110
LWS	Level Wake Status	0	no change	no change
EWS	Edge Wake Status	0	no change	no change
TWS	Temperature Warning Status	0	actual status	actual status
SDMS	Software Development Mode Status	0	no change	no change
ENS	Enable Status	0 (EN = LOW)	0 (EN = LOW)	0 (EN = LOW)
PWONS	Power-on Status	1	0	0

Note

1. Depends on history.

Table 20 System diagnosis register: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
GSD	Ground Shift Diagnosis	0 (OK)	actual status	actual status
CANFD	CAN Failure Diagnosis	0000	actual status	actual status
LINFD	LIN Failure Diagnosis	00	actual status	actual status
V3D	V3 Diagnosis	1 (OK)	actual status	actual status
V2D	V2 Diagnosis	1 (OK)	actual status	actual status
V1D	V1 Diagnosis	1 (OK)	actual status	actual status
CANMD	CAN Mode Diagnosis	00 (Off-line)	actual status	actual status

Table 21 Interrupt enable and interrupt enable feedback register: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
All	all flags	0 (interrupt disabled)	no change	no change

Interrupt register: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
All	all flags	0 (no interrupt)	0 (no interrupt)	0 (no interrupt)

Table 22 System configuration and system configuration feedback registers: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
GSTHC	GND Shift level Threshold Control	0 (–0.75 V)	no change	no change
RLC	Reset Length Control	1 (long)	no change	1 (long)
V3C	V3 Control	00 (off)	no change/00 (off) at external reset	no change
V1RTC	V1 Reset Threshold Control	0 (normal)	no change	0 (normal)
V1CMC	V1 Current Monitor Control	0 (no reset)	no change	no change
WEN	Wake Enable	1 (enabled)	no change	no change
WSC	Wake Sample Control	0 (control)	no change	no change
IC	INH Control	0 (floating)	0 (floating) if external reset or at V1 undervoltage	0 (floating)

Table 23 Physical layer control and physical layer control feedback registers: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
CPNC	CAN Partial Networking Control	0 (no control)	no change	no change
COTC	CAN Off-line Time Control	1	no change	no change
CTC	CAN Transmitter Control	0 (on)	no change	no change
CRC	CAN Receiver Control	0 (RXDC represents CAN-bus signals)	no change	no change
LSC	LIN Slope Control	0 (20 kbit/s)	no change	no change
L42C	LIN 42 V control	0 (BAT14)	no change	no change
LWRC	LIN Wake-up Reset Control	1 (enabled)	no change	no change
LTC	LIN Transmitter Control	0 (transmitter on)	no change	no change

Table 24 Special mode register: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
ISDM	Initial Software Development Mode	0 (no)	0 (no change)	0 (no change)
ERREM	Error pin emulation mode	0 (no)	no change	no change
LHM	Limp Home Mode	0 (no)	0 (no change)	0 (no change)

Table 25 General purpose and general purpose feedback register 0: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
GP0 11	general purpose bit 11: 1 for SBC identity; 0 for general user purpose	0	1	1
GP0 10 to 7	general purpose bits 10 to 7 (version)	0011 (N1C)	no change	no change
GP0 6 to 0	general purpose bits 6 to 0 (SBC type)	0000001 (UJA1061)	no change	no change

Table 26 General purpose and general purpose feedback register 1: status at reset

SYMBOL	NAME	POWER-ON	START-UP/ EXTERNAL RESET	RESTART
GP1	general purpose bits	0	no change	no change

6.16 Test modes

6.16.1 SOFTWARE DEVELOPMENT MODE

The Software Development mode is intended to support software developers, writing and pre-testing the application software without working around the watchdog triggering and without unwanted jumps to Fail-safe mode. This allows easy software development and debugging without forcing unintended reset events. Instead of resets caused by watchdog overflows, window missing, interrupt time-out or exceeded start-up time an interrupt will be forced instead of a reset. Once this mode is set, any watchdog trigger failure will not result in a reset, only in an interrupt, if enabled. Nevertheless the reset source information and interrupt information continues to be provided to the software as if there was a real reset event. Furthermore, the interrupt monitoring, forcing a LOW signal at pin RSTN if not serving the interrupt in time, is disabled too. Also the watchdog initialization time monitoring and reset monitoring have been disabled.Thus the software can already trigger the watchdog as intended for the final software version and any watchdog interrupt gives an indication about pending watchdog trigger problems. Once there are no further unwanted interrupts, the watchdog can be used as intended.

In addition to the disabling of the watchdog activity, the interrupt monitoring and the reset monitoring, any transition to Fail-safe mode is disabled; the UJA1061 then stays in the mode in which the problem occurred. Transitions to Restart mode are still possible, but not to Fail-safe mode. A V1 undervoltage of more than 256 ms is the only exception that results in entering Fail-safe mode and this is in order is to protect the UJA1061.

The Software Development mode can be used also for testing and/or measuring many parameters/mode changes during the pretest and final test programs.

For fail-safe reasons, the Software Development mode can be activated by setting the ISDM bit via the Special Mode register. This mode can be set only once after a first battery connection before the watchdog is initialized, this means within the 256 ms start-up period and before the first SPI write-access to any other register. A second possibility to enter this mode is a HIGH level (7 to 8 V) at pin TEST before the battery is applied to BAT42. Leaving this development mode and entering the normal operating behaviour is executed after disabling the SDM bit at any time during a write-access to the mode register. It should be noted that the SDM bit has to confirm the Software Development mode with each Mode Register access, even if the TEST pin is pulled to a voltage higher than (7 to 8) V. Entering the Software Development mode again is possible only by disconnection of the battery supply (BAT42) thus forcing a new power-on period for the UJA1061.

The watchdog behaviour within Standby and Sleep mode is not affected by the SDM bit. This allows the cyclic wake-up behaviour to be evaluated during the Standby or Sleep mode of the UJA1061.

6.16.2 Forced Normal mode

For system evaluation purposes the UJA1061 contains the Forced Normal mode. During this test the UJA1061 operates in Normal mode with disabled watchdog. All the voltage regulators are switched ON. The CAN-transceiver operates in Active and Automatic Fault-tolerant mode. The LIN-transceiver operates in Active mode and this mode can be activated only with a stable HIGH-level (12 V) at pin TEST during the first battery connection. Leaving this mode and entering the Normal operating mode will be executed after releasing the TEST pin (level at 0 V). Entering the Forced Normal mode again is possible only by disconnection of the battery supply (BAT42) thus forcing a new power-on period for the UJA1061.

The behaviour of the UJA1061 in Forced Normal mode is as follows:

- SPI access (writing and reading) is blocked
- Watchdog is disabled
- Interrupt Monitoring is disabled
- Reset Monitoring is disabled
- UJA1061 is held in Normal mode; any transition to Fail-safe mode is disabled and the UJA1061 remains in the mode in which the problem occurred; the only exception that results in entry into Fail-safe mode is a V1 undervoltage longer than 256 ms as self-protection of the SBC
- V1 is started with the defined Reset (20 ms LOW-to-HIGH)
- V2 is ON; undervoltage protection is still active, which results in V2 switching OFF; V2 can only be switched on again by disconnecting the TEST and BAT pins and then reconnecting first the TEST pin and later the BAT42/14 pin
- CAN and LIN are in active mode and cannot switch to an Off-line mode
- V3 is ON; undervoltage protection is still active, which results in V3 switching OFF; V3 can only be switched on again by disconnecting the TEST and BAT pins and then reconnecting first the TEST pin and later the BAT42/14 pin
- INH is ON
- SYSINH is ON
- In the case of a V1 undervoltage, a reset will be performed until V1 is restored (normal behaviour); the UJA1061 stays in Forced Normal mode; in case of a continuous overload at V1 (> 256 ms) Fail-safe mode will be entered; V1 can be switched on again only by disconnecting the TEST and BAT pins and then reconnecting first the TEST pin and later the BAT42/14 pin
- Pulling pin RSTN LOW externally will not result in leaving the Forced Normal mode, the UJA1061 will ignore external resets; this is because the FLASH programmer uses pin RSTN for other purposes (i.e. the FLASH programmer uses the RSTN line for serial communication entering/preparing the FLASH ROM routines with special sequences)
- No Reset Lengthening
- Directly after pin RSTN is released, pin EN will go HIGH; a LOW value on pin RSTN (but not an external LOW value) will result in a LOW value on the pin EN; pin EN stays active all the time during Forced Normal mode.

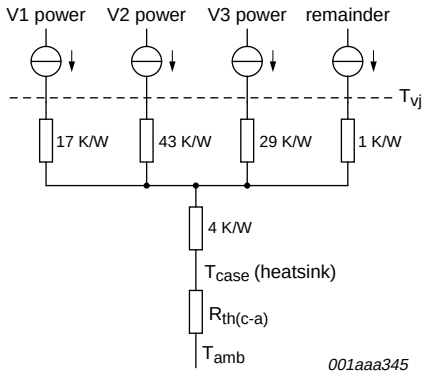
7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BAT42}	42 V supply voltage		–0.3	+60	V
		load dump; $t \leq 500$ ms	–	+60	V
V_{BAT14}	14 V supply voltage		–0.3	+33	V
		load dump; $t \leq 500$ ms	–	+50	V
V_{TXDC}, V_{RXDC}, V_{TXDL}, V_{RXDL}, V_{RSTN}, V_{INTN}, V_{SDO}, V_{SDI}, V_{SCK}, V_{SCS}, V_{EN}	DC voltages on pins TXDC, RXDC, TXDL, RXDL, RSTN, INTN, SDO, SDI, SCK, SCS and EN		–0.3	V_{V1} + 0.3	V
V_{INH}, V_{WAKE}, V_{V3}, V_{SYSINH}	DC voltage at pins INH, WAKE, V3 and SYSINH		–0.3	V_{BAT42} + 0.3	V
V_{CANL}, V_{CANH}, V_{LIN}	DC voltage at pins CANL, CANH and LIN		–60	+60	V
V_{trt}	transient voltage at pins CANL, CANH and LIN (ISO6737)	tested with a special application	–150	+100	V
V_{RTH}, V_{RTL}, V_{RTLIN}	DC voltage at pins RTH, RTL and RTLIN		–60	V_{BAT42} + 1.2	V
V_{V1}, V_{V2}	DC voltage at pins V1 and V2		–0.3	+5.5	V
V_{SENSE}	DC voltage at pin SENSE		–0.3	V_{BAT42} + 1.2	V
V_{TEST}	DC voltage at pin TEST		–0.3	12	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+125	°C
T_{vj}	virtual junction temperature	note 1	–40	+150	°C
V_{esd}	electrostatic discharge voltage	HBM; note 2			
		at pins CANH, CANL, RTH, RTL, LIN, RTLIN, WAKE, BAT14, BAT42, V3, SENSE	–8.0	+8.0	kV
		at any other pin	–2.0	+2.0	kV
		MM; note 3; at any pin	–200	+200	V

Notes

1. In accordance with IEC 60747-1. An alternative definition of virtual junction temperature T_{vj} is: $T_{vj} = T_{amb} + P_d \times R_{th(vj\text{-}amb)}$, where $R_{th(vj\text{-}amb)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P_d) and ambient temperature (T_{amb}).
2. Human Body Model (HBM): C = 100 pF; R = 1.5 kΩ.
3. Machine Model (MM): C = 200 pF; L = 0.75 μH; R = 10 Ω.



The value $R_{th(c-a)}$ depends on the PCB used.
Without any PCB, $R_{th(c-a)}$ = 113 K/W.
With a 4-layer JEDEC PCB with an effective area of 50 x 50 mm, Rth(c-a) = 32.5 K/W.

Fig.14 Thermal model of HTTSOP32 package.

8 DC CHARACTERISTICS

T_{vj} = −40 to +150 °C, V_{BAT42} = 5.5 to 52 V, V_{BAT14} = 5.5 to 27 V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC. All parameters are guaranteed over the virtual junction temperature range by design. Products are 100% tested at 125 °C ambient temperature on wafer level (pre-testing). Cased products are 100% tested at 25 °C ambient temperature (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin BAT42)						
I_{BAT42}	supply current BAT42	Sleep mode; V3 OFF or in Cyclic mode; CAN and LIN in Off-line; $I_{INH} = I_{SYSINH} = I_{RTH} = I_{RTL} = I_{RTLIN} = 0$; $V_{WAKE} = V_{BAT42}$	–	50	100	µA
		Sleep mode; V3 continuously ON; CAN and LIN in Off-line; $I_{INH} = I_{SYSINH} = I_{RTH} = I_{RTL} = I_{RTLIN} = 0$; $V_{WAKE} = V_{BAT42}$	–	60	120	µA
		Sleep mode; V2 ON; V3 continuously ON; CAN in Selective Sleep mode or On-line; LIN in Off-line; $I_{INH} = I_{SYSINH} = I_{RTH} = I_{RTL} = I_{RTLIN} = 0$; $V_{WAKE} = V_{BAT14} = V_{BAT42}$	–	70	140	mA
		Standby mode; V1, V2 ON; V3 continuously ON; CAN in Selective Sleep mode or On-line; LIN in Off-line; $I_{INH} = I_{SYSINH} = I_{RTH} = I_{RTL} = I_{RTLIN} = 0$; $V_{WAKE} = V_{BAT42}$	–	70	140	µA
		Normal mode; V1, V2, V3 ON; CAN and LIN in Active mode; watchdog ON; L42C = logic 0; $I_{V3} = I_{INH} = I_{SYSINH} = 0$; $V_{WAKE} = V_{BAT42}$; $V_{BAT14} \geq V_{BAT42}$	–	70	140	µA
		Normal mode; V1, V2, V3 ON; CAN and LIN in Active mode; watchdog ON; L42C = logic 0; $I_{V3} = I_{INH} = I_{SYSINH} = 0$; $V_{WAKE} = V_{BAT42}$; $V_{BAT14} < V_{BAT42}$	–	250	500	µA
		Normal mode; V1, V2, V3 ON; CAN and LIN in Active mode; watchdog ON; L42C = logic 1; $I_{V3} = I_{INH} = I_{SYSINH} = 0$; $V_{WAKE} = V_{BAT42}$; $V_{BAT14} > V_{BAT42}$	–	500	1000	µA
		Normal mode; V1, V2, V3 ON; CAN and LIN in Active mode; watchdog ON; L42C = logic 1; $I_{V3} = I_{INH} = I_{SYSINH} = 0$; $V_{WAKE} = V_{BAT42}$; $V_{BAT14} < V_{BAT42}$	–	700	1400	µA
$V_{(BAT42)POR}$	supply voltage BAT42 Power-on reset	Power-on reset flag (PWONS) set	–	–	1	V
		Power-on reset flag (PWONS) not set	4	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin BAT14)						
I_{BAT14}	supply current BAT14	Normal mode; V1, V2, V3 ON; CAN and LIN in Active mode; CAN in Single-wire mode; watchdog ON; V_{TXDC} = 0 V (dominant), V_{TXDL} = 0 V (dominant); I_{V1} =I_{RTH} = I_{RTL} = I_{RTLIN} = 0; no load on CANH, CANL and LIN	–	19	28	mA
		Normal mode; V1, V2, V3 ON; CAN and LIN in Active mode; CAN in Differential mode; watchdog ON; V_{TXDC} = 0 V (dominant); V_{TXDL} = 0 V (dominant); I_{V1} =I_{RTH} = I_{RTL} = I_{RTLIN} = 0; no load on CANH, CANL and LIN	–	13	21	mA
		Normal mode; V1, V2 and V3 ON; CAN and LIN in Active mode; CAN in single-wire mode; watchdog ON; V_{TXDC} = V_{V1} (recessive); V_{TXDL} = 0 V or V_{V1} (dominant or recessive); I_{V1} =I_{RTH} = I_{RTL} = I_{RTLIN} = 0; no bus failure; no load on CANH, CANL and LIN	–	10	19	mA
		Normal mode; V1, V2 and V3 ON; CAN and LIN in Active mode; CAN in Differential mode; watchdog ON; V_{TXDC} = V_{V1} (recessive), V_{TXDL} = 0 V or V_{V1} (dominant or recessive); I_{V1} = I_{RTH} = I_{RTL} = I_{RTLIN} = 0; no load on CANH, CANL and LIN	–	6.5	12	mA
		Standby mode; V1, V2, V3 ON; CAN in Selective Sleep mode or On-line; LIN in Off-line; CAN in single-wire mode; watchdog ON; V_{TXDC} = V_{TXDL} = V_{V1}; I_{V1} =I_{RTH} = I_{RTL} = I_{RTLIN} = 0	–	9	17	mA
		Standby mode; V1, V2, V3 ON; CAN in Selective Sleep mode or On-line; LIN in Off-line; CAN in differential mode; watchdog ON; V_{TXDC} = V_{TXDL} = V_{V1}; I_{V1} =I_{RTH} = I_{RTL} = I_{RTLIN} = 0	–	6	11	mA
		Standby mode; V1 ON; V2, V3 OFF; CAN and LIN in Off-line; I_{V1} =I_{RTH} = I_{RTL} = I_{RTLIN} = 0	–	250	450	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{BAT14} (cont.)	supply current BAT14 (cont.)	Sleep mode; V1, V2 OFF; V3 ON; CAN in Selective Sleep mode or On-line; LIN in Off-line; $I_{RTH} = I_{RTL} = I_{RTLIN} = 0$	–	6	11	mA
		Sleep mode; V1, V2 OFF; V3 ON; CAN and LIN in Off-line; $I_{RTH} = I_{RTL} = I_{RTLIN} = 0$; $V_{BAT14} > V_{BAT42}$	–	15	30	µA
		Sleep mode; V1, V2 OFF; V3 ON; CAN and LIN in Off-line; $I_{RTH} = I_{RTL} = I_{RTLIN} = 0$; $V_{BAT14} < V_{BAT42}$	–	10	20	µA
$V_{IL(BAT14)}$	BAT14 voltage level for low output current capability at V1	I_{V1} limited to –100 mA	8	–	27	V
$V_{IH(BAT14)}$	BAT14 voltage level for high output current capability at V1	I_{V1} limited to –300 mA	6.5	–	7	V
$V_{hys(BAT14)}$	hysteresis of BAT14 level for switching output current capability at V1		–	500	–	mV
Battery supply monitor input (pin SENSE)						
$V_{th(SENSE)}$	input threshold low battery voltage		1	2.5	4	V
I_{IH}	HIGH-level input current	Normal mode	tbf	50	tbf	µA
		Sleep and Standby modes	tbf	10	tbf	µA
Voltage source (pin V1)						
V_{V1}	supply voltage	V_{BAT14} = 9 to 16 V; I_{V1} = –50 to –5 mA	$V_{V1(nom)}$ – 0.1	$V_{V1(nom)}$	$V_{V1(nom)}$ + 0.1	V
		V_{BAT14} = 14 V; I_{V1} = –5 mA; T_j = 25 °C	$V_{V1(nom)}$ – 0.025	$V_{V1(nom)}$	$V_{V1(nom)}$ + 0.025	V
ΔV_{V1}	supply voltage regulation	V_{BAT14} = 9 to 16 V; I_{V1} = –5 mA; T_j = 25 °C	–	tbf	25	mV
	load regulation	V_{BAT14} = 14 V; I_{V1} = –50 to –5 mA; T_j = 25 °C	–	tbf	25	mV
$\Delta_{V1(T)}$	voltage drift with temperature	V_{BAT14} = 14 V; I_{V1} = –5 mA; T_j = –40 to +150 °C; note 1	–	tbf	200	ppm/K
$V_{BAT14-V1}$	V_{BAT14} to V_{V1} voltage drop	V_{BAT14} = 5.05 V; I_{V1} = –50 mA; T_j = 25 °C	–	tbf	0.3	V
$V_{rel(UV)(V1)}$	undervoltage release level of reset	V_{BAT14} = 14 V	0.90 × $V_{V1(nom)}$	0.92 × $V_{V1(nom)}$	0.94 × $V_{V1(nom)}$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{det(UV)(V1)}$	undervoltage detection and activation levels of reset	V_{BAT14} = 14 V; V1RTHC = logic 0	0.88 × $V_{V1(nom)}$	0.90 × $V_{V1(nom)}$	0.92 × $V_{V1(nom)}$	V
		V_{BAT14} = 14 V; V1RTHC = logic 1	0.68 × $V_{V1(nom)}$	0.70 × $V_{V1(nom)}$	0.72 × $V_{V1(nom)}$	V
$V_{hys(reset)}$	hysteresis of reset level	V_{BAT14} = 14 V; V1RTHC = logic 0	0.01 × $V_{V1(nom)}$	0.02 × $V_{V1(nom)}$	0.04 × $V_{V1(nom)}$	V
$V_{RAM(V1)}$	RAM content lost monitor level	V_{BAT14} = 14 V	0.40 × $V_{V1(nom)}$	0.45 × $V_{V1(nom)}$	0.50 × $V_{V1(nom)}$	V
$I_{thH(V1)}$	undercurrent threshold for watchdog enable		–2	–4	–6	mA
$I_{thL(V1)}$	undercurrent threshold for watchdog disable		–1.5	–3	–5	mA
$I_{hys(th)(V1)}$	undercurrent threshold hysteresis		0.5	1	1.5	mA
I_{V1}	output current capability	V_{BAT14} = 7 V	–300		tbf	mA
		V_{BAT14} = 8 to 27 V	–100		–200	mA
Voltage source (pin V2)						
V_{V2}	supply voltage	V_{BAT14} = 9 to 16 V; I_{V2} = –100 to –10 mA	4.8	5.0	5.2	V
		V_{BAT14} = 14 V; T_j = 25 °C, I_{V2} = –10 mA	4.95	5.0	5.05	V
ΔV_{V2}	supply voltage regulation load regulation	V_{BAT14} = 9 to 16 V; I_{V2} = –10 mA; T_j = 25 °C	–	tbf	25	mV
		V_{BAT14} = 14 V; I_{V2} = –100 to –10 mA; T_j = 25 °C	–	tbf	50	mV
$\Delta_{V2(T)}$	voltage drift with temperature	V_{BAT14} = 14 V; –40 °C < T_j < 150 °C; I_{V2} = –10 mA; note 1	–	tbf	200	ppm/K
$V_{BAT14-V2}$	V_{BAT14} to V_{V2} voltage drop	V_{BAT14} = 5.75 V; I_{V2} = –100 mA; T_j = 25 °C	–	tbf	1.0	V
$V_{det(UV)(V2)}$	undervoltage detection threshold	V_{BAT14} = 14 V	4.45	4.6	4.75	V
$V_{hys(det)UV}$	hysteresis of undervoltage detection threshold	V_{BAT14} = 14 V	–	50	–	mV
I_{V2}	output current capability	V_{BAT14} = 9 to 27 V	–200	–	–100	mA
Voltage source (pin V3)						
$V_{BAT42-V3}$	V_{BAT42} to V_{V3} voltage drop	V_{BAT42} = 9 to 58 V; I_{V3} = –20 mA	–	–	1.0	V
$I_{det(OL)(V3)}$	overload current detection threshold	V_{BAT42} = 9 to 58 V	–150	–	–70	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
42 V inhibit output (pin SYSINH)						
$V_{BAT42-SYSINH}$	V_{BAT42} to V_{SYSINH} voltage drop	I_{SYSINH} = −0.2 mA	–	–	1.0	V
$\|I_L\|$	leakage current	V_{SYSINH} = 0 V	–	–	5	µA
Inhibit output (pin INH)						
$V_{BAT14-INH}$	V_{BAT14} to V_{INH} voltage drop	I_{INH} = −10 µA	–	0.7	1.0	V
		I_{INH} = −200 µA	–	1.2	2.0	V
$\|I_L\|$	leakage current	V_{INH} = 0 V	–	–	5	µA
Wake input (pin WAKE)						
$V_{det(WAKE)}$	WAKE detection threshold	detection level	2.0	3.3	4.5	V
		release level	2.0	3.5	4.5	V
$V_{hys(det)WAKE}$	detection threshold hysteresis		100	200	500	mV
I_{WAKE}	pull-up input current	V_{WAKE} = 0 V	−10	–	−4	µA
Serial peripheral interface inputs (pins SDI, SCK, SCS)						
$V_{th(IL)}$	LOW-level input threshold voltage		−0.3	–	$0.3 \times V_{V1}$	V
$V_{th(IH)}$	HIGH-level input threshold voltage		$0.7 \times V_{V1}$	–	V_{V1} + 0.3	V
$\Delta V_{hys(th)}$	hysteresis of input threshold voltage		200	–	400	mV
$R_{pd(SCK)}$	pull-down resistor at pin SCK	V_{SCK} = 2 V; $V_{V1} \geq$ 2 V	50	130	400	kΩ
$R_{pd(SCS)}$	pull-down resistor at pin SCS	V_{SCS} = 1 V; $V_{V1} \geq$ 2 V	50	130	400	kΩ
I_{SDI}	input leakage current at pin SDI	V_{SDI} = 0 to V_{V1}	−5	–	+5	µA
Serial peripheral interface data output (pin SDO)						
I_{OL}	LOW-level output current	V_O = 0.4 V	1.6	–	tbf	mA
I_{OH}	HIGH-level output current	$V_O = V_{V1}$ − 0.4 V	tbf	–	−1.6	mA
I_{LOZ}	OFF-state output leakage current	V_O = 0 to V_{V1}	−5	–	+5	µA
Reset push-pull input/output (pin RSTN)						
$V_{th(IL)}$	LOW-level input threshold voltage		−0.3	–	$+0.3 \times V_{V1}$	V
$V_{th(IH)}$	HIGH-level input threshold voltage		$0.7 \times V_{V1}$	–	V_{V1} + 0.3	V
$\Delta V_{hys(th)}$	hysteresis of input threshold voltage		200	–	400	mV
I_{OL}	LOW-level output current	V_O = 0.4 V	50	–	1000	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH-level output current	$V_O = V_{V1} - 0.4$ V; V1 = ON	–1.6	–	–0.5	mA
V_{OL}	LOW-level output voltage with V1 LOW	I_{OL} = 20 µA; V_{V1} = 1.2 V	0	–	0.4	V
Enable output (pin EN)						
I_{OL}	LOW-level output current	V_O = 0.4 V	tbf	–	tbf	mA
I_{OH}	HIGH-level output current	$V_O = V_{V1} - 0.4$ V	tbf	–	–1.6	mA
V_{OL}	LOW-level output voltage	I_{OL} = 20 µA; V_{V1} = 1.2 V	0	–	0.4	V
Interrupt open-drain output (pin INTN)						
I_{OL}	LOW-level output current	V_O = 0.4 V	1.6	–	tbf	mA
CAN-bus transmit data input (pin TXDC)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3 \times V_{V1}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{V1}$	–	V_{V1} + 0.3	V
R_{pu}	TXDC pull-up resistor	V_{TXDC} = 0 V	5	12	25	kΩ
CAN-bus receive data output (pin RXDC)						
I_{OL}	LOW-level output current	V_{RXDC} = 0.4 V	1.6	–	tbf	mA
I_{OH}	HIGH-level output current	$V_{RXDC} = V_{V1} - 0.4$ V	tbf	–	–1.6	mA
CAN-bus lines (pins CANH and CANL)						
$V_{dif(CANH-CANL)}$	differential receiver threshold voltage	Active mode, On-line or Selective Sleep mode; V_{V2} = 5 V; no failures and bus failures H//, L//, HxGND and LxVCC	–3.5	–3.15	–2.8	V
$V_{se(CANH)}$	pin CANH single ended receiver threshold voltage	Active mode, On-line or Selective Sleep mode; V_{V2} = 5 V; bus failures LxGND, LxBAT and HxL	1.45	1.7	1.95	V
$V_{se(CANL)}$	pin CANL single ended receiver threshold voltage	Active mode, On-line or Selective Sleep mode; V_{V2} = 5 V; bus failures HxBAT and HxVCC	3.05	3.3	3.55	V
$V_{det(HxBAT)}$, $V_{det(LxBAT)}$	detection threshold voltage for bus failures HxBAT and LxBAT	Active mode, On-line or Selective Sleep mode; V_{V2} = 5 V	6.5	7.3	8.0	V
$V_{det(GSD)(CANH)}$	pin CANH ground shift detection threshold voltage	Active mode; V_{V2} = 5 V				V
		SPI bit GSDTH = logic 0	–1.25	–0.75	–0.25	V
		SPI bit GSDTH = logic 1	–2.0	–1.5	–1.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{wu(CANH)}$	pin CANH wake-up threshold voltage	Off-line	2.5	3.2	3.9	V
$V_{wu(CANL)}$	pin CANL wake-up threshold voltage	Off-line	1.1	1.8	2.5	V
$\Delta V_{wu(CANH-CANL)}$	wake-up threshold difference voltage	CANH to CANL; Off-line	0.8	1.4	–	V
$V_{O(reces)}$	CANH recessive output voltage	Active mode, On-line or Selective Sleep mode; V_{V2} = 4.75 to 5.25 V; $V_{TXDC} = V_{V2}$	–	–	0.2	V
	CANL recessive output voltage	Active mode, On-line or Selective Sleep mode; V_{V2} = 4.75 to 5.25 V; $V_{TXDC} = V_{V2}$	V_{V2} – 0.2	–	–	V
$V_{O(dom)}$	CANH dominant output voltage	Active mode, On-line or Selective Sleep mode; V_{TXDC} = 0 V; V_{V2} = 5 V; I_{CANH} = –40 mA	V_{V2} – 1.4	–	–	V
	CANL dominant output voltage	Active mode, On-line or Selective Sleep mode; V_{TXDC} = 0 V; V_{V2} = 5 V; I_{CANL} = –40 mA	–	–	1.4	V
$I_{O(CANH)}$	pin CANH output current	Active mode; V_{CANH} = 0 V; V_{TXDC} = 0 V; V_{V2} = 5 V	–100	–75	–45	mA
		Auto mode; V_{CANH} = 0 V; V_{BAT14} = 14 V	–	–0.25	–	µA
$I_{O(CANL)}$	pin CANL output current	Active mode; V_{CANL} = 5 V; V_{TXDC} = 0 V; V_{V2} = 5 V	45	75	100	mA
		Auto mode; V_{CANL} = 14 V; V_{BAT14} = 14 V	–	0	–	µA
CAN termination resistor (pin RTH)						
$R_{sw(RTH)}$	switch-on resistance	measured between RTH and GND; Active mode, On-line or Selective Sleep; $\lvert I_o \rvert$ = 10 mA; V_{TXDC} = 5 V	–	50	100	Ω
$V_{O(RTH)}$	output voltage	Off-line; I_O = 100 µA	–	0.7	1.0	V
$I_{O(RTH)}$	pin CANH output current during bus failure	Active mode; $V_{RTH} = V_{CANH} = V_{V2}$ = 5 V	–	75	–	µA
CAN termination resistor (pin RTL)						
$R_{sw(RTL)}$	switch-on resistance	Active mode, On-line or Selective Sleep; $\lvert I_o \rvert$ = 10 mA; V_{TXDC} = 5 V; V_{V2} = 5 V	–	50	100	Ω
$I_{O(RTL)}$	output current	Off-line; V_{RTL} = 0 V	–1.0	–0.3	–0.1	mA
$V_{O(RTL)}$	output voltage	Off-line; R_{RTL} = 10 MΩ	6	8	11	V
		Off-line; I_{RTL} = –100 µA	4.5	7	11	V
$I_{O(RTL)}$	output current during bus failure at CANL	Active mode; $V_{RTL} = V_{CANL}$ = 0 V; V_{V2} = 5 V	–	–75	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit data input (pin TXDL)						
V_{IL}	LOW level input voltage		–0.3	–	$0.3 \times V_{V1}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{V1}$	–	$V_{V1} + 0.3$	V
R_{pu}	TXDL pull-up resistor	V_{TXDL} = 0 V	5	12	25	kΩ
Receive data output (pin RXDL)						
I_{OH}	HIGH-level output current	$V_{RXDL} = V_{V1} - 0.4$ V	tbf	–	–0.4	mA
I_{OL}	LOW-level output current	V_{RXDL} = 0.4 V	0.4	–	tbf	mA
Temperature detection						
$T_{j(warning)}$	high junction temperature warning level		160	175	190	°C
LIN-bus line (pin LIN)						
$V_{o(dom)}$	LIN dominant output voltage	Normal mode; V_{TXDL} = 0 V L42C = logic 0; V_{BAT14} = 7.0 to 27 V; $R_{BAT14-LIN}$ = 500 Ω	0	–	$0.20 \times V_{BAT14}$	V
		L42C = logic 1; $V_{BAT42} \geq 18$ V; I_{LIN} = –20 mA	0	–	1.4	V
I_{LIH}	HIGH-level input leakage current	$V_{LIN} = V_{BAT42}$; $V_{TXDL} = V_{V1}$	–10	0	+10	µA
$I_{O(SC)}$	short-circuit output current	Normal mode; V_{TXDL} = 0 V; $t < t_{TXDL(dom)}$				
		L42C = logic 0; $V_{LIN} = V_{BAT14}$ = 12 V	25	40	60	mA
		L42C = logic 0; $V_{LIN} = V_{BAT14}$ = 27 V	55	90	125	mA
		L42C = logic 1; V_{LIN} = 58 V; $V_{BAT42} \geq 18$V	25	40	60	mA
$V_{th(dom)}$	receiver dominant state	L42C = logic 0	–	–	$0.4 \times V_{BAT14}$	V
		L42C = logic 1; $V_{BAT42} \geq 18$ V	–	–	4.4	V
$V_{th(rec)}$	receiver recessive state	L42C = logic 0	$0.6 \times V_{BAT14}$	–	–	V
		L42C = logic 1; $V_{BAT42} \geq 18$ V	7.8	–	–	V
$V_{th(centre)}$	receiver threshold voltage centre	L42C = logic 0	$0.475 \times V_{BAT14}$	$0.500 \times V_{BAT14}$	$0.525 \times V_{BAT14}$	V
		L42C = logic 1; $V_{BAT42} \geq 18$ V	5.4	6.0	6.6	V
$V_{hys(th)}$	hysteresis of receiver threshold voltage	L42C = logic 0	$0.05 \times V_{BAT14}$	–	$0.175 \times V_{BAT14}$	V
		L42C = logic 1; $V_{BAT42} \geq 18$ V	0.56	–	2.34	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LIN-bus termination resistor connection (pin RTLIN)						
V_O	output voltage	I_{RTLIN} = −10 µA; L42C = logic 1; $V_{BAT42} \geq 18$ V				V
		Normal mode; V_{LIN} = 12 V (rec)	10.8	11.4	12.0	V
		Normal mode; V_{LIN} = 0 V; $t > t_{LIN(dom)}$	9	12	15	V
		Off-line mode; V_{LIN} = 12 V (rec)	9	12	15	V
ΔV_{RTLIN}	RTLIN load regulation	Normal mode; I_{RTLIN} = −10 µA to −10 mA; L42C = logic 0 ($V_{LIN} = V_{BAT14(rec)}$) **or** L42C = logic 1 ($V_{LIN(rec)}$ = 12 V; $V_{BAT42} \geq 18$ V)	–	250	500	mV
$I_{O(pu)}$	RTLIN pull-up current	Normal mode; V_{RTLIN} = 0 V; V_{LIN} = 0 V ($t > t_{LIN(dom)}$)	−150	−75	−35	µA
		Off-line mode; V_{RTLIN} = 0 V; L42C = logic 0 ($V_{LIN} = V_{BAT14(rec)}$) **or** L42C = logic 1 ($V_{LIN(rec)}$ = 12 V; $V_{BAT42} \geq 18$ V)	−150	−75	−35	µA
$I_{O(RTLIN)}$	low-level leakage current	Off-line mode; V_{RTLIN} = 0 V; V_{LIN} = 0 V ($t > t_{LIN;dom}$)	−10	0	+10	µA
TEST input (pin TEST)						
$V_{th(TEST)}$	threshold voltage	for entering Watchdog-OFF mode	3	5	7	V
	threshold voltage	for entering forced Normal mode	8	10	12	V
$R_{(pd)TEST}$	pull-down resistor	between pin TEST and GND	2	4	8	kΩ

Note

1. Not tested during production.

9 AC CHARACTERISTICS

T_{vj} = –40 to + 150 °C; V_{BAT42} = 5.5 to 52 V; V_{BAT14} = 5.5 to 27 V; unless otherwise specified. All voltages are defined with respect to ground. Positive currents flow into the IC. All parameters are guaranteed over the virtual junction temperature range by design. Products are 100% tested at 125 °C ambient temperature on wafer level (pre-testing). Cased products are 100% tested at 25 °C ambient temperature (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial Peripheral Interface (SPI) timing (pins SCS, SCK, SDI, SDO) (see Fig.19)						
T_{cyc}	clock cycle time		480	–	–	ns
t_{lead}	enable lead time	clock is low when SPI select falls	240	–	–	ns
t_{lag}	enable lag time	clock is low when SPI select rises	240	–	–	ns
t_{SCKH}	clock HIGH time		190	–	–	ns
t_{SCKL}	clock LOW time		190	–	–	ns
t_{su}	input data set-up time		100	–	–	ns
t_h	input data hold time		100	–	–	ns
t_{DOV}	output data valid time	pin SDO, C_L = 10 pF	–	–	100	ns
t_{SSH}	SPI select HIGH time		200	–	–	ns
t_{SSL}	SPI select LOW time		100	–	–	ns
CAN transceiver (pins CANL, CANH, TXDC and RXDC)						
$t_{t(rec-dom)}$	output transition time recessive to dominant	10 to 90 %; C1 = 10 nF; C2 = 0 nF; R1 = 100 Ω; see Figs 15 and 16	0.6	1.2	–	µs
$t_{t(dom-rec)}$	output transition time dominant to recessive	90 to 10 %; C1 = 1 nF; C2 = 0 nF; R1 = 100 Ω; see Figs 15 and 16	0.3	0.7	–	µs
t_{PHL}	propagation delay TXDC to RXDC (HIGH to LOW transition)	50 % V_{TXDC} to 50 % V_{RXDC}; C1 = 10 nF; C2 = 0 nF; R1 = 100 Ω; see Figs 15 and 16	–	1.0	1.8	µs
t_{PLH}	propagation delay TXDC to RXDC (LOW to HIGH transition)	50 % V_{TXDC} to 50 % V_{RXDC}; C1 = 1 nF; C2 = 0 nF; R1 = 100 Ω; see Figs 15 and 16	–	1.2	1.9	µs
$t_{BUS(fail)(det)}$	bus failure detection time	bus failure HxBAT; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	7	–	38	µs
		bus failure HxVCC	1.6	–	8.0	ms
		bus failures LxGND and HxL	0.9	–	1.6	ms
		bus failure LxBAT; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	0.3	–	1.6	ms
		continuously dominant clamped CAN-bus detection time (start after detecting HxVCC); Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	0.3	–	1.6	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{BUS(fail)(recover)}$	bus failure recovery time	bus failure HxBAT	125	–	750	µs
		bus failure HxVCC	0.3	–	1.6	ms
		bus failures LxGND and HxL; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	7	–	38	µs
		bus failures LxGND and HxL	0.9	–	1.6	ms
		bus failure LxBAT; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	125	–	750	µs
		continuously dominant clamped CAN-bus Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	1	–	5	µs
$t_{TXDC(dom)}$	TXDC permanent dominant disable time	Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V; TXDC = logic 0 V	1.5	–	6	ms
$t_{CANH(d1)}$, $t_{CANL(d1)}$	minimum dominant time first pulse for wake-up on pins CANH, CANL	Off-line	7	–	38	µs
$t_{CANH(rec)}$, $t_{CANL(rec)}$	minimum recessive time pulse (after first dominant) for wake-up on pins CANH, CANL	Off-line	3	–	10	µs
$t_{CANH(d2)}$, $t_{CANL(d2)}$	minimum dominant time second pulse for wake-up on pins CANH, CANL	Off-line	0	–	3	µs
$t_{CANL(dom)}$	CANL dominant time entering Normal mode and TXDC goes dominant	V_{CANL} > 8 V, first dominant bit after entering Active mode	3	–	10	µs
$t_{offline}$	required recessive or dominant time for entering Off-line	On-line or Selective Sleep mode; COTC = logic 0; CM = logic 0	50	–	66	ms
		On-line or Selective Sleep mode; COTC = logic 1; CM = logic 0	200	–	265	ms
		On-line; CM = logic 0; coming out of Off-line	400	–	530	ms
t_{CANH}, t_{CANL}	ground shift sampling time required for CANH, CANL voltage level	Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V; TXDC recessive	20	–	80	µs
Δt_{PC}	pulse count difference between CANH and CANL for failure detection	bus failures H//, L//, HxGND and LxVCC; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	–	4	–	pulses
	dominant pulse count on CANH and CANL for failure recovery	bus failures H//, L//, HxGND and LxVCC; Active mode, On-line and Selective Sleep mode; V_{V2} = 5 V	–	4	–	pulses

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LIN-transceiver (pins LIN, TXDL and RXDL); note 1						
$\delta 1$	duty factor 1[2]	$V_{th(rec)(max)} = 0.744 \times V_{SUP}$; $V_{th(dom)(max)} = 0.581 \times V_{SUP}$; LSC = logic 0; t_{bit} = 50 µs; L42C = logic 0 with $V_{SUP} = V_{BAT14}$ = 7 to 18 V **or** L42C = logic 1 with $V_{BAT42} \geq 18$ V; V_{SUP} = internal 12 V	0.396	–	–	
$\delta 2$	duty factor 2[3]	$V_{th(rec)(min)} = 0.284 \times V_{SUP}$; $V_{th(dom)(min)} = 0.422 \times V_{SUP}$; LSC = logic 0; t_{bit} = 50 µs; L42C = logic 0 with $V_{SUP} = V_{BAT14}$ = 7.6 to 18 V **or** L42C = logic 1 with $V_{BAT42} \geq 18$ V; V_{SUP} = internal 12 V	–	–	0.581	
$\delta 3$	duty factor 3[2]	$V_{th(rec)(max)} = 0.778 \times V_{SUP}$; $V_{th(dom)(max)} = 0.616 \times V_{SUP}$; LSC = logic 1; t_{bit} = 96 µs; L42C = logic 0 with $V_{SUP} = V_{BAT14}$ = 7 to 18 V **or** L42C = logic 1 with $V_{BAT42} \geq 18$ V; V_{SUP} = internal 12 V	0.417	–	–	
$\delta 4$	duty factor 4[3]	$V_{th(rec)(min)} = 0.251 \times V_{SUP}$; $V_{th(dom)(min)} = 0.389 \times V_{SUP}$; LSC = logic 1; t_{bit} = 96 µs; L42C = logic 0 with $V_{SUP} = V_{BAT14}$ = 7.6 to 18 V **or** L42C = logic 1 with $V_{BAT42} \geq 18$ V; V_{SUP} = internal 12 V	–	–	0.590	
$t_{p(rx1)r}$, $t_{p(rx1)f}$, $t_{p(rx2)r}$, $t_{p(rx2)f}$	propagation delay of receiving nodes 1 and 2	C_{RXD} = 20 pF	–	–	6	µs
$t_{p(rx1)(sym)}$	symmetry of propagation delay of receiver	rising edge with respect to falling edge; C_{RXD} = 20 pF	–2	–	+2	µs
$t_{BUS(LIN)}$	dominant time for wake-up the LIN-transceiver	Off-line	30	–	150	µs
$t_{LIN(dom)(det)}$	continuously dominant clamped LIN-bus detection time	Active mode; LIN = logic 0 V	40	–	160	ms
$t_{LIN(dom)(rec)}$	continuously dominant clamped LIN-bus recovery time	Active mode	tbf	1	tbf	ms
$t_{TXDL(dom)(dis)}$	TXDL permanent dominant disable time	Active mode; TXDL = 0 V	20	–	80	ms
$t_{timeout}$	time-out period between wake-up message and confirm message	Selective Sleep mode	115	–	285	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Battery monitoring						
$t_{BAT42(L)}$	BAT42 LOW time for setting Power-on reset flag		5	–	20	µs
$t_{SENSE(L)}$	BAT42 LOW time for setting BAT fail flag		5	–	20	µs
Power supply V1 (pin V1)						
$t_{V1(CLT)}$	V1 clamped LOW time during ramp-up of V1	Start-up mode; V1 active	229	–	283	ms
t_{V1MODE}	LOW or HIGH time to change from V1 = 3 V to V1 = 5 V and back	V1 active	5	–	20	µs
Power supply V2 (pin V2)						
$t_{2(CLT)}$	V2 clamped LOW time during ramp-up V2	V2 active	28	–	36	ms
Power supply V3 (pin V3)						
$t_{W(CS)}$	cyclic sense period	V3C = 10; see Fig.12	180	–	220	µs
		V3C = 11; see Fig.12	360	–	440	µs
$t_{on(CS)}$	cyclic sense on-time	V3C = 10; see Fig.12	14	–	18	ms
		V3C = 11; see Fig.12	28	–	36	ms
Wake-up input (pin WAKE)						
t_{WU}	input port filter time	V_{BAT42} = 5 to 27 V	10	–	120	µs
		V_{BAT42} = 27 to 52 V	50	–	250	µs
$t_{su(CS)}$	cyclic sense sample set-up time	V3C = 11 or 10; see Fig.12	310	–	390	µs
Watchdog						
$t_{WD(ETP)}$	earliest trigger point	programmed Nominal Watchdog Period (NWP); Normal mode	0.45 × NWP	–	0.55 × NWP	
$t_{WD(LTP)}$	latest trigger point	programmed Nominal Watchdog Period (NWP); Normal mode, Standby and Sleep mode	0.9 × NWP	–	1.1 × NWP	
$t_{WD(init)}$	watchdog init period	watchdog time-out in Start-up mode	229	–	283	ms
Reset output (pin RSTN)						
$t_{RSTN(ext)}$	external reset monitoring time		229	–	283	ms
$t_{RSTN(CHT)}$	clamped HIGH time, pin RSTN	RSTN driven LOW internally but RSTN pin remains HIGH	115	–	141	ms
$t_{RSTN(INT)}$	interrupt monitoring time	INTN = logic 0	229	–	283	ms
t_{RSTNL}	reset lengthening time	after internal or external reset has been released; RST = logic 0	0.9	–	1.1	ms
		after internal or external reset has been released; RST = logic 1	18	–	22	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interrupt output (pin INTN)						
t_{INTNH}	interrupt release	after SPI has read out the interrupt register	2	–	5	µs
Oscillator						
f_{OSC}	oscillator frequency		460.8	512	563.2	kHz

Notes

1. t_{bit} = selected bit time, depends on LSC bits 50 or 96 µs (20 or 10.4 kbit/s respectively); bus load conditions (C_{bus}/R_{bus}): 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω; see Fig.18.

2. $\delta 1, \delta 3 = \frac{t_{BUS(rec)(min)}}{2 \times t_{bit}}$

3. $\delta 2, \delta 4 = \frac{t_{BUS(rec)(max)}}{2 \times t_{bit}}$

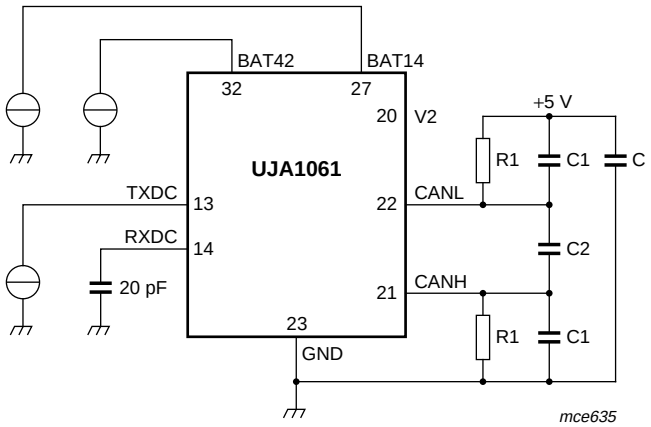


Fig.15 Timing test circuit for CAN-transceiver.

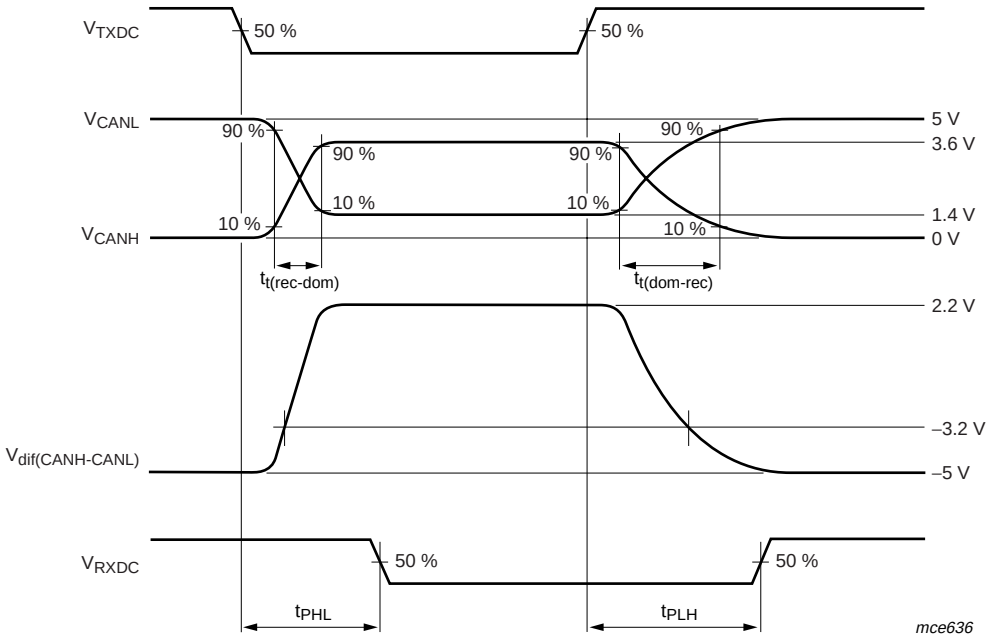


Fig.16 Timing diagram CAN-transceiver.

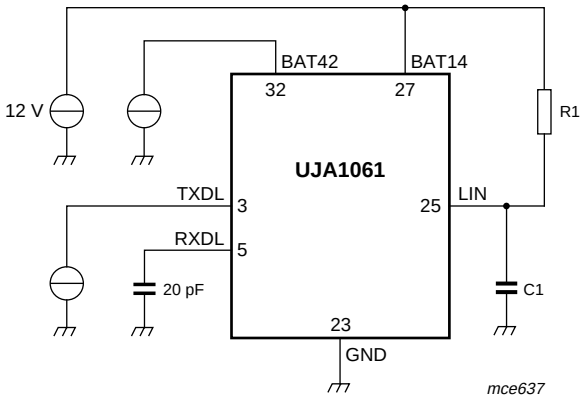
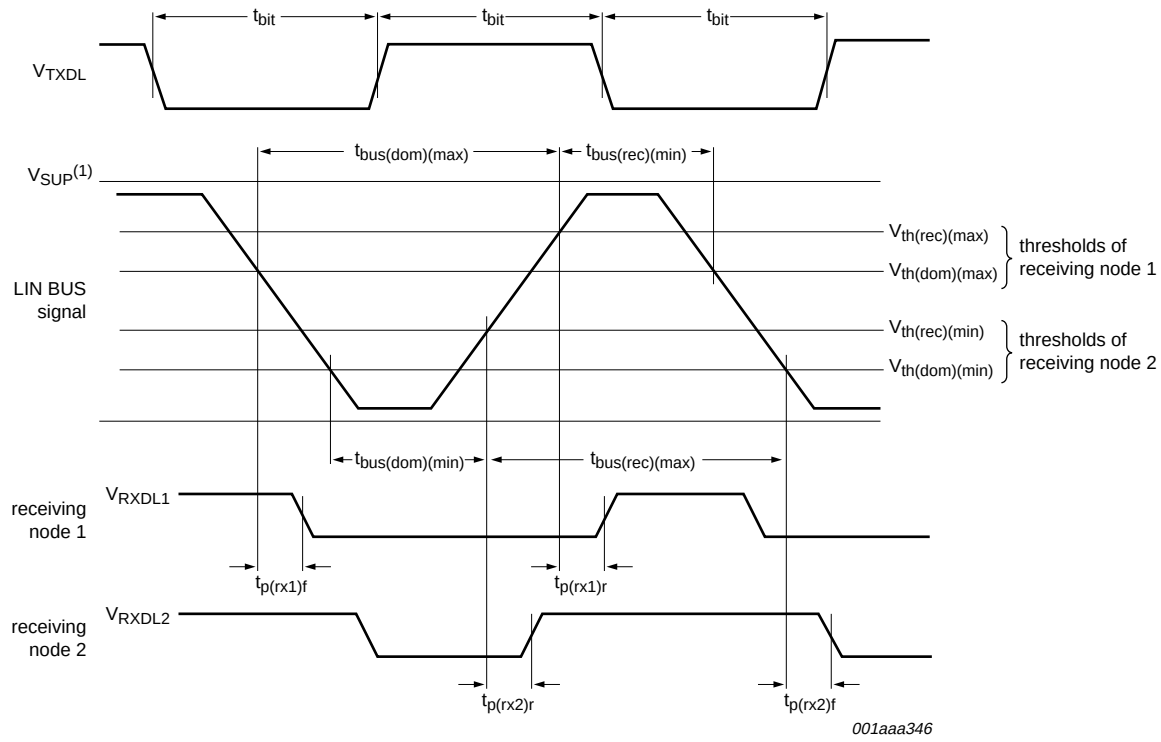


Fig.17 Timing test circuit for LIN-transceiver.



(1) Transceiver supply of transmitting node.

Fig.18 Timing diagram LIN-transceiver.

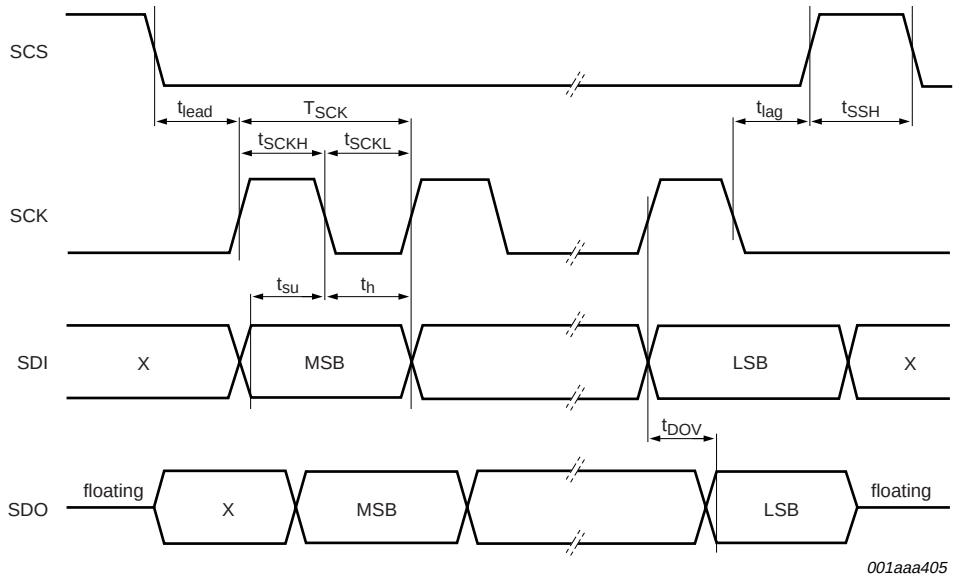
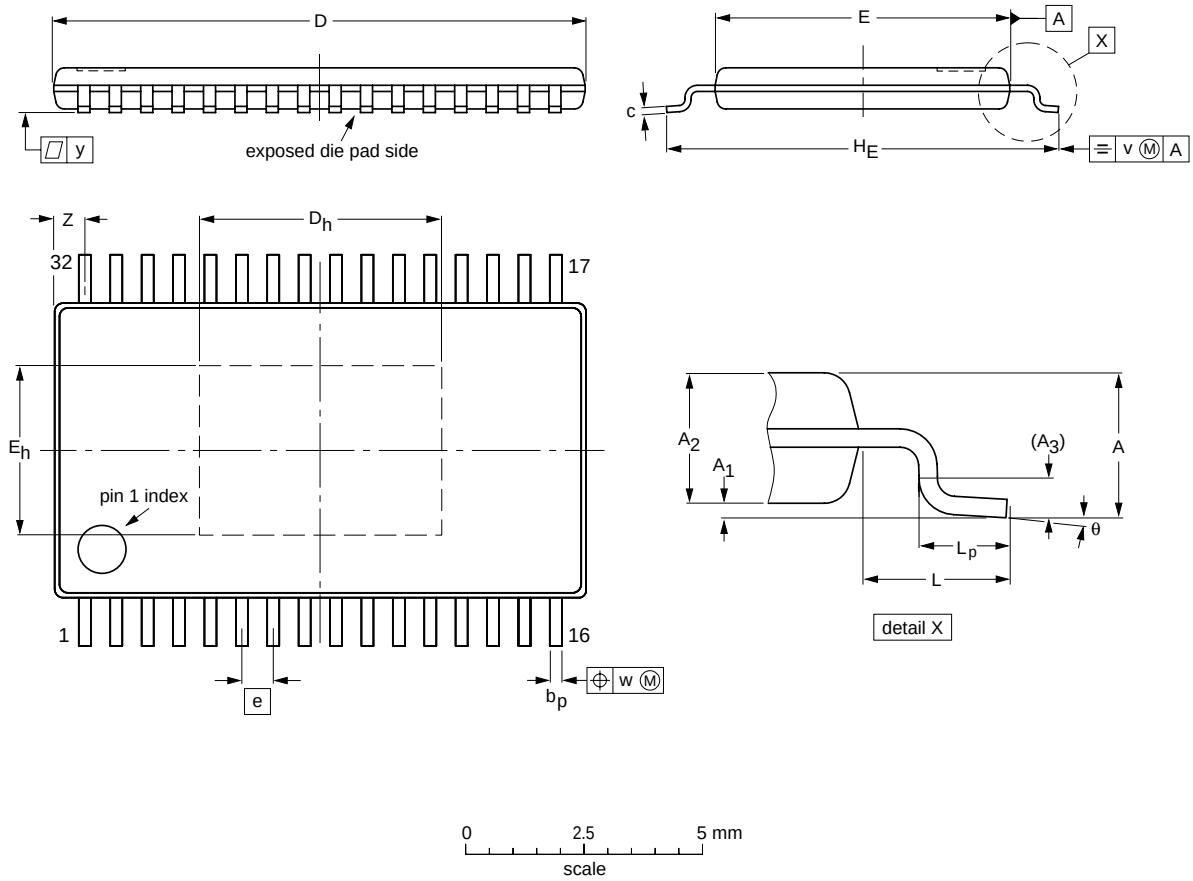


Fig.19 SPI timing.

10 PACKAGE OUTLINE

HTSSOP32: plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad **SOT549-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.1 10.9	5.1 4.9	6.2 6.0	3.6 3.4	0.65	8.3 7.9	1	0.75 0.50	0.2	0.1	0.1	0.78 0.48	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT549-1						~~99-03-04~~ 03-04-07

11 SOLDERING

11.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

11.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

11.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

12 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

13 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

14 DISCLAIMERS

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