MX98742

FEBC
100 BASE FAST ETHERNET
BRIDGE CONTROLLER

1.0 FEATURES

* 2-port MAC bridge supports both Fast Ethernet and Ethernet/Fast Ethernet bridging
* Minimum 16K byte, maximum 256K byte buffer memory
* Selectable TX/FX/T4 symbol-level repeater, MII interfaces, and 10BASE serial port
* T4 symbol mode includes the implementation of all PCS layers functions (8B/6T encode/decode, DE Balance encode/decode, error detection, ...etc.)
* 512-bit hash filtering
* Broadcast and Multicast packet filtering and inverse filtering
* Optional fast forwarding modes minimizes latency
* Optional dynamic auto buffer sizing
* JAM-based flow control ensures lossless buffering
* External Destination and Source Address filtering support
* Display of buffer boundary and flow-control JAM packet counts
* LED indication of flow-control JAM events

2.0 GENERAL DESCRIPTION

The Fast Ethernet Bridge Controller (FEBC) is a low-cost solution to link fast Ethernet repeaters together so that the distance between nodes can be expanded far beyond the 200m collision domain limitation. Each network segment connected through the bridge is in a separate collision domain, and the FEBC's function is to exchange all the good packets between two collision domain segments. A 512-bit hash filter is implemented to further reduce the traffic between segments if it is desired. A 10/100 bridge function is also supported.

The FEBC has two forwarding modes: (1) store-and forward : a complete packet is buffered before it is to be forwarded. Packets with CRC errors and other anomalies are discarded. (2) 64-byte forward : a packet is forwarded after the first 64 bytes are buffered. The number of bridges that can be put in one network is constrained largely by the buffer memory and performance consideration. Multiple FEBCs are totally invisible to the upper layer protocol.

The FEBC supports direct TX PHY interface and 25MHz-MII on both side. Port A of the FEBC also supports TX and T4 repeater ports at the symbobl level and port B of the FEBC also supports the 7-wire serial 10 MHz interface. The FEBC supports buffer memory from minimum 16 Kbytes to 256 Kbytes. The memory is partitioned into two sections with section A as the receive buffer for port A and section B for port B. The size of each section is equal if both sides are operating at 100 Mbps speed; the minimum size of each section is 8 Kbytes. In the auto-sizing mode, the FEBC will change the buffer size according to traffic pattern in each segment.

3.0 SYSTEM DIAGRAM

3.1 REPEATER WITH A BUILT-IN BRIDGE

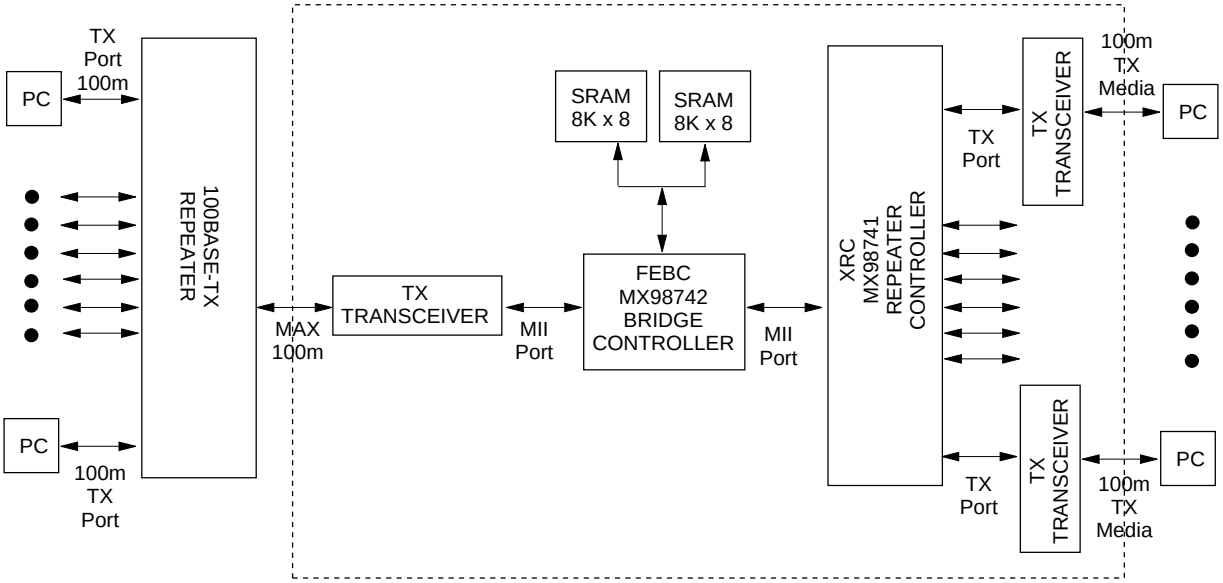


Figure 3-1. A Typical TX Connection

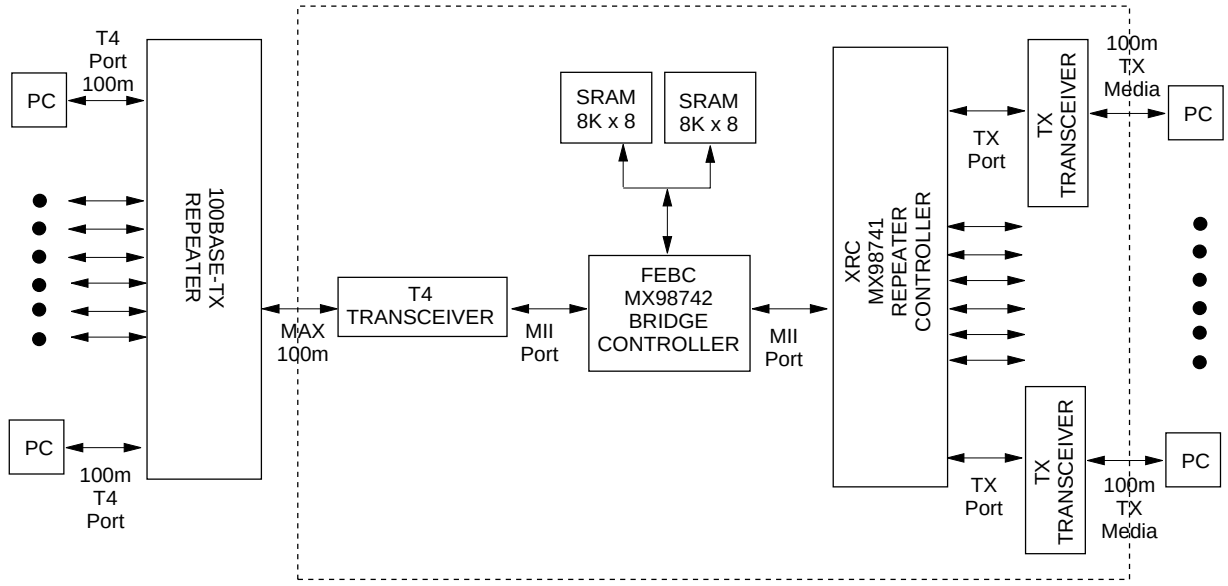


Figure 3-2. A Typical T4 Connection

4.0 CONNECTION DIAGRAM

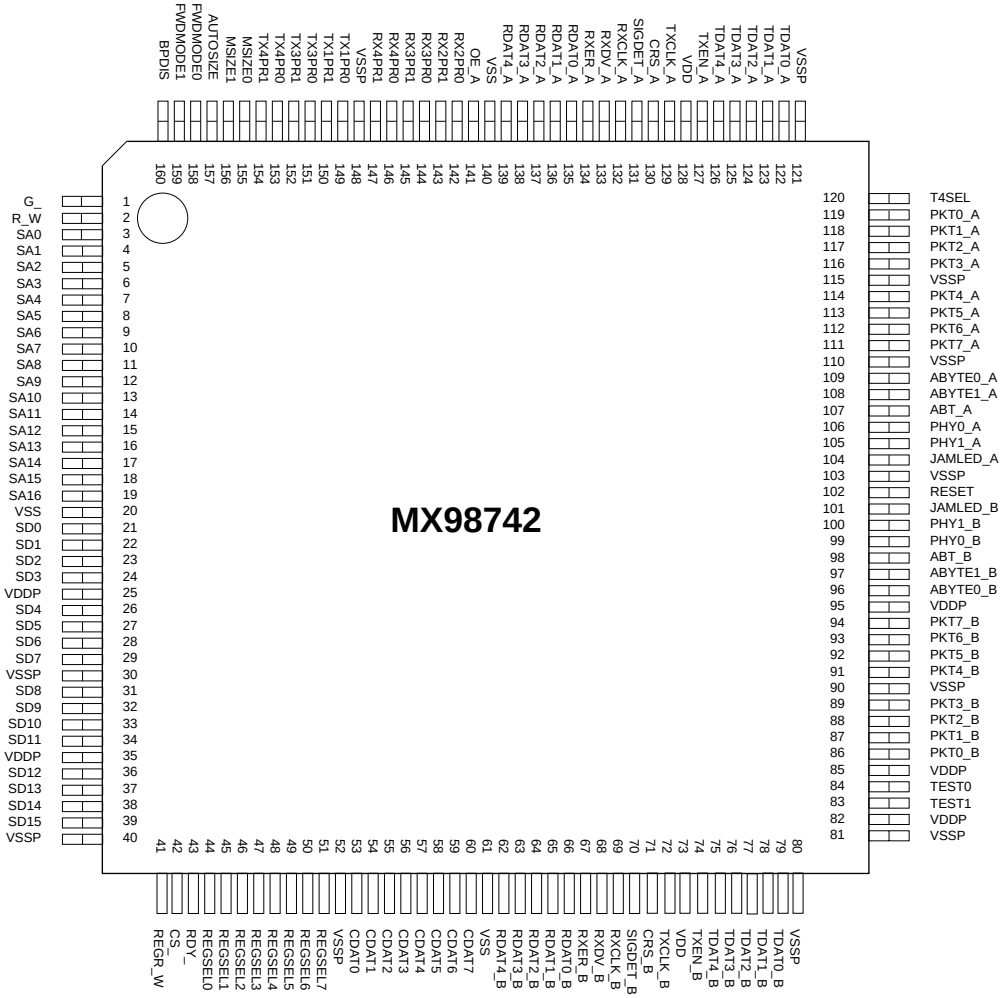


Figure 4-1. 160-pin PQFP Package

5.0 PIN DESCRIPTIONS

Table 5-1. Port A TX Interface (Am79865 and Am79866 or MC68836 or Macronix Data Transceiver or TX repeater port, 13 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
126-122	TDAT4-0_A/TXD3-0_A	O/Z, CMOS	TX Mode : Transmit Data X Port A. These five outputs driven at the rising edge of TXCLK_A are 4B/5B encoded transmit data symbols. TDAT4 is the Most Significant Bit. MII Mode : Transmit Data MII A. For each TXCLK_A period in which TXEN is asserted, TXD3-0, synchronous to TXCLK_A's rising edge, are driven by the MAC. The value of TXD3-0 is ignored when TXEN is deasserted. TXD3 is the Most Significant Bit.
129	TXCLK_A	I, TTL	TX Mode : Local Symbol Clock. 25 MHz clock input. TXCLK_A and RXCLK_A should be driven by the same timing reference if the MX98742 interfaces to TX repeater ports. MII Mode : Transmit Clock MII A. 25 MHz transmit clock.
139-135	RDAT4-0_A/RXD3-0_A	I, TTL	TX Mode : Received Data X Port A. These 5-bit parallel data symbols from transceiver are latched by the rising edge of RXCLK_A. RDAT4 is the Most Significant Bit. MII Mode : Receive Data X Port A. For each RXCLK_A period in which RXDV is asserted, RXD3-0, synchronous to RXCLK_A's rising edge, should be latched by the MAC. While RXDV is deasserted, RXD3-0 are the 5B/4B decoded nibbles from RDAT4-0. RXD3 is the Most Significant Bit.
132	RXCLK_A	I, TTL	TX Mode : Recovered Symbol Clock Port A. This 25 MHz clock input is derived from the clock symchronization PLL circuit. RXCLK_A and TXCLK_A should be driven by the same timing reference if MX98742 interfaces to TX repeater ports. T4 Mode : Recovered Symbol Clock. MII Mode : Receive Clock MII A. 25 MHz continuous clock that provides the timing reference for the transfer of RXDV, RXD and RXER signals.

131	SIGDET_A/LKGD/COL_A	I, TTL	TX Mode : Signal Detect Port A. This signal indicates that the received signal is above the detection threshold. If MX98742 interfaces to TX repeater ports, this pin should be pulled high. T4 : Link Good. The link state machine is in Link Pass state. MII Mode : Collision MII A. This signal is asserted if both the receiving media and TXEN are active.

Table 5-2. Port A T4 Symbol Level Interface (Broadcom/Cypress compatible, 17 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
143-142	RX2PR1-0	I, TLL	Receive Pair 2. 00:0V, 01:3.5V, 10:-3.5V. (Broadcom). 00:0V, 01:-3.5V, 10:3.5V. (Cypress)
145-144	RX3PR1-0	I, TLL	Receive Pair 3. 00:0V, 01:3.5V, 10:-3.5V. (Broadcom). 00:0V, 01:-3.5V, 10:3.5V. (Cypress)
147-146	RX4PR1-0	I, TLL	Receive Pair 4. 00:0V, 01:3.5V, 10:-3.5V. (Broadcom). 00:0V, 01:-3.5V, 10:3.5V. (Cypress)
150-149	TX1PR1-0	O/Z, CMOS	Transmit Pair 1. 00:0V, 01:3.5V, 10:-3.5V. (Broadcom). 00:0V, 01:-3.5V, 10:3.5V. (Cypress)
152-151	TX3PR1-0	O/Z, CMOS	Transmit Pair 3. 00:0V, 01:3.5V, 10:-3.5V. (Broadcom). 00:0V, 01:-3.5V, 10:3.5V. (Cypress)
154-153	TX4PR1-0	O/Z, CMOS	Transmit Pair 4. 00:0V, 01:3.5V, 10:-3.5V. (Broadcom). 00:0V, 01:-3.5V, 10:3.5V. (Cypress)
120	T4SEL	I, TTL	Transceiver Select : 1 : Broadcom, 0:Crypress
132	RXCLK_A	I, TTL	Receivered Symbol Clock.
130	PMACRS	I, TTL	PMA Carrier Sense. Mux'd with MII mode pin CRS_A.
134	PMARXER	I, TTL	PMA Receive Error. Mux'd with MII pin RXER_A.
131	LKGD	I, TTL	Link Good. Mux'd with TX pin SIGDET_A.

Table 5-3. Port A Meddia Independent Interface (15 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
129	TXCLK_A	I, TTL	Transmit Clock MII A. 25MHz transmit clock.
127	TXEN_A	O, CMOS	Transmit Enable MII A. TXEN_A, synchronous to TXCLK_A's rising edge, is asserted by the MAC with first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
125-122	TXD3-0_A	O, CMOS	Transmit Data MII A. Mux'd with TX mode pins TDAT3-0_A.
133	RXDV_A	I,TTL	Receive Data Valid MII A. This signal, synchronous to RXCLK's rising edge, remains asserted through the whole frame, starting with start-of-frame delimiter and excluding any end-of-frame delimiter.
130	CRS_A/PMACRS	I, TTL	MII Mode : Carrier Sense MII A. This pin is asserted when the receiving medium is not idle. T4 Mode : PMA Carrier Sense. This pin, synchronous to RXCLK_A, signals that activity is detected.
134	RXER_A/PMARXER	I, TTL	MII Mode : Receive Error MII A. While RXDV is asserted, i.e. a frame is being received, this signal which is synchronous to RXCLK_A's rising edge is asserted if any coding error is detected. T4 Mode : PMA Receive Error. Misaligment is detected.
132	RXCLK_A	I, TTL	Receive Clock MII A.
138-135	RXD3-0_A	I, TTL	Receive Data MII A. Mux'd with TX mode pins RDAT3-0_A.
131	COL_A	I, TTL	Collision MII A. Mux'd with TX SIGDET_A.

Table 5-4. Port A Output Control Pin (1 pin)

PIN#	PIN NAME	TYPE	DESCRIPTION
141	OE_A	I, TTL	Output Enable Port A. The assertion of OE_A, active low, enables TDAT4-0 (TX) or TX1_PR1-0, TX3_PR1-0, TX4_PR1-0 (T4) or TXD3-0 (MII), or TXENA, and it tristates these output pins if held High.

Table 5-5. Port B TX Interface (Am79865 and Am79866 or MC68836 or Macronix Data Transceiver, 13 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
72	TXCLK_B	I, TTL	TX Mode : Logic Symbol Clock. 25MHz clock input. If the FEBC is used to connected between two TX medum, TXCLK_A and TXCLK_B should be driven by the same reference source. MII Mode : Transmit clock MII B. 25/2.5MHz transmit clock. 7_wire Mode : This is the 10MHz transmit clock which is used only when 7_wire interface is selected at Port B.
75-79	TDAT4-0_B/TXD3-0_B	O, CMOS	TX Mode : Transmit Data X Port B. These five outputs driven at the rising edge of TXCLK_B are 4B/5B encoded transmit data symbols. TDAT4 is the Most Significant Bit. MII Mode : Transmit Data MII/B. For each TXCLK_B period in which TXEN is asserted, TXD3-0, synchronous to TXCLK_B's rising edge, are driven by the MAC. The value of TXD3-0 is ignored when TXEN is deasserted. TXD3 is the Most Significant Bit. If 7_wire mode is selected, only TXD0_B is active.
62-66	RDAT4-0_B/RXD3-0_B	I, TTL	TX Mode : Receive Data X Port B. These 5-bit parallel data symbols from transceiver are latched by the rising edge of RXCLK_B. RDAT4 is the Most Signaificant Bit. MII Mode : Receive Data MII/B. For each RXCLK_B period in which RXDV is asserted, RXD3-0, synchronous to RXCLK_B's rising edge, should be latched by the MAC. While RXDV is deasserted, RXD3-0 are the 5B/4B decoded nibbles from RDAT4-0. RXD3 is the Most Significant Bit. If 7_wire mode is selected, only RXD0_B is active.
69	RXCLK_B	I, TTL	TX Mode : Recovered Symbol Clock Port B. This is a 25MHz clock which is derived from the clock synchronization PLL circuit. RXCLK_B and TXCLK_B should be driven by the same timing reference if MX98742 interfaces to TX repeater ports. MII Mode : Receive Clock MII/B. This is the 25/2.5 MHz continuous clock that provides the timing reference for the transfer of the RXDV, RXD and RXER signals. If 7-Wire mode is selected, this is the 10MHz recovered clock.

70	SIGDET_B/COL_B	I, TTL	TX Mode : Signal Detect Port B. This signal indicates that the received signal is above the detection threshold. If MX98742 interfaces to TX repeater port, this pin should be pulled high. MII Mode : Collision MII/B. This signal is asserted if both the receiving media and TXEN are active. If 7_wire mode is selected, this pin is the collision signal.

Table 5-6. Port Media Independent Interface (15 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
72	TXCLK_B	I, TTL	Transmit clock MII/B. 25/2.5 MHz transmit clock. This is the 10MHz transmit clock which is used only when 7_wire mode interface is selected at Port B.
74	TXEN_B	O, CMOS	Transmit Enable MII/B. TXEN_B, synchronous to the TXCLK_B's rising edge, is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented. If 7_wire mode is selected, this pin denotes transmit enable.
76-79	TXD3-0_B	O, CMOS	Transmit Data MII/B. Mux'd with TX mode pins TDAT3-0_B. If 7_wire mode is selected, only TXD0_B is active.
68	RXDV_B	I, TTL	Receive Data Valid MII B. This signal, synchronous to RXCLK_B's rising edge, remains asserted through the whole frame, starting with start-of-frame delimiter and excluding any end-of-frame delimiter.
71	CRS_B	I, TTL	Carrier Sense MII/B. This pin is asserted when the receiving medium is not idle. In 7_wire mode is selected, this pin is an asynchronous CRS.
67	RXER_B	I, TTL	Receive Error MII. While RXDV_B is asserted in the case like a frame is received, this signal, synchronous to RXCLK_B's rising edge, is asserted when any coding errors are detected.
69	RXCLK_B	I, TTL	Receive Clock MII/7_wire B.
63-66	RXD3-0_B	I, TTL	Receive Data MII/7_wire B. Mux'd with TX mode pins RDAT3-0_B.
70	COL_B	I, TTL	Collision MII/10 B. Mux'd with TX mode pin SIGDET_B.

Table 5-7. Buffer SRAM Interface (35 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
19-3	SA16-0	O, CMOS	SRAM Address 0-16. These 17 address inputs select one of the 16-bit-wide words in the 128K x 16 SRAM buffers.
39-36, 34-31, 29-26, 24-21	SD15-0	I/O, CMOS	SRAM Data Input/Output Ports. These 16 bi-directional ports are used to read data from or write data into the SRAM.
2	R_W	O, CMOS	Write Enable. The write enable input is active low during write cycle to SRAM.
1	G_	O, CMOS	Read Enable. The read enable input is active low during read cycle to SRAM.

Table 5-8. Buffer Memory Configuration Pin (5 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
156-155	MSIZE1-0	I, TTL	Memory Size. These two pins select buffer memory size. [MSIZE1, MSIZE0]='00' : 16 Kbytes; '01' : 64 Kbytes; '10' : 256 Kbytes; '11' : 128 Kbytes (after rev E)
157	AUTOSIZE	I, TTL	Auto Sizing. When asserted high, this pin activates the Macronix Proprietary auto-sizing algorithm to adjust buffer area dynamically.
159-158	FWDMODE1-0	I, TTL	Forward mode. [FWDMODE1, FWDMODE0]= '00' : full-packet-store-and-forward; '01' : 64-byte-store-and-forward; '10' : half-duplex-and-forward; '11' : full-duples-and-forward mode.

Table 5-9. Address Field Access Pins (22 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
114-111	PKTD0-7_A	O, CMOS	Packet Data from Port A. These pins, synchronous to the MII clock RXCLK_A, display the Port A packet data on the aligned byte boundary every two RXCLK_A cycles for each byte.
108-109	ABYTE1-0_A	O, CMOS	Address Byte from Port A. These two pins, synchronous to RXCLK_A, whose binary value indicates that DA, SA, or data is present on PKT0-7_A. [ABYTE1, ABYTE0]='00' : Idle; ='01' : Data; ='11' : Source Address; ='10' : Destination Address;
107	ABT_A	I, TTL	Abort Packet from Port A. This pin is asserted to signal the FEBC to abort forwarding packet from Port A. In Fast Forward mode of FEBC, the assertion of this signal must be acknowledged by FEBC before the complete receipt of the 64 bytes of data; otherwise a fragment may be sent into the segment due to the late assertion.
86-89 91-94	PKTD0-7_B	O, CMOS	Packet Data from Port B. These pins, synchronous to the MII clock RXCLK_B, display the Port B packet data on the aligned byte boundary every two RXCLK_B cycles for each byte.
97-96	ABYTE0-1_B	O, CMOS	Address Byte from Port B. These two pins, synchronous to RXCLK_B, whose binary value indicates that DA, SA, or Data is present on PKT0-7_B. [ABYTE1, ABYTE0]='00' : Idle; ='01' : Data; ='11' : Source Address; ='10' : Destination Address;
98	ABT_B	I, TTL	Abort Packet from Port B. This pin is asserted to signal the FEBC to abort forwarding packet from Port B. In Fast Forward mode of FEBC, the assertion of this signal must be acknowledged by FEBC before the complete receipt of the 64 bytes of data; otherwise a fragment may be sent into the segment due to the late assertion.

Table 5-10. LED Pins (2 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
104	JAMLED_A	O, CMOS	JAM LED Port A. Active Low. This pin which is capable of driving LEDs directly denotes that the Port A receive buffer is full. For better visibility, the ON and OFF time of the LEDs should be at least 80 and 20 ms respectively.
101	JAMLED_B	O, CMOS	JAM LED Port B. Active Low. This pin which is capable of driving LEDs directly denotes that the Port B receive buffer is full. For better visibility, the ON and OFF time of the LEDs should be at least 80 and 20 ms respectively.

Table 5-11. PHY Configuration Pins (pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
105-106	PHY1-0_A	I, TTL	PHY of Port A. [PHY1_A, PHY0_A] ='00' : 100BASE T4; ='01' : MII; ='10' : 100BASE-FX; ='11' : 100BASE-TX.
100-99	PHY1-0_B	I, TTL	PHY of Port AB [PHY1_A, PHY0_B] ='00' : 10Base(7_wire); ='01' : MII; ='10' : 100BASE-FX; ='11' : 100BASE-TX.

Table 5-12. CPU Interface (19 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
60-53	CDAT[7:0]	I/O	CPU Data. 8-bit CPU data.
51-44	RegSel[7:0]	I, TTL	CPU Address. This pin selects internal registers.
43	RDY_	O/Z	Register Latch. This pin is asserted low by the FEBC to terminate a read or write cycle.
42	CS_	I,TTL	Chip Select. This pin enables the read or write access to the registers
41	REGR_W	I, TTL	Register Read Or Write. This pin indicates Read or Write on the registers

Table 5-13. Miscellaneous Pins (2 pins)

PIN#	PIN NAME	TYPE	DESCRIPTION
160	BPDIS	I, TTL	Back Pressure Disable:This pin, active high, disables the back pressure mechanism.
102	RESET_	I, TTL	Reset. Active low. This signal is an output from the system to reset all the logic on the chip.

Table 5-14. Test Pins/ Power/ Ground, 22 pins

PIN#	PIN NAME	TYPE	DESCRIPTION
83-4	TEST1-0	I, TTL	Test pins. [TEST1, TEST0] ='00' : notmal operation, back pressure=2; '01', '10' : internal functions checking; '11' : normal operation, back pressure=∞;
128, 95, 85, 82, 73, 35, 25	VCC		5V Power Supply.
148, 140 121, 115, 110, 103, 90, 81, 80, 61, 52, 40, 30, 20	GND		Ground.

6.0 OPERATION DESCRIPTION

The MX98742 FEBC is equipped with user-configurable modes which provides media flexibility or 100BASE-TX, 100BASE-FX, T4, MII, and 10BASE-T by using pins PHY0-1_A and PHY0-1_B. Three types of operations for FEBC are illustrated below:

6.1 BUILD-IN BRIDGE APPLICATION

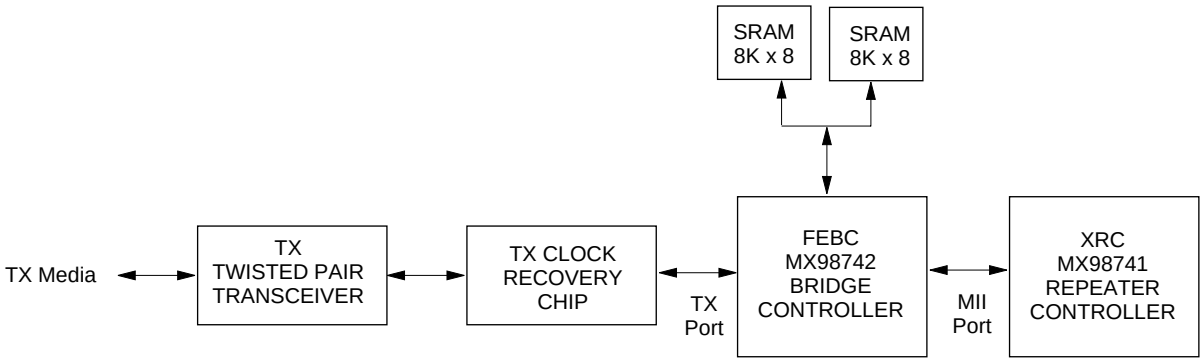


Figure 6-1. TX Connection With MX98741

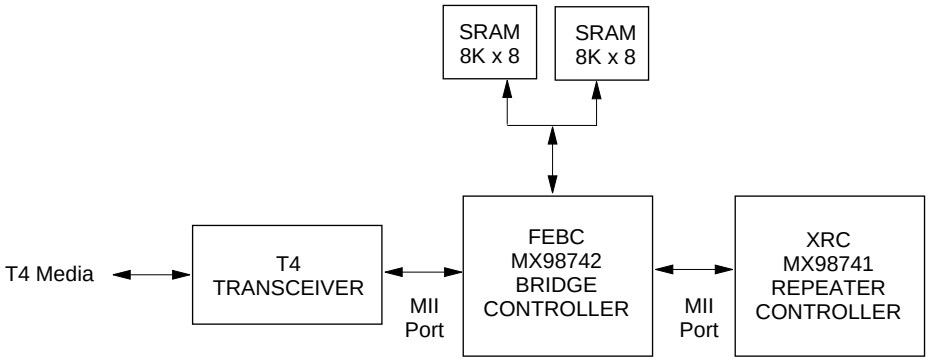


Figure 6-2. T4 Connection With MX98741

6.2 SPARE MII APPLICATION

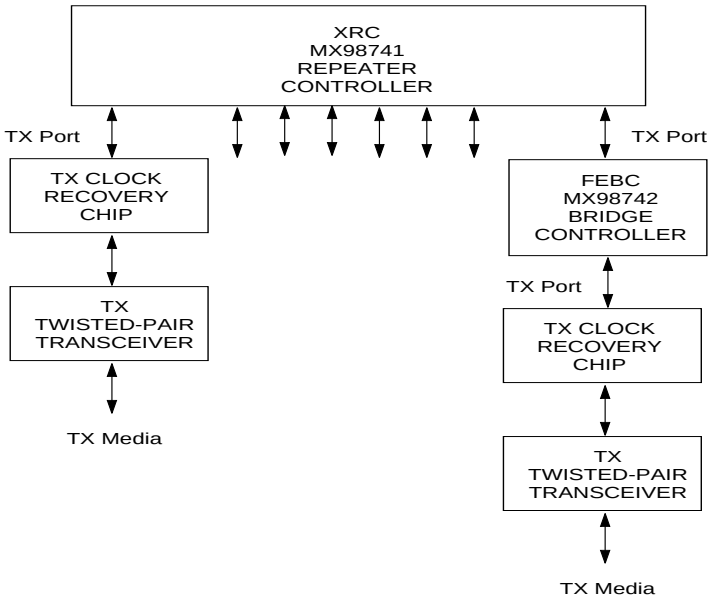


Figure 6-3. Alternative TX Connection With MX98741

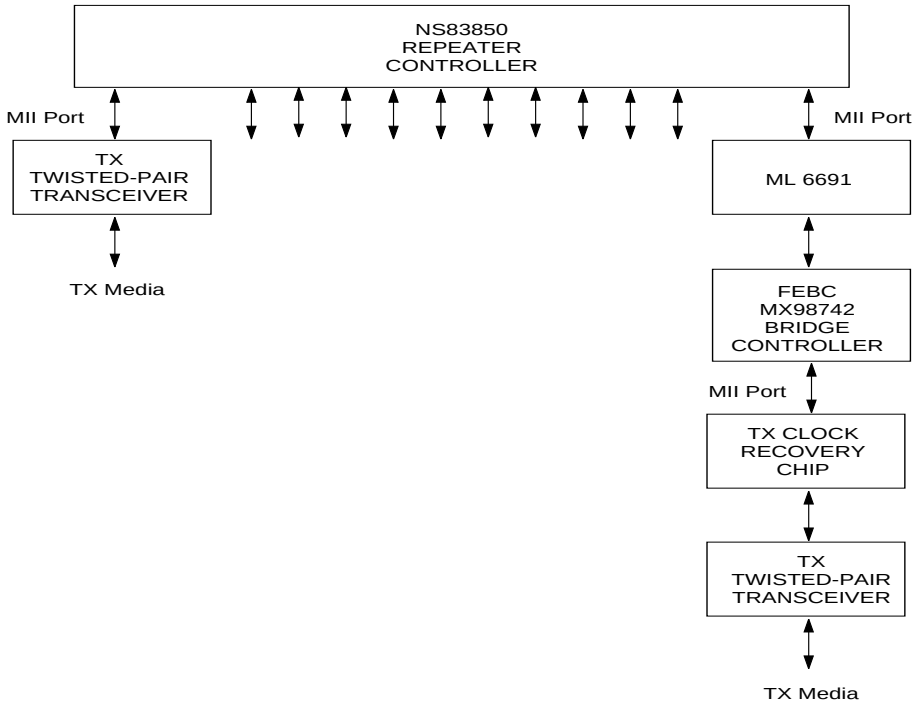


Figure 6-4. TX Connection With NS83850

6.3 STAND-ALONE BRIDGE APPLICATION

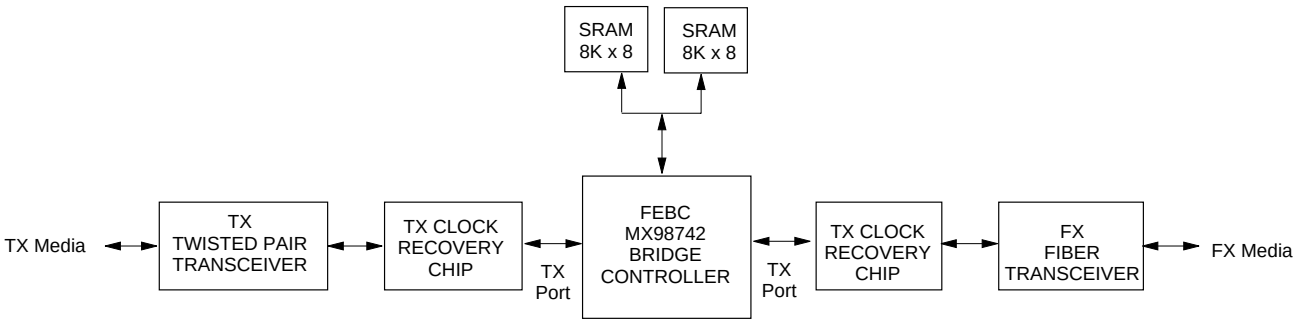


Figure 6-5. TX/FX Bridging

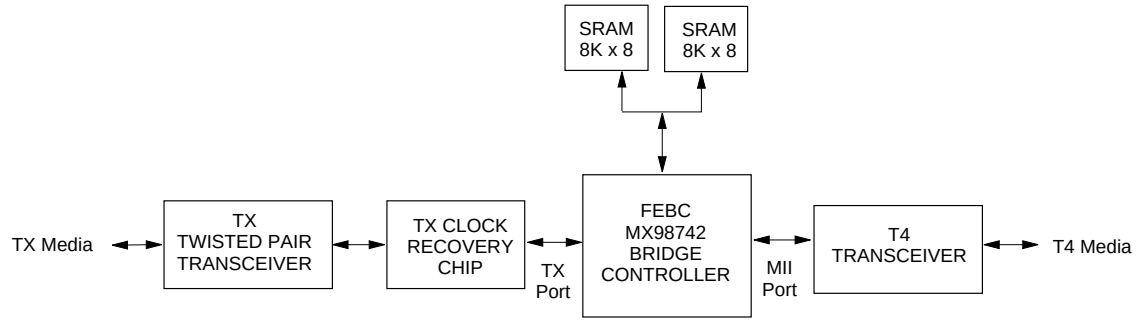


Figure 6-6. TX/T4 Bridging

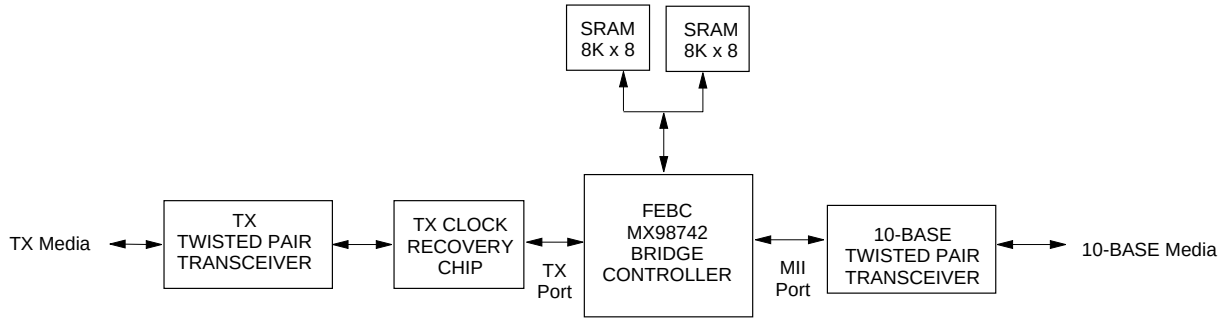


Figure 6-7. TX/10 BASE-T Bridging

6.4 CLOCK CONNECTION TO THE FEBC

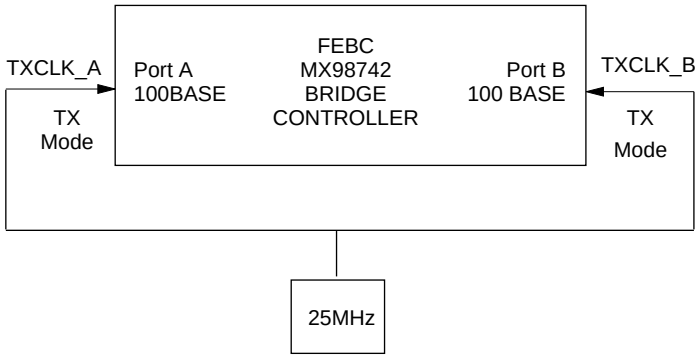


Figure 6-8. TX/TX Mode

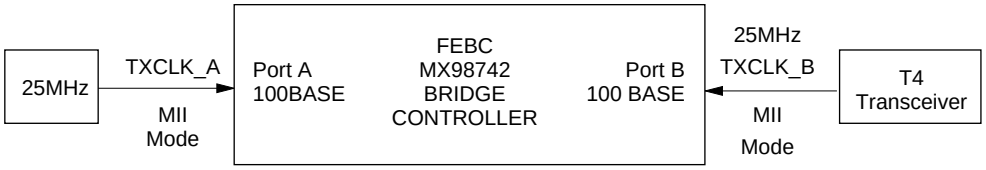


Figure 6-9. MII/MII Mode

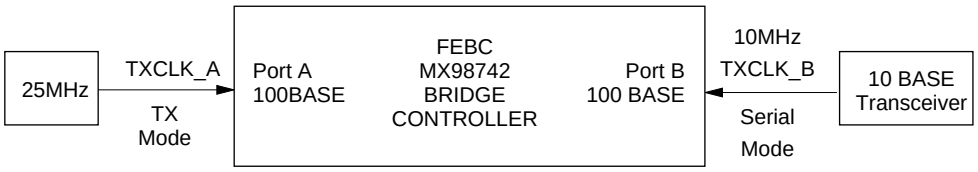


Figure 6-10. TX/Serial Mode

6.5 ML6691-MX98742 INTERFACE

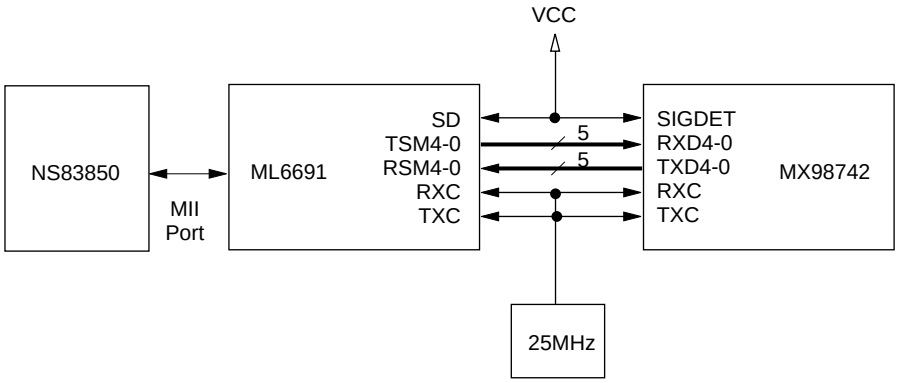


Figure 6-11. ML6691-MX98742 Interface

7.0 PHYSICAL INTERFACE AND SELECTION

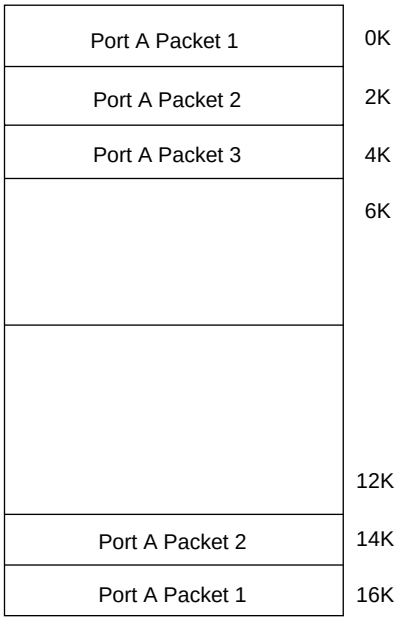
The FEBC provides 4 physical interfaces on port A and B. The TX/FX interfaces can be connected to a repeater controller's TX port or a TX PHY chip. The T4 interface is connected to a repeater controller's T4 port only.
The speed selection algorithm is described in the following table:

PHY1	PHY0	PHY Selection
0	0	Port A : T4; Port B : 10BASE (7_wire)
0	1	MII
1	0	FX
1	1	TX

8.0 BUFFER MANAGERMENT

8.1 BUFFER CONFIGURATION

The FEBC requires a minumum of 16K-byte buffer which has to be implemented with high-speed (25 ns or faster) SRAMs. A 16K-byte buffer SRAM is configured initially as the following:



The first 2 bytes of each buffer is for the status storage. The FEBC writes the packet length in the storage at the end of receiving. A 'bad' packet is rejected at the end and the buffer is reclaimed. If both sides are selected at 100Mps after reset, the buffer sizes for A and B are equal. However, if port B is operated at 7_wire mode, then the ratio of the two buffer sizes of the 100Mbps and 10Mbps is 7:1. In the Macronix Proprietary auto-sizing mode, the FEBC can dynamically adjust the buffer area size. For example, if buffer A is full and buffer B is still available; buffer A will grow into buffer B's area, and vice versa.

8.2 BUFFER ACCESS

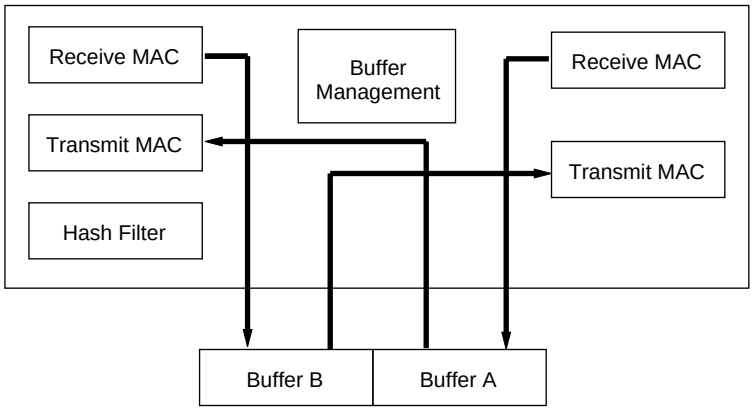


Figure 8-1. Simplified Block Diagram

The minimum size of a packet buffer is 2 Kbytes; therefore, a maximum-size packet, 1518 bytes can always be accommodated once a buffer is available. Combined with back-pressure flow control, a packet will never be lost due to buffer overflow. The A buffer starts with an address 0, and the port B buffer starts with the maximum address e.g. 16k. The accesses from both ports are interleaved to guarantee the bandwidth. The buffer memory access has 4 modes: (1) receiving from A, transmitting to B, (2) receiving from B, transmitting to A, (3) receiving from A, receiving from B, (4) transmitting to A, transmitting to B.

If port A buffer is full and CRS_A is high, then a JAM packet which length is 1024 bytes will be sent out to generate collision in A segment. JAM packet will be sent continuously until a buffer space is available. The total number of JAM sequences that can be sent consecutively is programmable. Once the terminal count is reached, no more JAM sequences are sent, and the flow-control JAM mechnism is disabled. Consequently any new packets sent from the network are lost. The JAM mechanism of port A will be restored if the associated buffer is available again.

If auto-sizing is enabled, the buffer boundary will be changed according to the need. For example, if A buffer is full and B buffer still has an unused space adjacent to A buffer, then A buffer will get one packet buffer (2KByte) from B buffer. The packet buffer B space that is assigned to A segment will remain unless B buffer segment has a need to reclaim it. The starting address of the last packet buffer in A segment can be read from a status register through register access pins.

9.0 FILTERING FUNCTIONS, FORWARDING MODES AND EXTERNAL FILTERING FUNCTIONS

9.1 FILTERING FUNCTIONS

FEBC provides a total of six filtering functions. Filters 1, 2, 3, and 4 can be implemented simultaneously, while Filters 4, 5, and 6 can be implemented simulneously:

1. Broadcast Packet Filter:Packets with all 1's in the 48-bit Destination Address will not be forwarded.
2. Multicast Packet Filter:Packets with '1' in the Group address bit will not be forwarded. This does not include Broadcast packets.
3. Self-Addressing Packet (DA=SA) Filter:Packets with same Destination Address and Source Address will not be forwarded.
4. 512-bit Hash Filter:The Destination Address of an incoming packet is fed through the standard Ethernet 32-bit CRC function. The 9 most significant bits of the decoded results are used to index a unique hash-filtering bit in the hash table. If the index bit is set, the packet is filtered (not forwarded). The packet is forwarded only when the index bit is cleared.
5. Inverse Broadcast Filter:Packets with 1's in the 48-bit Destination Address as well as hash filtered packets will be forwarded.
6. Inverse Multicast Packet Filter:Packets with '1' in the Group Address bit as well as hash filtered packets will be forwarded. This does not include Broadcast packets.

All the possible combinations of the above mentioned filtering schemes are listed below:

Table 9-1.

	B	M	S	H	IB	IM	DESCRIPTION
1	0	0	0	0	0	0	All packets are accepted.
2	0	0	0	1	0	0	Hash-filtering addressed packets are filtered.
3	0	0	1	0	0	0	Self-addressing packets are filtered.
4	0	0	1	1	0	0	Hash-filtering & self-addressing packets are filtered.
5	0	1	0	0	0	0	Multicast addressed packets are filtered.
6	0	1	0	1	0	0	Multicast & Hash-filtering addressed packets are filtered.
7	0	1	1	0	0	0	Multicast & Self-addressing packets are filtered.
8	0	1	1	1	0	0	Multicast, Self-addressing, & Hash-filtering packets are filtered.
9	1	0	0	0	0	0	Broadcast addressed packets are filtered.
10	1	0	0	1	0	0	Broadcast & Hash-filtering addressed packets are filtered.
11	1	0	1	0	0	0	Broadcast, Self-filtering addressed packets are filtered.
12	1	0	1	1	0	0	Broadcast, Self-addressing & Hash-filtering packets are filtered.

13	1	1	0	0	0	0	Broadcast, Multicast addressed packets are filtered.
14	1	1	0	1	0	0	Broadcast, Multicast & Hash-filtering packets are filtered.
15	1	1	1	0	0	0	Broadcast, Multicast & Self-addressing packets are filtered.
16	1	1	1	1	0	0	Inverse Broadcast & Inverse Multicast addressed packets are accepted.
17	0	0	0	0	0	1	Inverse Multicast addressed packets are filtered.
18	0	0	0	0	1	0	Inverse Broadcast addressed packets are filtered.
19	0	0	0	0	1	1	Inverse Multicast & Inverse Broadcast addressed packets are filtered.
20	0	0	0	1	0	1	Hash-filtering & Inverse Multicast addressed packets are filtered.
21	0	0	0	1	1	0	Hash-filtering & Inverse Broadcast addressed packets are filtered.
22	0	0	0	1	1	1	Hash-filtering, Inverse Brocast & Inverse Multicast packets are filtered.

Note: B : Broadcast Packet Filter; M : Multicast Packet Filter; S : Self-Addressing Packet Filter;
H : 512-bit Hash Filter; IB : Inverse Broadcast Filter; IM : Inverse Multicast Packet Filter.

9.2. FORWARDING MODES

Two forwarding modes are implemented:

1. Full-Packet Store and Foward:In this mode, a packet is forwarded only after the complete packet is received. An ill-formed packet will be discarded and the buffer reclaimed.
2. 64-byte-store-and-Forward:In the 64-byte mode. the FEBC attempts to forward a packet once the first 64 bytes are received without collision. This method introduces lower latency but carrier the risk of forwarding an ill-formed packet into next segment. This mode is not valid if there are still packets inside the buffer need to be transmitted.
3. Half-duplex-and-Forward (Test Mode 1):In this mode, no buffer memory is required. The data from one port is transmitted to another port directly. Collision sensed on one port will cause JAM sequence to be generated for as long as it lasts. This mode is useful when the bridge is used as a timing device to connect different PHY devices. If 100 meter UTP cable is attached to the bridge, the other end must be a DTE.
4. Full-duplex-and-forward-mode (Test Mode 2):In this mode, no buffer memory is required. The bridge functions strictly as a relay. The data can flow toward both directions at the same time. Both PHY interfaces to port A and Port B must be TX or FX and the collision detection in PCS is disabled. No flow control mechansim is implemented.

9.3. EXTERNAL FILTERING FUNCTIONS

The incoming packet is displayed on the PKTD7-0 starting at the data. The two pins ABYTE1 and ABYTE0 indicates the content of PKTD7-0. Destination Address and Source Address of a packet received can be easily extracted from PKT D7-0 according to hte following table:

ABYTE1	ABYTE0	PKT7-0
1	0	Destination Address
1	1	Source Address
0	1	Data
0	0	Idle

The forwarding action can be terminated by asserting ABT_A or ABT_B. The FEBC's response to the assertion of ABT depends on the timing. The ABT functions are independent of forwarding modes and filtering modes. Upon receipt of the asserted ABT signal, the FEBC will either (1) reclaim the buffer if transmitting has not started or (2) terminate transmission immediately and result in incomplete packet being forwarded.

10.0 MAC

The two MACs in the FEBC are IEEE 802.3 compliant except the following:
(1) A JAM packet could be sent to a segment to suppress more traffic until at least one buffer is available.
(2) The length of the JAM packet is 1024 bytes.
The back pressure function can be disabled by pulling BP_DIS pin high. The MAC does not expect CRS to be looped back while transmitting; i.e. the MAC can work with RXEN doubling as CRS.

11.0 REGISTERS

There are 8-bit registers in FEBC, that can be selected through REGSEL[7:0]

REGSEL[7:0]	REGISTER DESCRIPTION	R/W
0000, 0000	Reset Register	R/W
0000, 0001	JAM Control Register	R/W
0000, 0010	Forward Mode Register	R/W
0000, 0011	Filtering Mode Register	R/W
0000, 0100	JAM Counter A - upper 8-bit	R
0000, 0101	JAM Counter A - lower 8-bit	R
0000, 0110	JAM Counter B - upper 8-bit	R
0000, 0111	JAM Counter B - lower 8-bit	R
0000, 1000	Buffer Status	R

0000, 1001	Reserved	R
0000, 1010	Reserved	R
0000, 1011	Reserved	R
0000, 1100	Reserved	R
0000, 1101	Reserved	R
0000, 1110	Reserved	R/W
0000, 1111	Reserved	R/W
0001, 0000-0011, 1111	Reserved	
0100, 0000	Hash Filter byte 0_A	R/W
0100, 0001-0111, 1110	Hash Filter byte 1-62_A	R/W
0111, 1111	Hash Filter byte 63_A	R/W
1000, 0000-1011, 1111	Reserved	
1100, 0000	Hash Filter byte 0_B	R/W
1100, 0001-1111, 1110	Hash Filter byte 1-62_B	R/W
1111, 1111	Hash Filter byte 63_B	R/W

11.1 RESET REGISTER (R/W)

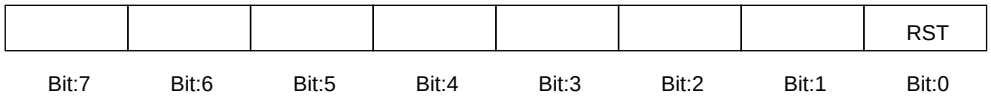


Table 11-1 Reset Register R/W

BIT(S)	SYMBOL	DESCRIPTION	R/W
0	RST	Reset 1:Reset (disable)FEBC. 0:Not reset (disable)FEBC. After power-up reset, RST is cleared to "0".	R/W
1-7	Reserved	Don't care.	

11.2 JAM CONTROL REGISTER (R/W)

JAS1	JAS0	JADIS		JBS1	JBS0	JBDIS	
Bit:7	Bit:6	Bit:5	Bit:4	Bit:3	Bit:2	Bit:1	Bit:0

JAS1 and JAS0 are the JAM selection bits for port A. These two bits determine the number of consecutive JAM packets sent to port A for flow-control. Each JAM packet is 1024 bytes which is less than Jabber timer. After the count is up, no more JAM will be sent to a busy segment, and the flow-control jamming mechanism is disabled. It will be enabled again once one packet buffer is available. JBS1 and JBS0 are the JAM selection bits for port B. These two bits determine the number of consecutive JAM packets sent to port B for flow-control. Each JAM packet is 1024 bytes which is less than Jabber timer. After the count is up, no more JAM will be sent to a busy segment, and the flow-control jamming mechanism is disabled. It will be enabled again once one packet buffer is available.

Table 11-2 JAM Control Register R/W

BIT(S)	SYMBOL	DESCRIPTION			R/W
7-6	JAS1-0	JAM Selection Port A			R/W
		JAS1	JAS0	Number of Consecutive JAM into port A	
		0	0	2 (default)	
		0	1	4	
		1	0	8	
		1	1	infinity	
5	JADIS	JAM Port A is Disabled 1:JAM function on port A is disabled. 0:JAM function on port A is enabled. This bit is valid only if BPDIS pin is tied low; JADIS is cleared to '0' after power-up reset.			R/W
4	Reserved				
3-2	JBS1-0	JAM Selection Port B			R/W
		JBS1	JBS0	Number of Consecutive JAM into port A	
		0	0	2 (default)	
		0	1	4	
		1	0	8	
		1	1	infinity	
1	JBDIS	JAM Port B is Disabled 1:JAM function on port B is disabled. 0:JAM function on port B is enabled. This bit is valid only if BPDIS pin is tied low; JADIS is cleared to '0' after power-up reset.			R/W
0	Reserved				

11.3 FILTERING MODE REGISTER

BCSF	MCSF	SAF	HF	IBCSF	IMCSF		
Bit:7	Bit:6	Bit:5	Bit:4	Bit:3	Bit:2	Bit:1	Bit:0

After power-up reset, no filtering is performed at all and all packets are forwarded.

Table 11-3 Filtering Mode Register R/W

BIT(S)	SYMBOL	DESCRIPTION	R/W
7	BCSF	Broadcast Address Packet Filter 1:Enable broadcast address packet filter; broadcast packets will not be forwarded. 0:Not enable broadcast address packet filter. BCSF is cleared to '0' after power-up reset.	R/W
6	MCSF	Multicast Address Packet Filter 1:Enable multicast address packet filter; multicast packets will not be forwarded. 0:Not enable Multicast address packet filter. MCSF is cleared to '0' after power-up reset.	R/W
5	SAF	Self Address Packet Filter 1:Enable self-address packet filter; self-addressed packets will not be forwarded. 0:Not enable self-address packet filter. SAF is cleared to '0' after power-up reset.	R/W
4	HF	Hash Filter 1:Enable hash filter packet filter; selected packets will not be forwarded. 0:Not enable hash filter packet filter. HF is cleared to '0' after power-up reset.	R/W
3	IBCSF	Inverse Broadcast Address Packet Filter 1:Enable inverse broadcast address packet filter; only broadcast packets and packets which pass hash-filter (if HF='1') will not be forwarded. 0:Not enable inverse broadcast address packet filter. IBCSF is cleared to '0' after power-up reset.	R/W

2	IMCSF	Inverse Multicast Address Packet Filter 1:Enable inverse multicast address packet filter; only multicast packets and packets which pass hash-filter (if HF='1') will not be forwarded. 0:Not enable inverse multicast address packet filter. IMCSF is cleared to '0' after power-up reset.	R/W
1-0	Reserved		

11.4 FORWARD MODE REGISTER

OVRD						FMS1	FMS0
Bit:7	Bit:6	Bit:5	Bit:4	Bit:3	Bit:2	Bit:1	Bit:0

Table 11-4 Forward Mode Register R/W

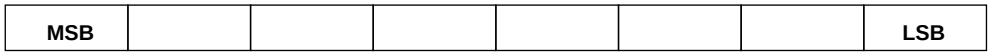
BIT(S)	SYMBOL	DESCRIPTION	R/W
7	OVRD	Over-ride 1:Over-ride the forwarding mode selected by FWDMODE(1:0). 0:Not over-ride the forwarding mode. OVRD is cleared to '0' after power-up reset.	R/W
6-2	Reserved		
1-0	FMS1-0	Forward Mode Selection FMS1 FMS0 Forward Mode Slection 0 0 Full-Packet-Store-and-Forward 0 1 64-Byte-Store-and-Forward 1 0 Half-Duplex-and-Forward 1 1 Full-Duplex-and-Forward	R/W

11.5 JAM COUNTER REGISTER (R/W)

MSB							LSB
Bit:7	Bit:6	Bit:5	Bit:4	Bit:3	Bit:2	Bit:1	Bit:0

There are two 16-bit counters inside FEBC counting the number of JAM events on each port. The value of these counters are displayed through 4 8-bit JAM Counter Register. After reset, all the counter values are cleared to 0.

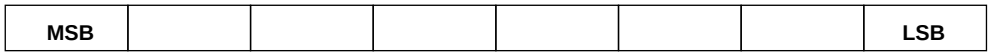
11.6 BUFFER STATUS REGISTER (R/W)



These 8 bits display the starting address of the last packet buffer in Buffer A. For example:

A:B	MEMORY SIZE	STAT[7:0]	LAST A BUFFER ADDR RANGE
1:1	16K bytes	0000, 0011 (3)	6K-8K
1:1	64K bytes	0000, 1111 (15)	30K-32K
1:1	256K bytes	0011, 1111 (63)	126K-128K
7:1	16K bytes	0000, 0110 (6)	12K-14K
7:1	64K bytes	0001, 1011 (27)	54K-56K
7:1	256K bytes	0110, 1111 (111)	222K-224K

11.7 HASH FILTER REGISTER



The 512-bit hash table are implemented by 64 8-byte hash filter register. CRC [23:31] are indexed to these register.

CRC [23:31]	HASH REGISTER BYTE	HASH REGISTER BIT
0_0000_0000	0	0
0_0000_0001	0	1
0_0000_0010	0	2
0_0000_1000	1	0
0_0000_1001	1	1
0_0000_1010	1	2
1_1111_1101	63	5
1_1111_1110	63	6
1_1111_1111	63	7

After reset, all the hash-filtering bits are zeros and all packets are forwarded. The addresses to be blocked are transformed by the CRC hash algorithm. The hash-filtering bits that correspond to the Destination Addresses to be rejected are then set to ones.

12.0 ABSOLUTE MAXIMUM RATINGS

Table 12-1 Absolute Maximum Rating

RATING	VAULE
Supply Voltage (VCC)	4.75 V to 5.25 V
DC Input Voltage (Vin)	-0.5 V to VCC + 0.5 V
DC Output Voltage (Vout)	-0.5 V to VCC + 0.5 V
Storage Temperature Range (TSTG)	-55 C to 150 C
Power Dissipation (PD)	375 mW
ESD Rating (Rzap = 1.5 K, Czap = 100 pF)	2000 V
Ambient Operating Temp	0 C to 70 C

Note:

1. Stress greater than those listed under Absolute Maximum Ratings may cause pemanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Preliminary, subject to change.

13.0 DC CHARACTERISTICS

Table13-1 Supply Current

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
ICC	Average Active (TXing/ RXing) Supply Current	CLOCK=25MHz	--	75	mA
IDD	Static IDD Current	CLOCK=Undriven	--	1	mA

Table13-2 DC Characteristics of Inputs, Output, Tri-states

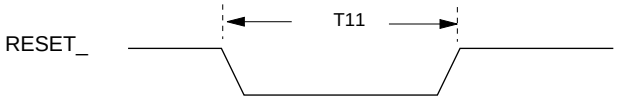
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vil	Maximum Low Level Input Voltage		--	0.8	V
Vih	Minumum High Level Input Voltage (except SD15-0, CDAT7-0)		2.2	--	V
Iin	Input Current	VI=VCC/GND	-1.0	1.0	uA
Vil	Maximum Low Level Input Voltage for RESET_	Schmitt	--	0.6	V
Vih	Minumum High Level Input Voltage for RESET_	Schmitt	2.7	--	V

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voh	Minimum High Level Output Voltage for PKT7-0_A, PKT7-0_B, ABYTE1-0_A, ABYTE1-0_B	Ioh=-2mA	2.4	--	V
Vol	Maximum Low Level Output Voltage for PKT7-0_A, PKT7-0_B, ABYTE1-0_A, ABYTE1-0_B	Iol=-2mA	--	0.4	V
Voh	Minimum High Level Output Voltage for TDAT4-0, TDAT4-0_B, TXEN_A, TXEN_B, TX1PR1-0, TX3PR1-0, TX4PR1-0; OE_A, BPDIS, CS_, REGR_W, SA16-0, SD15-0, R_W, G_	Ioh=4mA	2.4	--	V
Vol	Maximum Low Level Output Voltage for TDAT4-0, TDAT4-0_B, TXEN_A, TXEN_B, TX1PR1-0, TX3PR1-0, TX4PR1-0; OE_A, BPDIS, CS_, REGR_W, SA16-0, SD15-0, R_W, G_	Iol=4mA		0.4	V
Voh	Minimum High Level Output Voltage for RDY_	Ioh=-8mA	2.4	--	V
Vol	Maximum Low Level Output Voltage for RDY_	Iol=8mA	--	0.4	V
Voh	Minimum High Level Output Voltage for CDAT7-0	Ioh=-12mA	2.4	--	V
Vol	Maximum Low Level Output Voltage for CDAT7-0	Iol=12mA	--	0.4	V
Voh	Minimum High Level Output Voltage for JAMLED_A JAMLED_B	Ioh=-16mA	2.4	--	V
Vol	Maximum High Level Output Voltage for JAMLED_A JAMLED_B	Ioh=16mA		0.4	V
Ioz	Maximum Tri-State Output Leakage Current	VOUT=VCC/GND	-10.0	10.0	uA

14.0 AC CHARACTERISTICS AND WAVEFOEMS

AC Test Conditions

Input Pulse Level : VIH/VIL=2.4V/0.4V
Input Rise and Fall Time : tr/tf=2ns/2ns
Timing Reference Level : 1.5V



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	Assertion time for RESET_	2400		ns

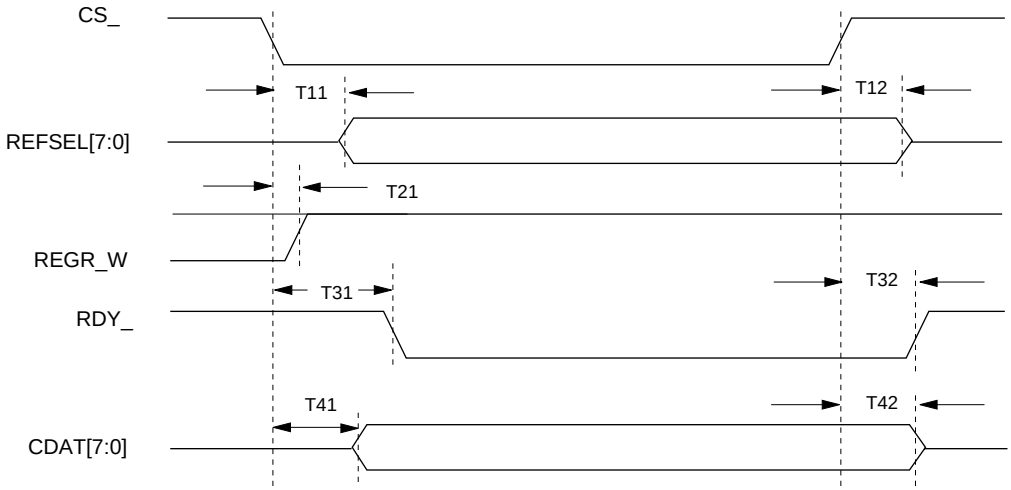


Figure 14-1.Register Read

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	CS_low to REGSEL[7:0] valid		40	ns
T12	REGSEL[7:0] hold from CS_high	0		ns
T21	CS_low to REGR_W high		35	ns
T31	CS_low to RDY_low	120	160	ns
T32	CS_high to RDY_high impedance	40	80	ns
T41	CS_low to CDAT[7:0] valid		150	ns
T42	CDAT[7:0] hold from CS_high	0		

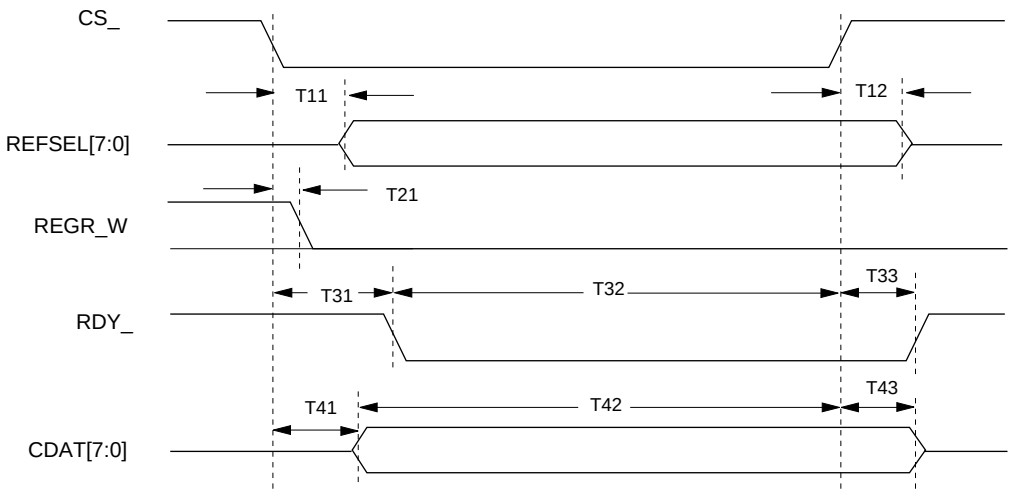


Figure 14-2.Register Write

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	CS_low to REGSEL[7:0] valid		40	ns
T12	REGSEL[7:0] hold from CS_high	5		ns
T21	CS_low to REGR_W high		35	ns
T31	CS_low to RDY_low	80	120	ns
T32	RDY_low to CSzx_high	10		ns
T33	CS_high to RDY_high impedance	40	80	ns
T41	CS_low to CDAT[7:0] valid		75	ns
T42	CDAT[7:0] valid to CS_high	15		
T43	CDAT[7:0] hold from CS_high	5		ns

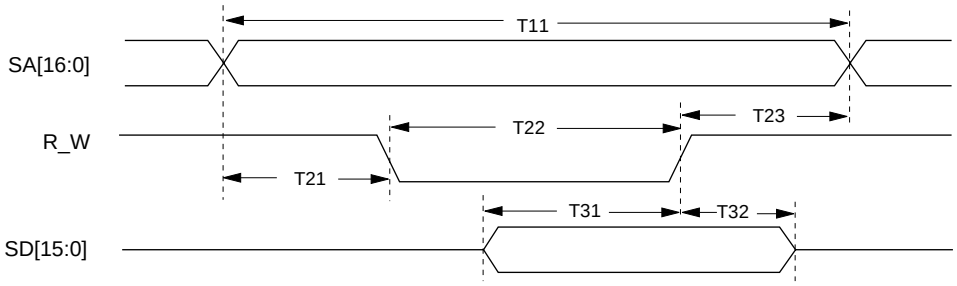


Figure 14-3 Memory Write

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	Write cycle time	78	82	ns
T21	Address setup time	13	19	ns
T22	Write pulse width	39	41	ns
T23	R_W high to address change	20	25	ns
T31	Data setup time	33	38	ns
T32	Data hold time	1	7	ns

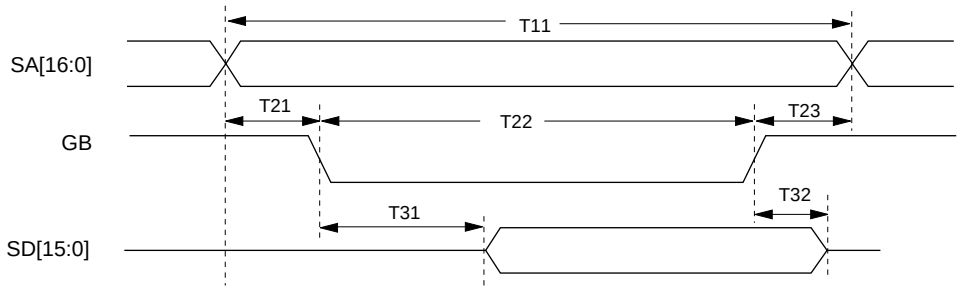


Figure 14-4 Memory Read

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	Read cycle time	78	82	ns
T21	Address setup time	13	19	ns
T22	Pulse width of GB	39	41	ns
T23	Read recoverty time	21	26	ns
T31	Output enable to SD[15:0] valid	0	25	ns
T32	Output disable to SD[15:0] high impedance	0	20	ns

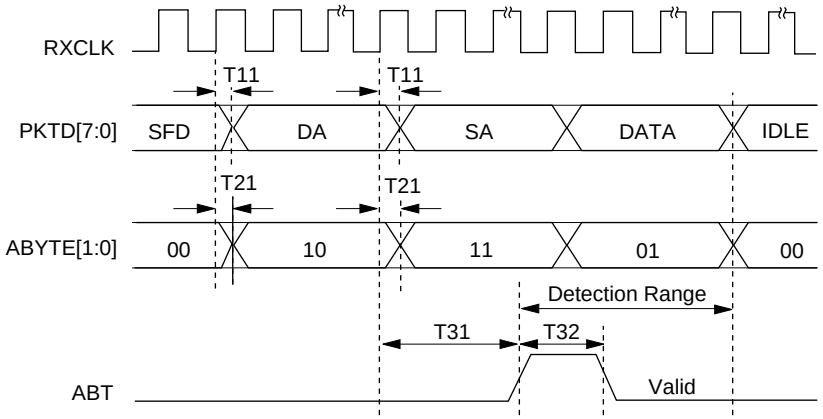


Figure 14-5 CAM Interface Timing For 100BASE, RXCLK=25MHz or 2.5 MHz

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	RXCLK rising edge to PKTD[7:0] valid		12	ns
T21	RXCLK rising edge to ABYE[1:0] valid		12	ns
T31	RXCLK rising edge to ABT high	230 (Note 2) 2300 (Note 3)		ns
T32	ABT pulse width	80 (Note 2) 800 (Note 3)		ns

Note 1: Any ABT pulse sampled by RXCLK's rising edge during detection range will purge current receiving packet.
Note 2: For RXCLK=25MHz
Note 3: For RXCLK =2.5 MHz

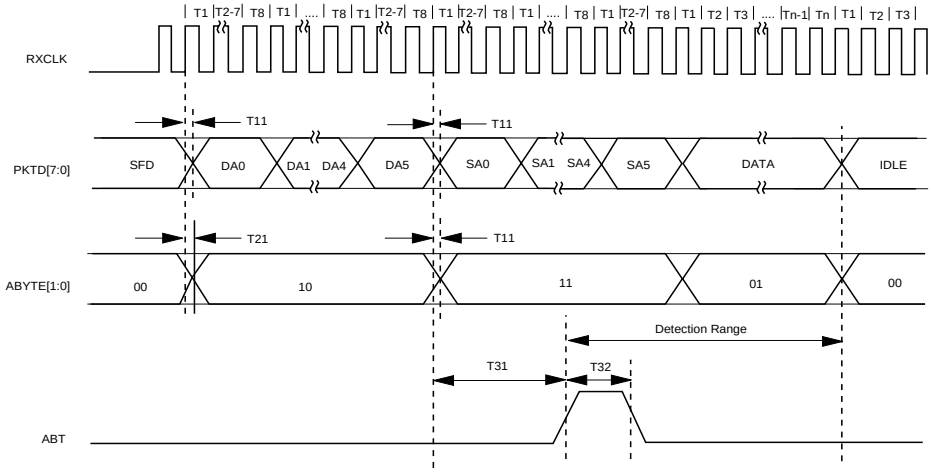


Figure 14-6 CAM Interface Timing For 10BASE, RXCLK=10MHz (10 Base)

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	RXCLK rising edge to PKTD[7:0] valid		12	ns
T21	RXCLK rising edge to ABYTE[1:0] valid		12	ns
T31	RXCLK rising edge to ABT high	2300		ns
T32	ABT pulse width	800		ns

Note 1: Any ABT pulse sampled by RXCLK's rising edge during detection range will purge current receiving packet.

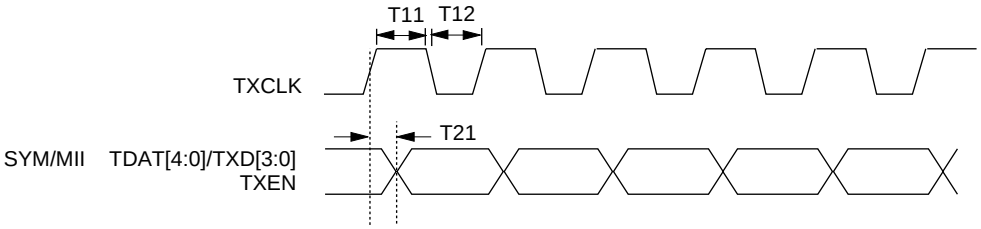


Figure 14-7 Transmit Signals Timing

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11*	TXCLK high for 25MHz (100BASE-TX)	14	26	ns
T12*	TXCLK low for 25MHz (100BASE-TX)	14	26	ns
T21*	TXD, TXEN to TXCLK rising edge	10	23	ns

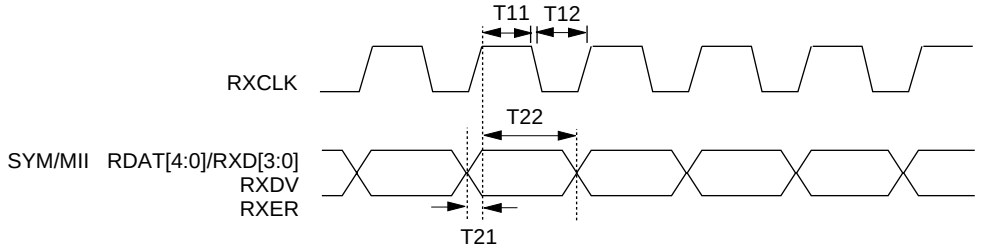


Figure 14-8 Receive Signals Timing

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	RXCLK high for 25MHz (100BASE-TX)	14	26	ns
T12	RXCLK low for 25MHz (100BASE-TX)	14	26	ns
T21	RXD, RXDV & PXER setup time to RXCLK's rising edge	10		ns
T22	RXD, RXDV & RXER holg time to RXCLK'S rising edge	5		ns

*Note 1: The suty cycle of TXCLK should be between 35% and 65% inclusively.
2: The transmit timing T21 measured with 30 pf loading.

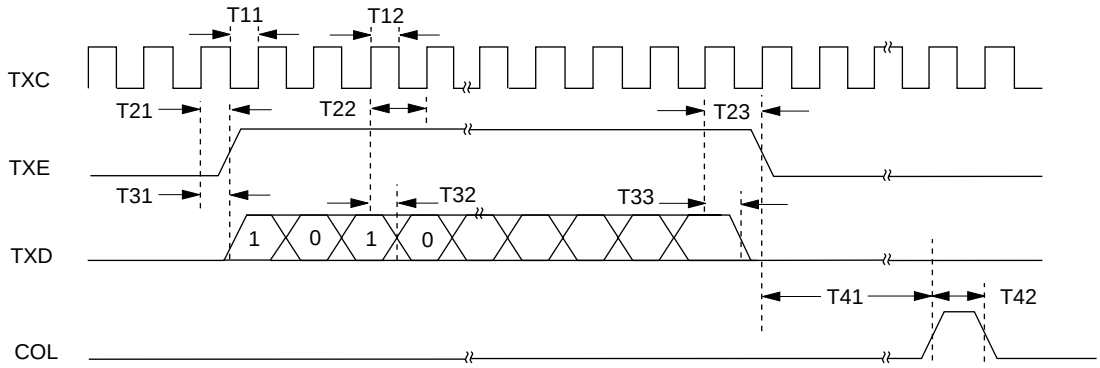


Figure 14-9 Serial Transmission With A Collision Detect Heartbeat

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	Transmit clock low time	36		ns
T12	Transmit clock high time	36		ns
T21	Transmit clock high to transmit enable high		45	ns
T22	Transmit clock cycle time	90	110	ns
T23	Transmit lock to TXE low		55	
T31	Transmit clock high to serial data valid		65	ns
T32	Serial data hold time from transmit clock high	6		ns
T33	Transmit clock to data low		55	ns
T41	TXE low to the start of the collision detect heartbeat	0	64*T22	ns
T42	Collision detect width	2*T22		ns

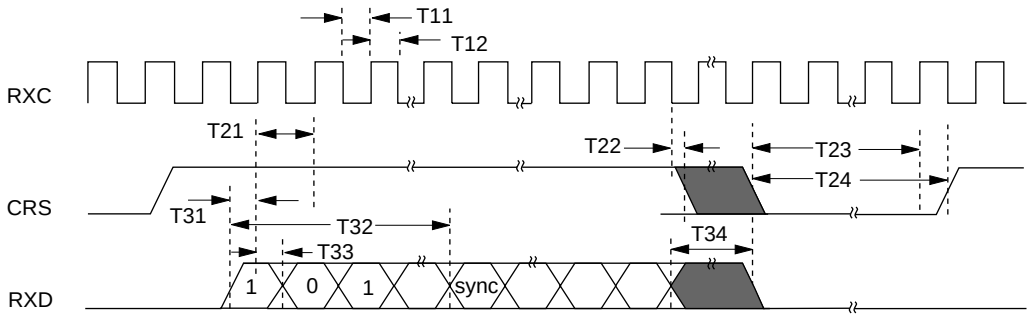


Figure 14-10 Serial Receive Timing

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	Receive clock low time	36		ns
T12	Receive clock high time	36		ns
T21	Receive clock cycle time	90	110	ns
T22	Receive clock to carrier sense low	0	1*T21	ns
T23	Minimum number of receive clocks after CRS low	3*T21		ns
T24	Receive recovery time		40*T21	
T31	Receive data setup time to receive clock high	20		ns
T32	First preamble bit to synchronize	8*T21		ns
T33	Receive data hold time from receive clock high	15		ns
T34	Maximum of allowed dribble bits/ clocks		5*T21	ns

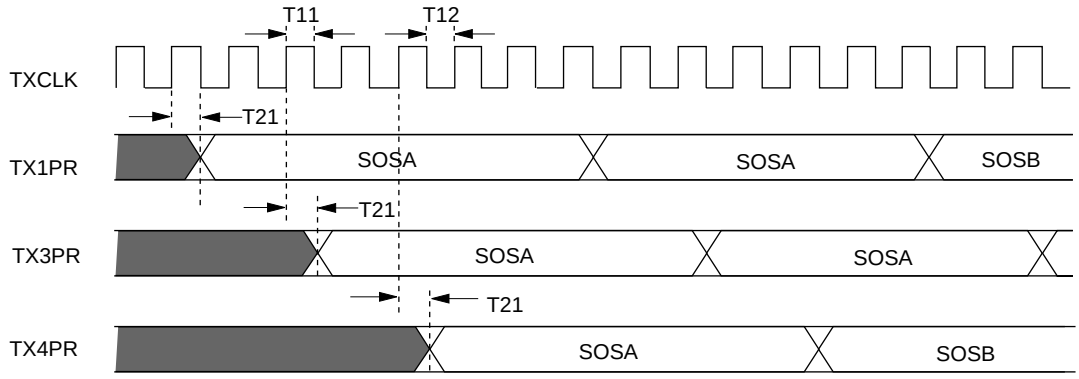


Figure 14-11 T4 Transmit Timing

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	TXCLK high for 25MHz	14	26	ns
T12	TXCLK low for 25MHz	14	26	ns
T21	TX pairs valid to TXCLK's risig edge	--	25	ns

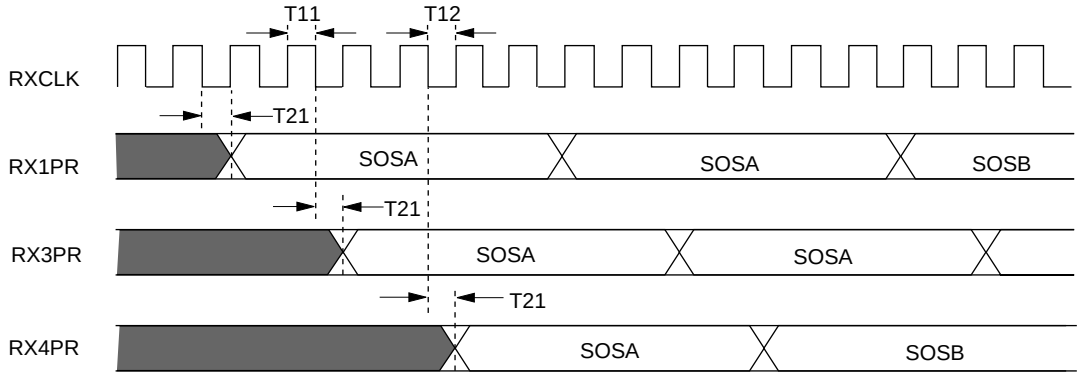


Figure 14-12 T4 Receive Timing

TA=0°C-70°C, VCC=4.75V-5.25V

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T11	RXCLK high for 25MHz	14	26	ns
T12	RXCLK low for 25MHz	14	26	ns
T21	RX pairs should be valid after RXCLK's falling edge	--	15	ns

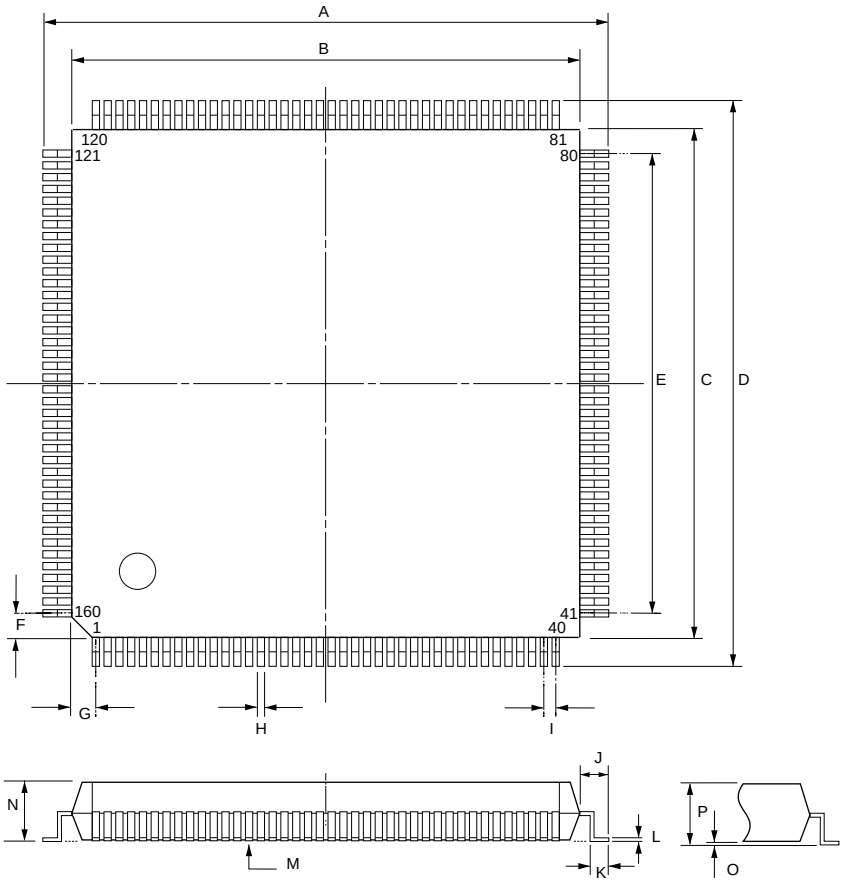
Note:The duty cycle of the RXCLK and TXCLK should be between 35% to 65% inclusively.

14.0 PACKAGE INFORMATION

160-Pin Plastic Quad Flat Pack

ITEM	MILLIMETERS	INCHES
A	31.20 ± .30	1.228 ± .012
B	28.00 ± .10	1.102 ± .004
C	28.00 ± .10	1.102 ± .004
D	31.20 ± .30	1.228 ± .012
E	25.35	.999
F	1.33 [REF]	.052 [REF]
G	1.33 [REF]	.052 [REF]
H	.30 [Typ.]	.012 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	1.60 [REF.]	.063 [REF.]
K	.80 ±.20	.031 ± .008
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	3.35 max.	.132 max.
O	.10 min.	.004 min.
P	3.68 max.	.132 max.

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.



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