DSLAM

VORTEX CHIPSET

DSLAM REFERENCE DESIGN: SYSTEM DESIGN

RELEASED

Issue 4

December, 2000

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REVISION HISTORY

Issue No.	Issue Date	Details of Change
4	December 2000	Replaced “metadriver” with “VORTEX Chipset Driver” for consistency with software driver documents. Better LVDS hot swap explanation and cell transfer, which is affected by setting OCAEN bit in register 0x0A of the S/UNI-DUPLEX at the very end of the chipset activation. Register write sequence is required. The sequence is already implemented with the VORTEX Chipset Driver on CD-ROM Ver 3.0.
3	September 2000	Updated with WAN Card Issue 3, Line Card Issue 3, Core Card Issue 3 and release of VORTEX chipset metadriver. Removed errors and typos. Updated LED description on front panel. Updated current supply to each DSLAM card.
2	February 2000	Block Diagram of Wan Card updated to include changes made to Wan Card reference design. Updated most obvious deficiencies and inconsistencies with present knowledge about DSLAM reference design. Also: replaced phrase “DSLAM chipset” with “VORTEX chipset”, replaced Core Card Block Diagram with updated one, updates to front panel drawings and shelf drawings.
1	August 1999	Creation of Document

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CONTENTS

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

LIST OF FIGURES

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

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1. TECHNOLOGY OVERVIEW

1.1. Introduction

PMC-Sierra's Digital Subscriber Line Access Multiplexer (DSLAM) is a network element that supports high bandwidth applications in the public telephone network and provides both data and voice over existing subscriber lines. DSLAMs are typically installed in a Telco central office (CO) or similar location, and provide the required ATM link to numerous xDSL (Digital Subscriber Line) modems. The Digital Subscriber Line solves the bandwidth bottleneck to homes or businesses, over existing twisted pair old copper telephone lines (POTS). Loading coils, typically present in those lines, must be removed, because they do not allow xDSL to be transported. This section of the network is known as the *Last Mile Solution* in digital data services.

The DSLAM Reference Design presents a multi-device entity that comprises rack-mounted shelves with 6U high plug-in cards. It also provides an overview of the DSLAM architecture based on the VORTEX chipset. The VORTEX chipset includes the following:

- PM7350 S/UNI-DUPLEX multiplexer
- PM7351 S/UNI-VORTEX multiplexer
- PM7326 S/UNI-APEX traffic manager (switch)
- Also, PM7324 S/UNI-ATLAS ATM layer solution (traffic policing device), which supplements VORTEX Chipset.

The DSLAM Reference Design shelf is a stand-alone entity that shows how the PMC-Sierra VORTEX chipset operates. The PMC-Sierra VORTEX chipset provides a cost-effective and compact solution for manufacturers of high-speed Internet access equipment.

1.2. DSLAM Reference Design Features

The DSLAM Reference Design features:

- traffic management, policing and OAM functionality with the S/UNI-APEX and S/UNI-ATLAS
- in-system demonstration of PMC-Sierra's 8- or 16-bit ANY-PHY Interface (extended Utopia L2, at up to 50 MHz clock rate)
- high-speed Low Voltage Differential Signaling (LVDS) interface up to 200 Mb/s

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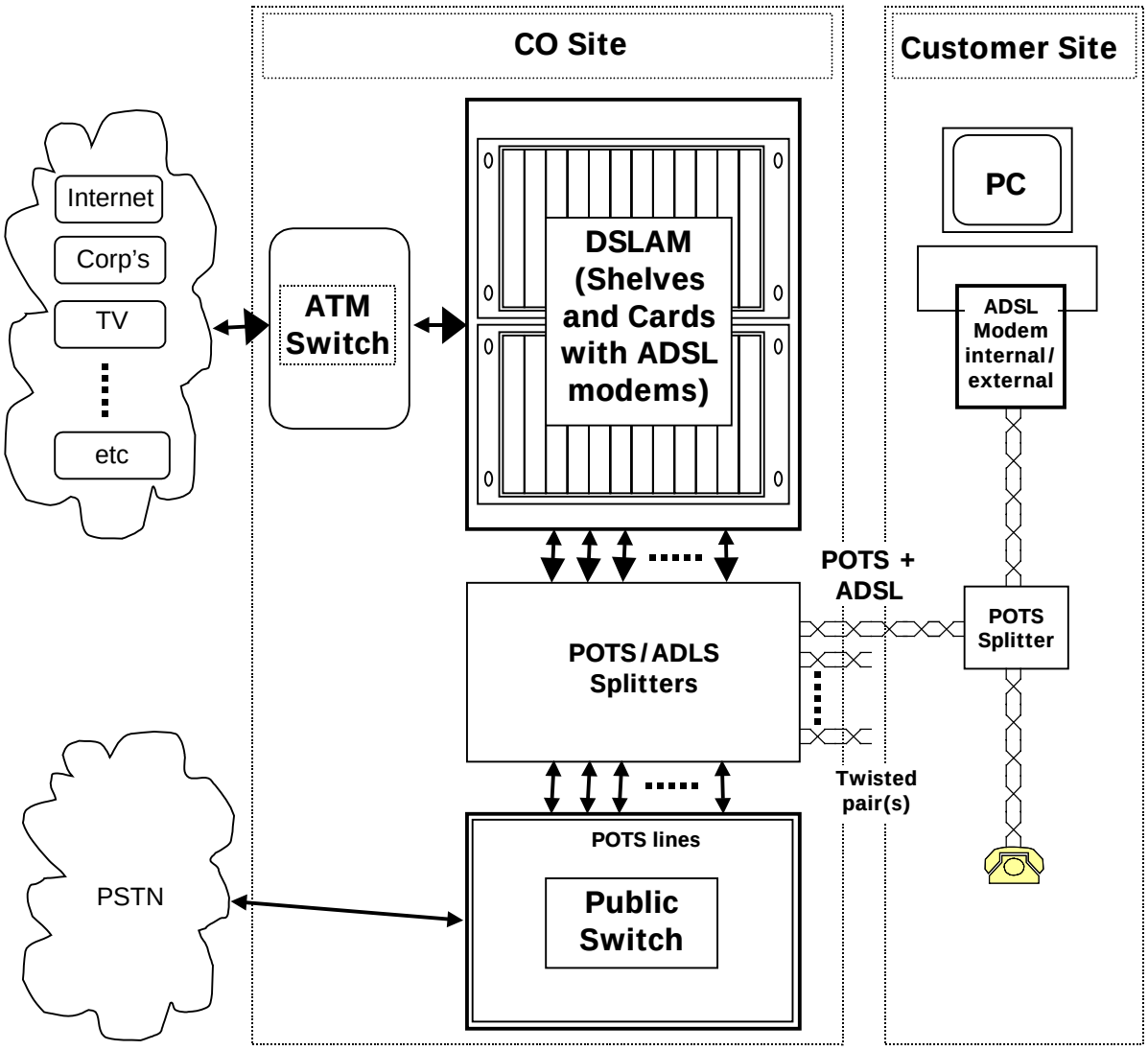
- 1:1 protection switching between the Core Card, the WAN up-link cards and the Line Cards
- 8 kHz synchronization method for the whole DSLAM system, including loop entities
- hot swap capability on all cards: power rails hot swap on WAN and Line Cards; power rails hot swap and software ready hot swap on Core Card.

1.3. Example of a DSLAM Connection in an ADSL Application

Figure 1 shows an example of a DSLAM connection in an ADSL application.

Figure 1. DSLAM-ADSL in the Public Telephone/Data Network



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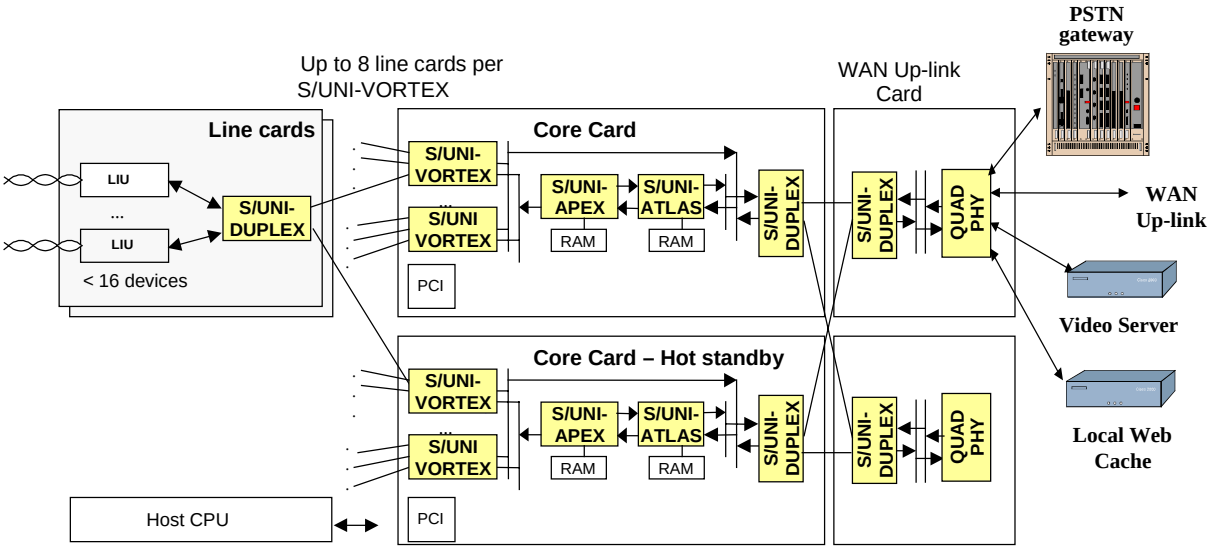
In the example, the DSLAM shelf is associated with a Public Switch of a telephony network. The downstream data flows from an ATM switch that connects different service providers to the xDSL network. POTS and xDSL signals are delivered to the customer over a twisted pair.

1.4. DSLAM Block Diagram

Figure 2 shows a typical application for the S/UNI-DUPLEX, S/UNI-VORTEX, S/UNI-APEX, and S/UNI-ATLAS. The system shows two Core Cards operating in a protection mode. One of the cards is in hot standby mode.

The DSLAM Reference Design Line Card supports sixteen LIU devices. The S/UNI-DUPLEX loop side that interfaces with the LIU is set to Data-and-clock. The WAN Card supports the S/UNI-DUPLEX with the Utopia L2 interface towards the Quad-PHY and WAN direction.

Figure 2. DSLAM Overview



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1.5. CompactPCI Shelves

The DSLAM Reference Design is based on the CompactPCI shelf form factor.

1.5.1. Shelf Types

Vendors provide various CompactPCI shelves, which are typically described as development shelves, system shelves, and portable shelves. Development shelves usually support four to eight card slots. System shelves usually support eight or sixteen card slots. Portable shelves support four to eight slots, and focus on developing a package that is easy to transport and provides protection against mechanical damage.

1.5.2. DSLAM Shelf

The DSLAM Reference Design shelf is built as a development shelf. The development shelf is basically a skeleton of the shelf, equipped with a backplane, a switching power supply, and minimal metal work, which allows for easier access to components for troubleshooting and development.

The DSLAM Reference Design cards and shelves are scalable entities with demonstration capability of as little as three cards in a single shelf, and a maximum size of sixteen Line cards, two WAN Cards and two Core Cards. 19-inch rack-mounted cPCI shelves with 20 cards. A single shelf solution shows limited functionality, but is built for ease of system demonstration. Each DSLAM Reference Design shelf, accommodating a Core Card, is equipped with a CPU card. This CPU is the PCI bus host processor.

The current DSLAM design uses a custom-made backplane (LVDS-backplane) to optimize connectivity for LVDS interfaces. This design may restrict some of the DSLAM cards to work on other types of the cPCI shelves. This Reference Design is an excellent example of a DSLAM entity, which proves DSLAM architecture can be used by customers as a starting point for building larger systems.

1.5.3. Rear Panel I/O

The custom LVDS-backplane is equipped with a rear panel I/O conenctor, at the first slot, allowing connection of periipherals for the host processor card. An example of the Rear Panel I/O interface is described in APPENDIX – A: REAR PANEL I/O.

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1.5.4. Hot Swap on cPCI backplane

The hot swap functionality is another important features built into the cPCI shelves. The cPCI connectors have staged pins and a mechanical switch built into the extraction handle. This enables a card in an operating shelf to be inserted or removed without data corruption to the system. The DSLAM Reference Design cards are hot swap compatible. The cards are hot-swap-ready as stated in the *Hot Swap Specification* (Draft) with limited functionality on backplane connectors. The WAN Card and Line Cards use only +5 V rails on the cPCI backplane and have the appropriate voltage/current ramping serial MOSFET transistors. Those cards have no PCI bus interface. The Core Card is equipped with +5 V and +3.3 V voltage/current ramping serial MOSFETs. The card is equipped with a precharging network on the PCI bus, as stated in the *Hot Swap Specification* (Draft). The Core Card is equipped with an ejector microswitch, blue LED, and active ENUM# line, making card hardware and softwarehot-swap-ready.

1.6. DSLAM Reference Design Package

Issue 3* of the DSLAM System Reference Design package includes the following contents:

- *DSLAM System Reference Design* document
- *Reference Design* documents for each card
- Schematics and layout for each card, accompanied with a bill of material
- Software driver for each PMC-Sierra's chip on the Core Card, VORTEX Chipset Driver (board level driver or metadriver) and some test routines.

* See the PMC-Sierra web site for the latest documents.

1.7. VORTEX Chipset Development Kits

The VORTEX Chipset Development Kits are available on request from PMC-Sierra, Inc., while quantity lasts. Two types of development sets are available: KitA – the Core Card only, and KitB - the Core Card and WAN Card.

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2. DSLAM REFERENCE DESIGN SHELF

This section introduces Core Card architecture, DSLAM Reference Design architecture, and a physical concept of the DSLAM Reference Design.

2.1. DSLAM Reference Design Architecture

The DSLAM Reference Design comprises four separate, application-specific card types:

- Core Card
- Line Card
- Wan Card and
- LVDS-backplane

2.1.1. DSLAM Reference Design Architecture Block Diagram

Figure 3 shows the block diagram that depicts the basics of this DSLAM Reference Design Shelf.

The very basic DSLAM configuration supported with this Reference Design consists of two Line Cards, two Core Cards, and two WAN Cards. The backplane allows a number of LVDS interfaces to be run with copper traces. Other LVDS connections can be done with external cables.

Ports P[1] on both WAN Cards are connected to corresponding ports P[1] on Core Cards. The Core Card can switch between the two WAN Cards by toggling S/UNI-DUPLEX ports. On the Loop side, Line Cards switch between Core Cards also by toggling S/UNI-DUPLEX ports.

The preferred interface between Line Cards and Core Cards, via the backplane, is through the S/UNI-VORTEX-1 (ports 1 and 2) on both Core Cards. A system built with more Line Cards uses up the remaining ports on S/UNI-VORTEX-1 and then on S/UNI-VORTEX-2.

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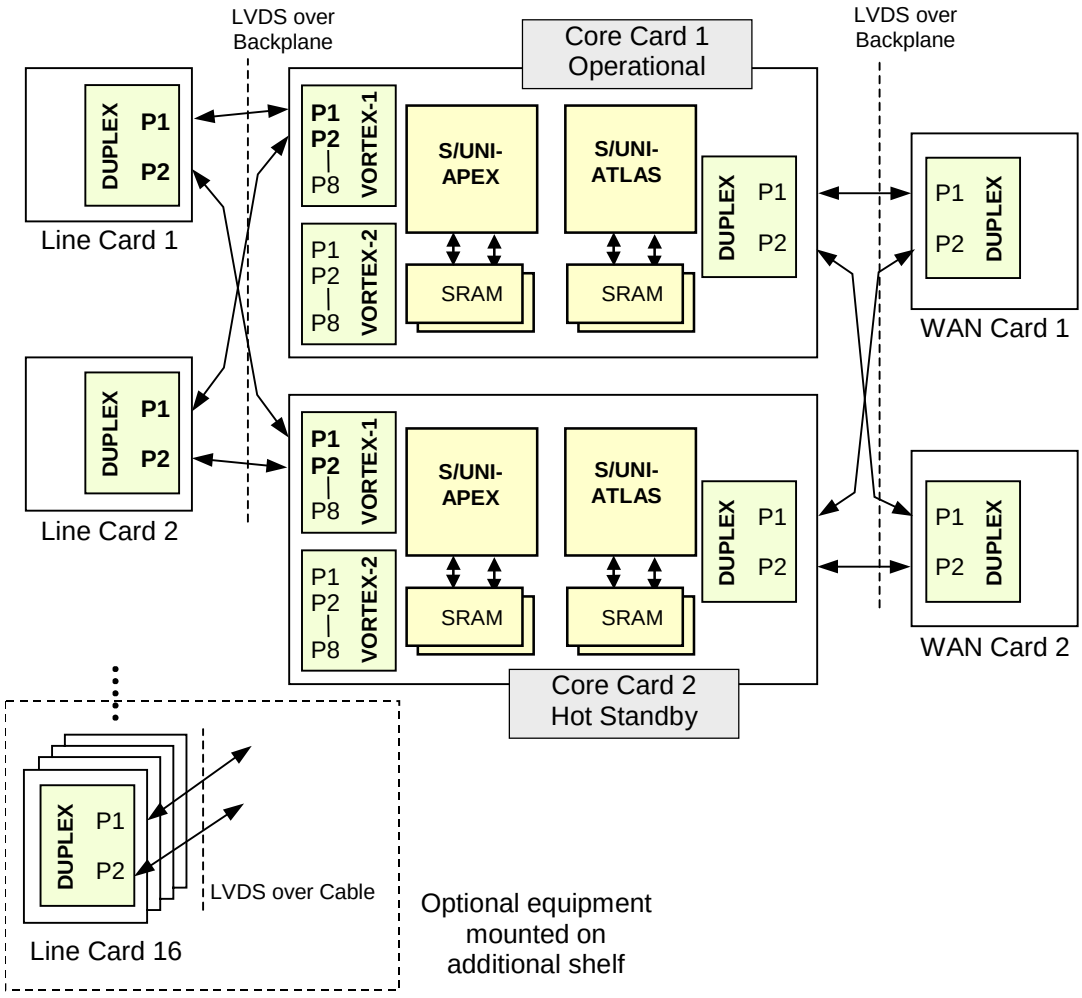
Figure 3. DSLAM Shelf Architecture Block Diagram



2.1.2. Core Card Architecture Block Diagram

This Reference Design is built around a single S/UNI-ATLAS with the S/UNI-APEX architecture used on the Core Card.

Figure 4 shows the Reference Design Core Card with the VORTEX chipset architecture.

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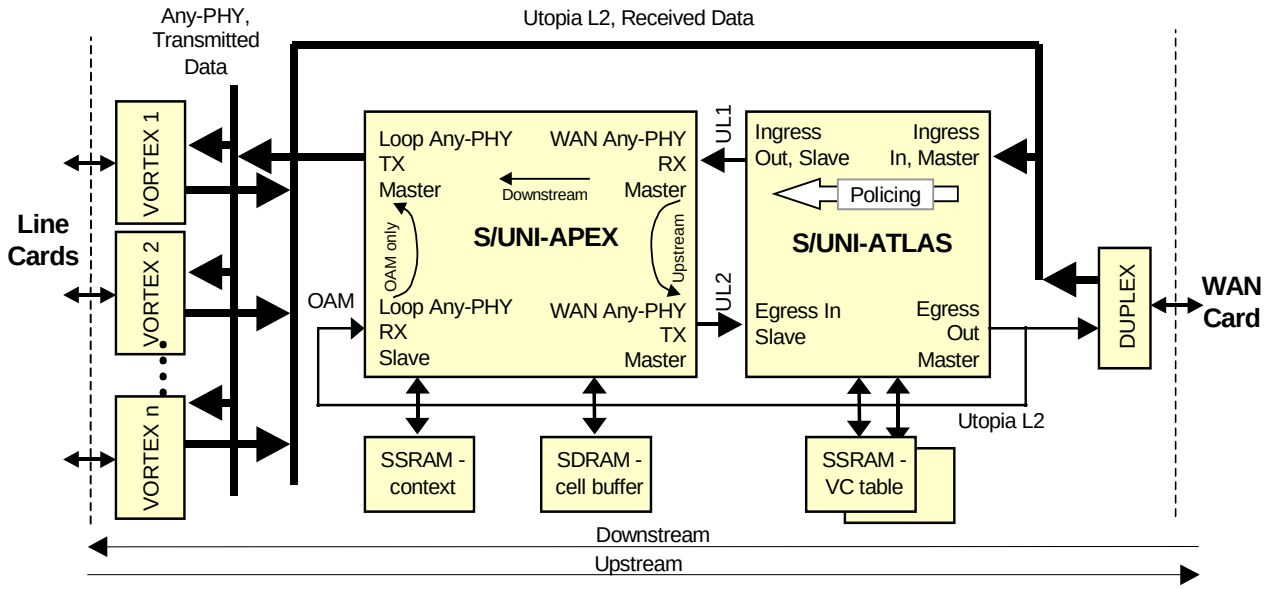
Figure 4. Core Card Architecture Block Diagram



The S/UNI-APEX and S/UNI-ATLAS are the focus point of this design. The downstream and upstream cells interfaces with the S/UNI-ATLAS through the same “Ingress In” port. The S/UNI-ATLAS communicates with the S/UNI-APEX via the UL1 port, in the Ingress direction. The “Loop Any-PHY Rx Slave” port on the S/UNI-APEX is connected to the WAN direction “Egress Out”, allowing flow of the OAM cells. The S/UNI-APEX switches data to the “Loop Any-PHY TX” or to the “WAN Any-PHY TX” ports as required for the cell destination. The Core Card communicates with Line Cards through a set of S/UNI-VORTEX devices. The interface to the network is done through the S/UNI-DUPLEX, followed by a WAN Card. The large size of the RAMs associated with the S/UNI-APEX and S/UNI-ATLAS supports ATM traffic management, traffic policing, OAM cell flow, and cell switching up to 2048 ports. For more information about the Core Card, see document [1].

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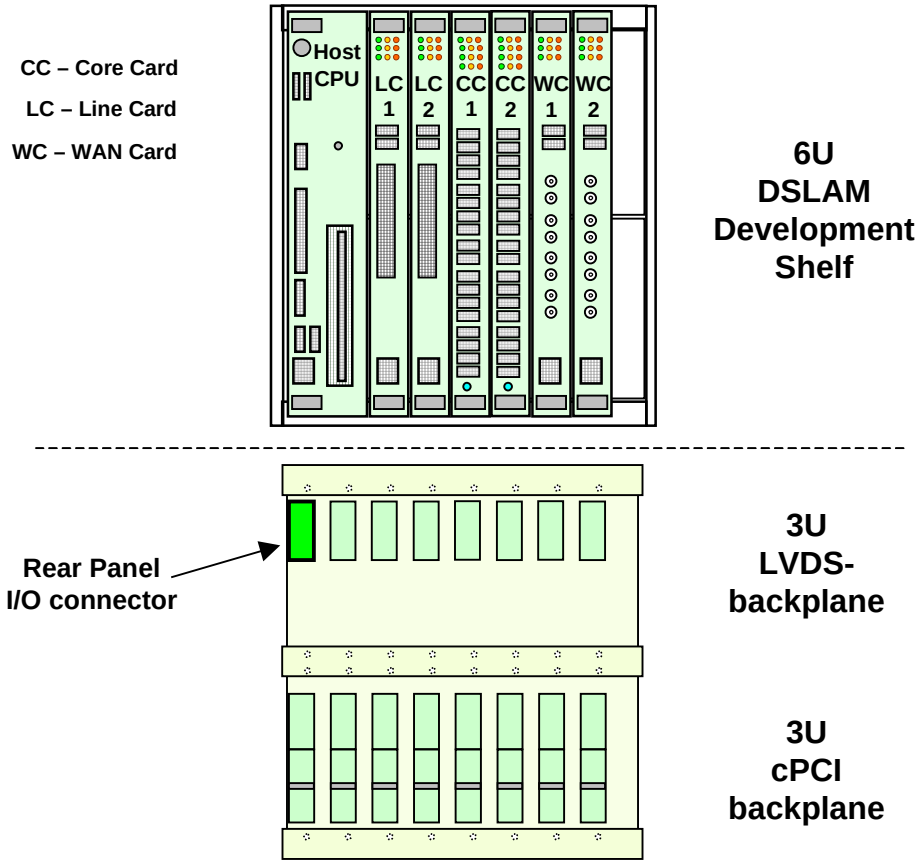
2.2. DSLAM Shelf Configuration

Figure 5 shows an example of card placement on the DSLAM Reference Design development shelf.

Figure 5. Development Shelf Configuration



The shelf is shown with a host processor card, two Line Cards (LC1, LC2), two Core Cards (CC1, CC2), and two WAN Cards (WC1, WC2). Backplanes are shown below the shelf. The upper 3U high board is a custom made entity that supports LVDS over the backplane. This board is called the “LVDS-backplane” throughout this document. The lower 3U high standard cPCI backplane supports PCI bus and power lines, and it is purchased on the market. The DSLAM LVDS-backplane is developed by PMC-Sierra, Inc., and it is a custom made design, specific to this DSLAM Reference Design.

The DSLAM Shelf may require forced air cooling system, if all cards are placed on the shelf. The host processor card may have forced airflow cooling at the Intel Pentium™.

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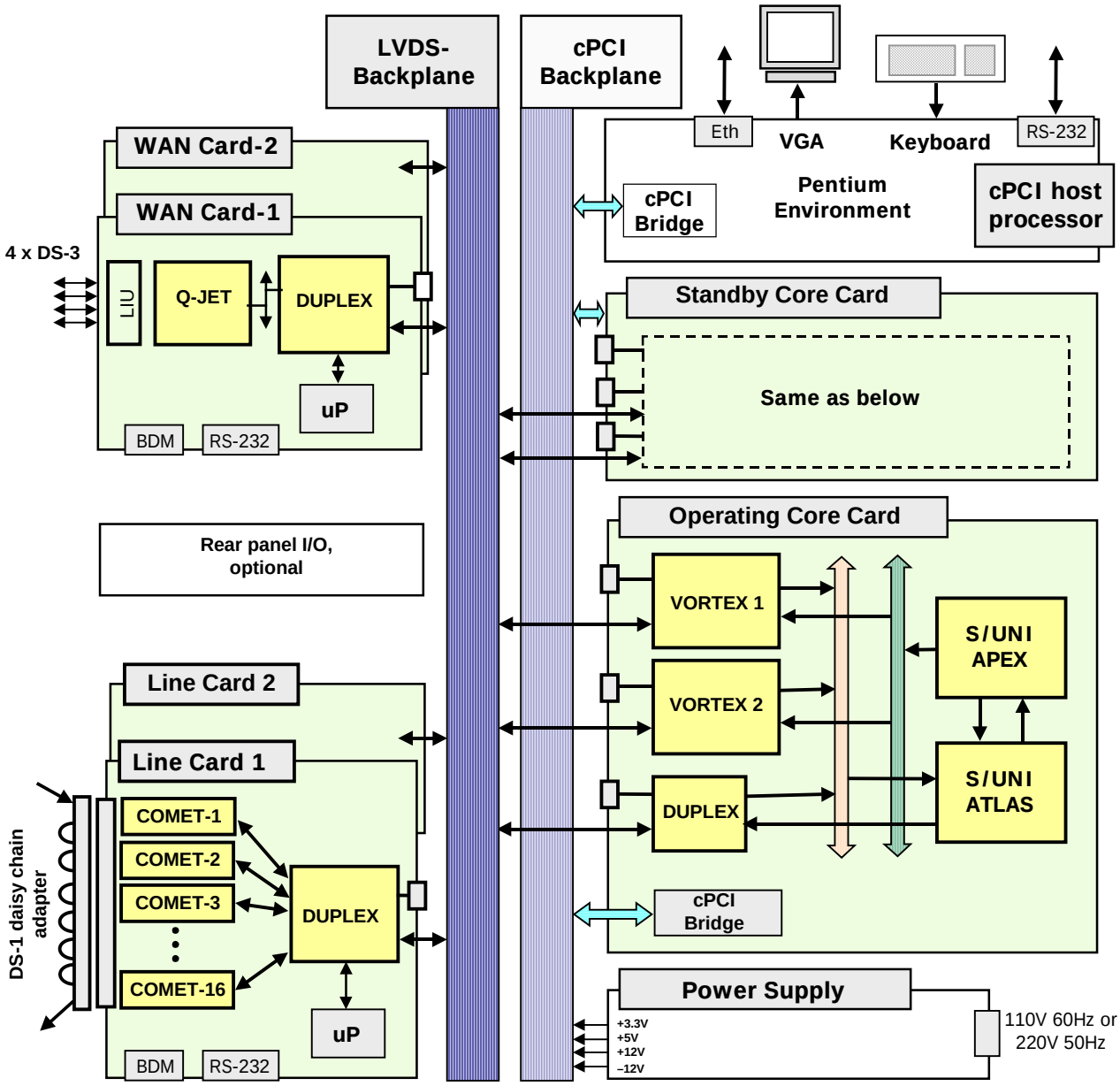
2.2.1. DSLAM System Block Diagram

Figure 6 shows block diagram of an example DSLAM Reference Design Shelf.

Figure 6. DSLAM Reference Design Shelf Block Diagram



The DSLAM Reference Design shelf assembly shown in Figure 5 and the shelf configuration shown in Figure 6 supports the following PMC-Sierra devices:

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S/UNI-DUPLEX, S/UNI-VORTEX, S/UNI-APEX, S/UNI-ATLAS, S/UNI-QJET, and COMET.

The DSLAM Shelf includes the following Reference Design cards:

- Operating Core Card — with two S/UNI-VORTEX'es, S/UNI-DUPLEX, S/UNI-ATLAS, and S/UNI-APEX.
- Standby Core Card — same as the Operating Core Card
- Line Card 1-2 — with 16 COMETs and one S/UNI-DUPLEX on each card
- WAN Card 1-2 — with S/UNI-DUPLEX and S/UNI-QJET
- DSLAM Backplane — custom backplane with J4 and J5

The purchased off-the-shelf components are:

- 6U high, aluminium shelf
- CPU card – based on the 233 MHz MMX Intel Pentium
- cPCI backplane with J1 and J2 connectors
- Power Supply
- Peripheral devices: VGA monitor and keyboard
- during development phase, additional PC and network server were used (PC with a Tcl/Tk environment interfacing with the host CPU through the serial port; the Lab Server allowing the download of metadriver test routines through the Ethernet port).

The clock-and-data interface on the S/UNI-DUPLEX is shown with sixteen COMETs (bit aligned serial data and clock). The Utopia L2 interface on the S/UNI-DUPLEX is shown with S/UNI-QJET on the WAN Card.

Both Core Cards are assembled and programmed to be identical. Core Cards interface with the CPU card via a 32-bit cPCI bus. The LVDS interface on Core Cards can be connected to the LVDS-backplane via the jumper field, which is set manually before card insertion. The jumper field configuration is shown in the schematic associated with the Core Card Reference Design document [1]. Core Cards can be placed into slots 5 or 6 on the DSLAM shelf and must be associated with host CPU card at slot 1.

The CPU card can only be at slot 1. This slot is always marked with a "Δ"(triangle).

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Line Cards 1 and 2 are identical. Cards can be placed primarily into slots 3 and 4, and, optionally, into any slot. The LVDS interface (on the Line Card) can be programmed for the backplane, if the Core Card is present on the shelf.

The WAN Cards are identical. Cards can be placed primarily into slot 7 or 8, and optionally into any slot. Slots 7 and 8 have additional WAN LVDS connections over the backplane to Core Card1 or Core Card2.

LVDS interface configuration on all cards is very flexible and can be configured to LVDS interface over the backplane only, over the front cables only, or mixed connection partially over the backplane and partially over cables. Any card can connect to another shelf over the front cable LVDS interface.

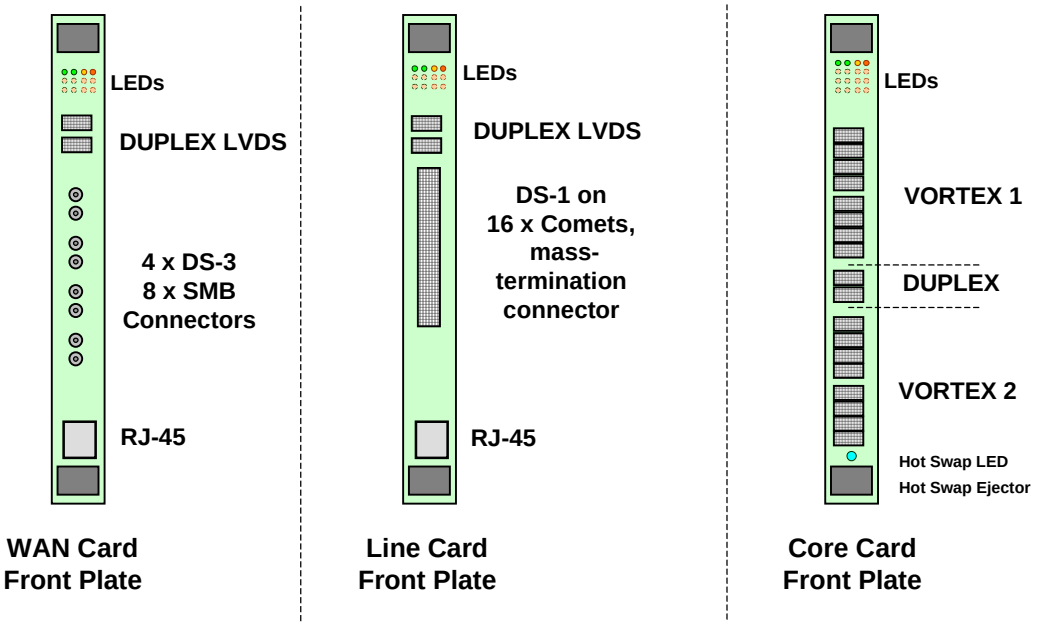
The jumper field configuration for Line Card and WAN Card are shown in corresponding schematics documents [2] and [3].

2.2.2. Front Plates on DSLAM Cards

The front plates on each DSLAM card have external dimensions as specified in cPCI document [13]. Plates are mechanically customized for each card.

Figure 7 shows an example of the front plates.

Figure 7. Front Plate for WAN, LC and CC Cards



The WAN Card is equipped with eight SMB connectors supporting four DS-3 interfaces. The front plate has a cutout for two IEEE 1394 connectors for the

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S/UNI-DUPLEX LVDS. The RJ-45 connector is used for the microprocessor serial port interface. Light emitting diodes (LEDs) show basic Card status. LEDs are placed at the top of the plate for best visibility.

The Line Card is equipped with a mass-termination connector that supports sixteen DS-1/E1 interfaces. The DS-1/E1 lines are connected in a daisy chain configuration with a custom connector sub-assembly. For more information, see the Line Card Reference Design document [2]. DS-1/E1 signals can be branched out of the mass-termination into individual DS-1/E1 bantam connectors with a cable harness or through a rack-mounted patch-panel. The Line Card is also equipped with two IEEE 1394 connectors that supports the S/UNI-DUPLEX LVDS connections. The RJ-45 connector is used for microprocessor serial port interface. The LEDs show basic Card status.

The Core Card is equipped with eighteen IEEE 1394 connectors (FireWire). The top eight connectors support S/UNI-VORTEX-1 LVDS. The center pair supports the S/UNI-DUPLEX LVDS, and the lower eight connectors support S/UNI-VORTEX-2 LVDS. The LEDs show basic status of the Core Card. The blue LED and lower ejection handle with a micro-switch are used for hot swap compatibility.

The 8 kHz timing reference (stratum clock) is supported only through internal header connectors, not accessible at the front panel.

The aluminum front plates are covered with silkscreen print. Labels identify connectors, LEDs, Card type, and manufacturer (PMC-Sierra, Inc.).

2.3. LVDS Interface

The LVDS interface is a key element in the DSLAM application using a high-speed serial communication link that runs up to 200 Mbps.

2.3.1. LVDS Introduction

Over the decades, the use of 5V power supply voltages has allowed simple interfacing between logic circuits of different technologies and manufacturers. However, lower supply voltages are required as integrated circuit technology migrates to a finer geometry. At the same time, the data rate has to be increased. Reducing supply voltages also reduces the power required to operate high-density IC circuits and therefore reduces the amount of heat that high-density circuits dissipate.

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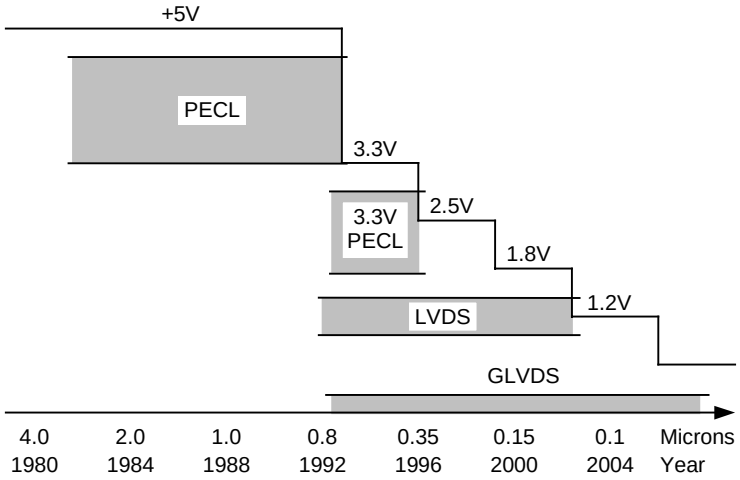
A perfect example of a reduced supply voltage and reduced logic voltage swing is the LVDS. The LVDS physical interface uses a 400mV signal swing around an offset voltage of 1.2V. In comparison, ECL and PECL signals use a 800mV signal swing and depend more on supply voltages. ECL requires a negative supply and PECL is referenced from the positive power supply rail (Vcc). Ground Referenced Impedance Matched (GRIM) Low Voltage Differential Signaling (GLVDS) is another method of fast data transfer with low power consumption and dissipation. GLVDS uses a 500mV power supply to provide a 250mV signal swing; however, the standards outlined here need verification.

Figure 8 shows the differential voltage swing for different low voltage logic signals.

Figure 8. Differential Voltage Swings



The S/UNI-DUPLEX and S/UNI-VORTEX devices both use the LVDS interface to communicate serial data at speeds of up to 200 Mbps.

Two standards define LVDS:

- IEEE P1596.3 Low Voltage Differential Signaling (LVDS) for Scalable Coherent Interface (SCI)
- ANSI/TIA/EIA-644 Electrical Characteristics of LVDS.

Both standards define the electrical characteristics of LVDS. The IEEE standard defines encoding for packet switching in the SCI protocol. Also, each standard is specified as physical media independent, which means the interface will operate properly as long as the media delivers the signal to the receiver within the specified noise margin and skew tolerance range.

Figure 9 shows a typical LVDS interface.

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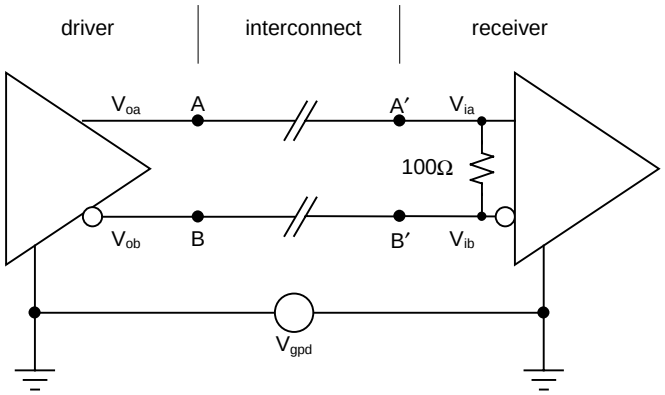
Figure 9. LVDS Interface



Each differential pair is a point-to-point connection and consists of a driver, interconnect and receiver. The low voltage swing driver signals (400mV single-ended maximum) enable high-speed operation and minimize power dissipation. Differential signals provide the low voltage swing with adequate noise margin and a large reduction in power dissipation. The large reduction in power dissipation allows for the integration of multiple interface drivers and receivers in the same integrated circuit. This helps to reduce PCB real estate and costs. The S/UNI-VORTEX supports eight LVDS interfaces.

IEEE P1596.3-1995 allows for two variations of LVDS specifications; General Purpose Link and Reduced Range Link. The significant difference between the two specifications is the allowed ground potential difference (Vgpd). The General Purpose Link specifies the maximum Vgpd at 925mV while the reduced range link specifies the maximum Vgpd at 50mV. In effect, the reduced range link specification is directed towards links on PCBs or other similar environments where the ground potential difference is expected to remain below 50mV.

Figure 10 (below) shows two single-ended signals combined to create a differential pair. The single-ended Voa signal represents *true* and Vob is its *compliment* and the offset (common mode) voltage is 1.2V. The differential signal, Vod, results when the compliment is subtracted from the true signal.

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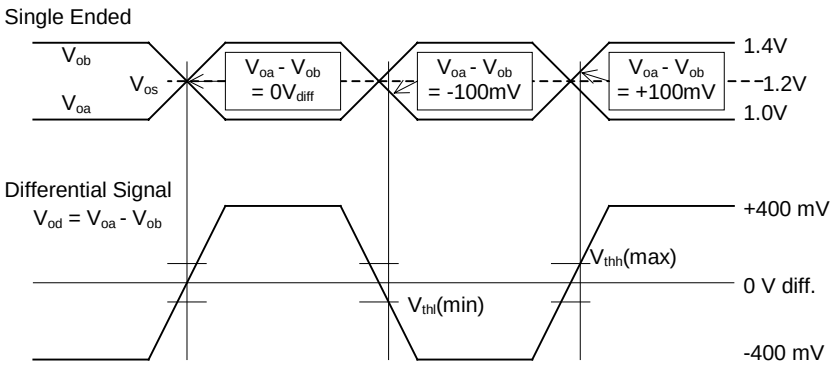
Figure 10. Low Voltage Differential Signal Output levels



The peak-to-peak voltage swing across the LVDS differential pair is up to 800 mV. A single line swings with peak-to-peak amplitude up to 400 mV.

The differential receivers are capable of handling signal swings down to 100mV. A wide common mode range makes them compatible with LVDS signals. External termination resistors must be provided to match the cable impedance.

2.3.2. DSLAM High-Speed LVDS Serial Interface

The S/UNI-DUPLEX and S/UNI-VORTEX provides backplane interconnection through 100 to 200 Mbps serial links that use the LVDS standard. All data going to and coming from the cell processing on the Core Card are concentrated on these high-speed links. The LVDS transmitter/receiver supports UTP-5 cable lengths up to 10 m. Clock is transmitted and the receivers recover a local clock from the incoming data, to avoid clock skew issues. Transmitter outputs are internally terminated current mode drivers. Correct termination at the receiver provides appropriate signal levels.

Two bi-directional LVDS links are provided on the S/UNI-DUPLEX for redundancy. Each link is intended for routing to different Core Cards. Both LVDS transmitters carry identical traffic except for internally generated overhead. Both links are frequency locked to the single input reference clock, although their phase is not guaranteed to match. At the S/UNI-DUPLEX, LVDS receivers clock recovery and cell delineation are always active for both receivers to allow a quick switch to the redundant Core Card with minimal cell loss. The S/UNI-VORTEX LVDS interface recovers clock and data on each link independently. The transmit data on each port is synchronous to the same reference clock. The data edges are not guarantied to have the same phase. The cell delineation phase is different on each transmit and receive ports.

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The internal transmit clock is synthesized from a 12.5 MHz to 25 MHz clock. The resulting data bit rate is eight times the frequency of the REFCLK input. All jitter below 1 MHz on REFCLK is passed unattenuated to the TXD1+/- and TXD2+/- outputs. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference input and a low noise board layout, the intrinsic jitter is typically less than 0.01 UI RMS and 0.10 UI peak-to-peak, when measured using a band pass filter with 12 kHz and 1.3 MHz cutoff frequencies.

The receivers monitor for loss of signal (LOS) on the links. LOS is declared in 2048 bit periods (13.2 µs at 155.52 Mb/s) without a signal transition in the scrambled data. Consequently, a status bit is set, a maskable interrupt is asserted, and the RDI (Remote Defect Indication) codeword is sent repetitively in the BOC bit in the corresponding downstream link. The LOS indication is cleared when a signal transition has occurred in each of the 16 consecutive intervals of 16 bit periods each.

Clock recovery is performed by a digital locked loop (DLL). The implementation is robust against operating condition variations and power supply noise. The receive link is constrained to be within 100 ppm of eight times the REFCLK frequency.

Both the S/UNI-DUPLEX and S/UNI-VORTEX provide LVDS loopback capability to aid in system diagnostics. The metallic loopback routes high-speed serial receive data to the transmitter. Both devices also provide diagnostic loopback, which allows loopback of data on the drop side. The loopbacks can be enabled individually or simultaneously, and each link can be looped back independent of the other.

The DSLAM Reference Design Line and WAN Cards have a hardwired provision for remote reset through the RSTBOB pin on the S/UNI-DUPLEX device. The reset function is one of the pre-programmed patterns. Other functionality is not implemented in this issue of the Reference Design.

NOTE:
The LVDS interface is fully hot swap compatible. The LVDS transmitters and receivers can stay active while other card is hot swap. Writing to corresponding registers on the S/UNI-DUPLEX or S/UNI-VORTEX can disable transmitters. IMPORTANT - Proper register write sequence is required to ensure cell transfer. The sequence is implemented in the VORTEX Chipset driver files vcs_api1.c and dpx.c. The most critical is to make sure the OCAEN bit in register 0x0A in the S/UNI-DUPLEX stays disabled until S/UNI-ATLAS polling is enabled. The OCAEN is set to 1 as the very last write, enabling cell transfer from the S/UNI-DUPLEX at that interface. Software designers are required to observe sequencing in their drivers.

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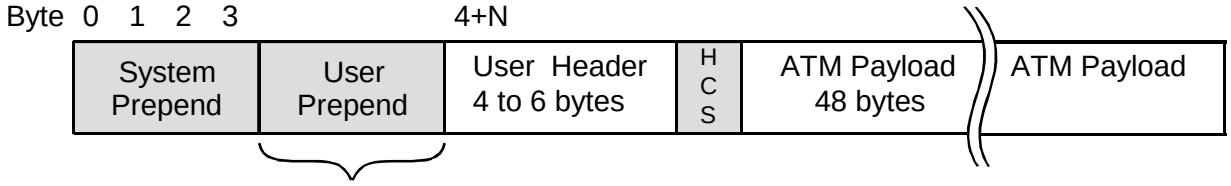
2.3.3. ATM Cell on High-speed Link

The high-speed link supports a proprietary protocol with cells similar to the ATM cells with additional octets carrying interface overhead.

The serial LVDS link carries ATM cells with prepended bytes. Figure 11 shows the cell format.

Figure 11. High-Speed Serial Link Data Structure



The S/UNI-DUPLEX and S/UNI-VORTEX appends the first four bytes and the Header Check Sequence (HCS) byte in LVDS transmit directions. At the receiver, the high-speed cell is stripped off the prepend and the remainder of the bytes in the data structure is transferred transparently. The high-speed transmit bytes are serialized most significant bit first. The bit stream is a simple concatenation of the extended cells. Cell rate decoupling is accomplished through introduction of stuff cells.

The transmitter inserts a correct CRC-8 that protects both the ATM cell header and prepended bytes in the HCS byte. Cells with an HCS in error are counted and then discarded. The receiver also uses the HCS byte for determining cell delineation. Failure to establish cell alignment results in a loss of the cell delineation (LCD) alarm. The entire bit stream is scrambled with a $x^{43} + 1$ self-synchronous scrambler. TABLE 1 summarizes the contents of the system prepended bytes.

TABLE 1. Prepended Fields

Byte	Bits	Mnemonic	Description

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Byte	Bits	Mnemonic	Description
0 1	7:0 7:0	CA[15:8] CA[7:0]	The CA[15:0] bits carry per-PHY flow control information in the upstream direction. To support 32 PHYs, the status for each PHY is sent every other cell; the CASEL indicates which half is represented. If CASEL is logic 0, CA[15:0] corresponds to those PHYs with addresses 0 through 15. If CASEL is logic 1, CA[15:0] corresponds to those PHYs with addresses 16 through 31. In the downstream direction, CA[15:0] communicates congestion of the upstream entity. The encoding is identical to the upstream direction. A logic 0 indicates the far end can accept no more cells for a specific logical channel. A logic 1 indicates the S/UNI-DUPLEX is free to send queued traffic for that logical channel immediately. In the event of an errored header (as detected by an incorrect HCS), the CA bits will be assumed to be all zero. This ensures cells are not transmitted for which there is no buffer space.
2	7	CASEL	The state of the CA select bit determines which half of the PHY devices the CA[15:0] bits correspond to. CASEL toggles with each cell transmitted.
2	6	UPCA	The UPCA bit carries flow control information for the microprocessor control channel. If this bit is one, control channel cells may be transferred. In the event of an errored header, the UPCA bit will be assumed to be zero. This ensures cells are not transmitted for which there is no buffer space.
2	5:0	PHYID	The PHY identifier determines to which PHY a cell is destined in the downstream direction and from which PHY it came in the upstream direction. It also indicates whether the cell is a stuff or control channel cell. The field is encoded as follows: “111111” – Stuff cell provided for cell rate decoupling. The payload carries no useful data and the cell shall be discarded. “111110” – Control channel cell. On the transmit serial link, PHYID equals this value for all cells inserted through the Microprocessor Cell Buffer. All cells received on the serial link with this encoding will be routed to the local microprocessor. “100000” to “111101” – Reserved “000000” to “011111” – Logical channel index for the PHY devices.
3	7	BOC	The Bit Oriented Code (BOC) bit position carries a repeating 16 pattern that encodes one of 63 possible code words used for remote control and status reporting. Five codes are predefined to represent a remote defect, a loopback activate request, a loopback deactivate

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Byte	Bits	Mnemonic	Description
			request, a reset activate request, and a reset deactivate request. The remaining codes are either reserved or user defined. The receiver ensures the pattern is the same for 10 (default) or 5 repetitions before validating a new code word. For more information, see the data sheet section.
3	6	ACTIVE	The link active bit indicates which of the redundant links is currently chosen. The S/UNI-DUPLEX will switch to the link that contains a one in this location for at least three consecutive cells. The local microprocessor can override this selection. If both links present a one in this location, the selection remains unchanged. To confirm which link is active, the transmitted ACTIVE bit will be a one if the associated receive link is selected. In the event of a header in error, the previous ACTIVE value is retained.
3	5:0	TREF[5:0]	The timing reference encodes an 8 kHz signal inband that is independent of the serial bit rate. The TREF[5:0] binary value represents the number of high-speed link bytes after the one in the timing reference is inferred. An all ones value indicates no timing mark is associated with this cell.

2.3.4. Inband Communication Channel Over the High-speed Link

The Inband Communication Channel (ICC) allows building custom communication channel between two DSLAM entities, and in turn, the whole DSLAM system can be in-system reprogrammed and controlled from a single processing center.

The channel allows insertion, identification, and removal of cells at Any-PHY/SCI-PHY interfaces on both sides of the LVDS link. The ICC channel is dedicated entirely to custom massages transmitted across LVDS link between two cards interfacing with S/UNI-VORTEX to S/UNI-DUPLEX, or S/UNI-DUPLEX to S/UNI-DUPLEX.

It is assumed that the microprocessor entities on both sides of the connection are running a reliable communications protocol.

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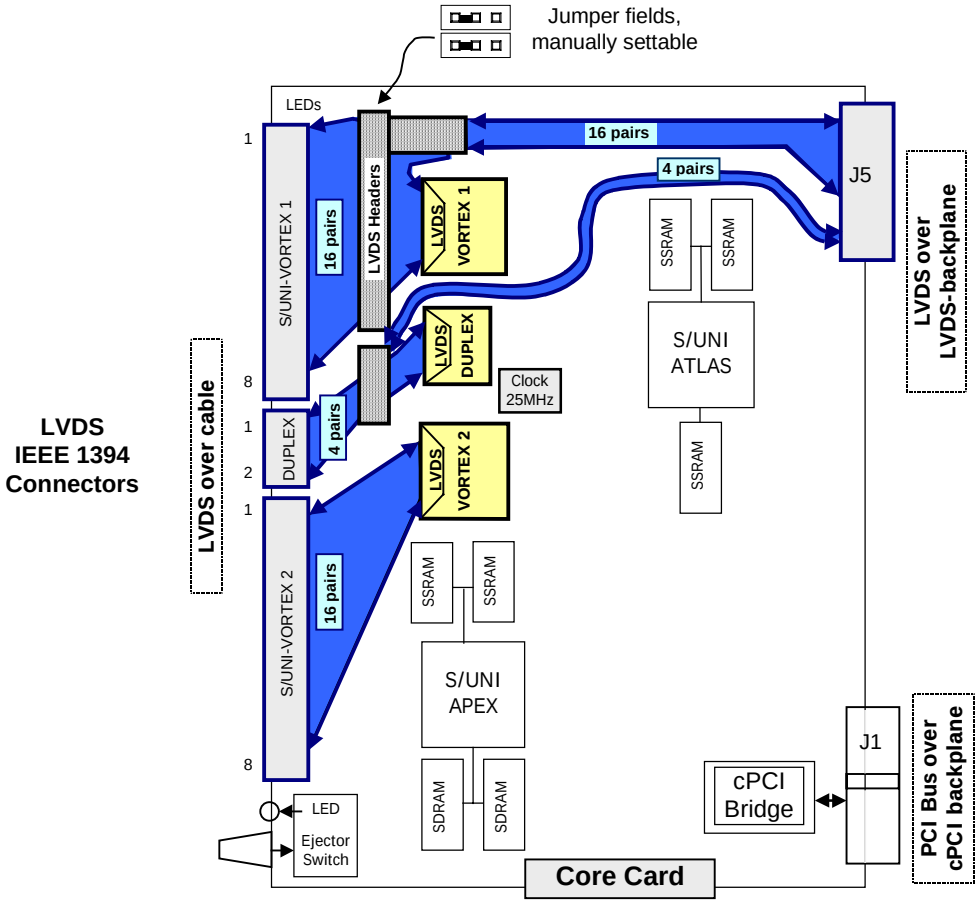
2.3.5. Example of LVDS Layout on Core Card

The LVDS lines on the Core Card are run through jumper fields and allow an interface to the backplane or to the front panel connectors. Figure 12 shows components that support LVDS on the Core Card.

Figure 12. LVDS on Core Card



The LVDS interface on the S/UNI-VORTEX-1 and the S/UNI-DUPLEX can be connected to J5 or to front panel IEEE 1394 connectors. S/UNI-VORTEX-2 provides an interface to the front panel only. The total number of LVDS traces running through J5 to the DSLAM backplane is 40. The LVDS traces to the J5 connector are relatively long, and care is taken to avoid crosstalk to and from digital lines. Front plate connectors are FireWire type (IEEE 1394) designed to handle LVDS up to 400 Mb/s.

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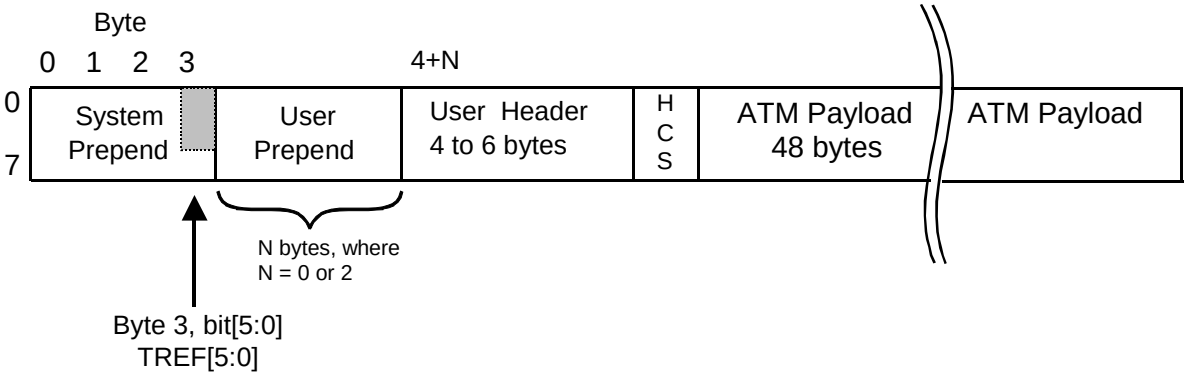
2.4. 8kHz Interface and System Synchronization

The Reference Design uses an 8 kHz clock as a means of system synchronization (stratum clock). The S/UNI-DUPLEX_S/UNI-VORTEX pair transports the 8 kHz time reference over the LVDS connection between different hardware entities in the DSLAM system. The synchronization clock is not restricted to 8 kHz; however, the phase lock loop (PLL)—used to remove jitter and chosen for this design—is optimized for 8 kHz.

The time reference is encoded in the third byte of the prepend that is attached to a modified ATM cell and transmitted over the serial high-speed LVDS connection. Figure 13 shows the LVDS ATM-like cell.

Figure 13. Prepend Fields



The TREF[5:0] binary value represents the number of high-speed LVDS bytes after byte number 3 (shown above) at which the timing reference (can be 8 kHz) is inferred. An all-ones value indicates no timing mark is associated with this cell.

At the receiver site the inherent jitter is at ± one octet. For example, at 200 MHz it is ±40 ns. A phase lock loop (PLL) circuitry is required to filter that jitter. At the receive site the positive edge is timed by a counter starting at byte-3 and counting down value of received TREF[5:0]. When the count-down is at zero (hex 00), the RX8K is toggled high for a short period of time.

The timing channel is not limited to 8 kHz, and any clock frequency lower than the cell rate can be encoded. The encoded timing reference is independent of the serial LVDS link bit rate.

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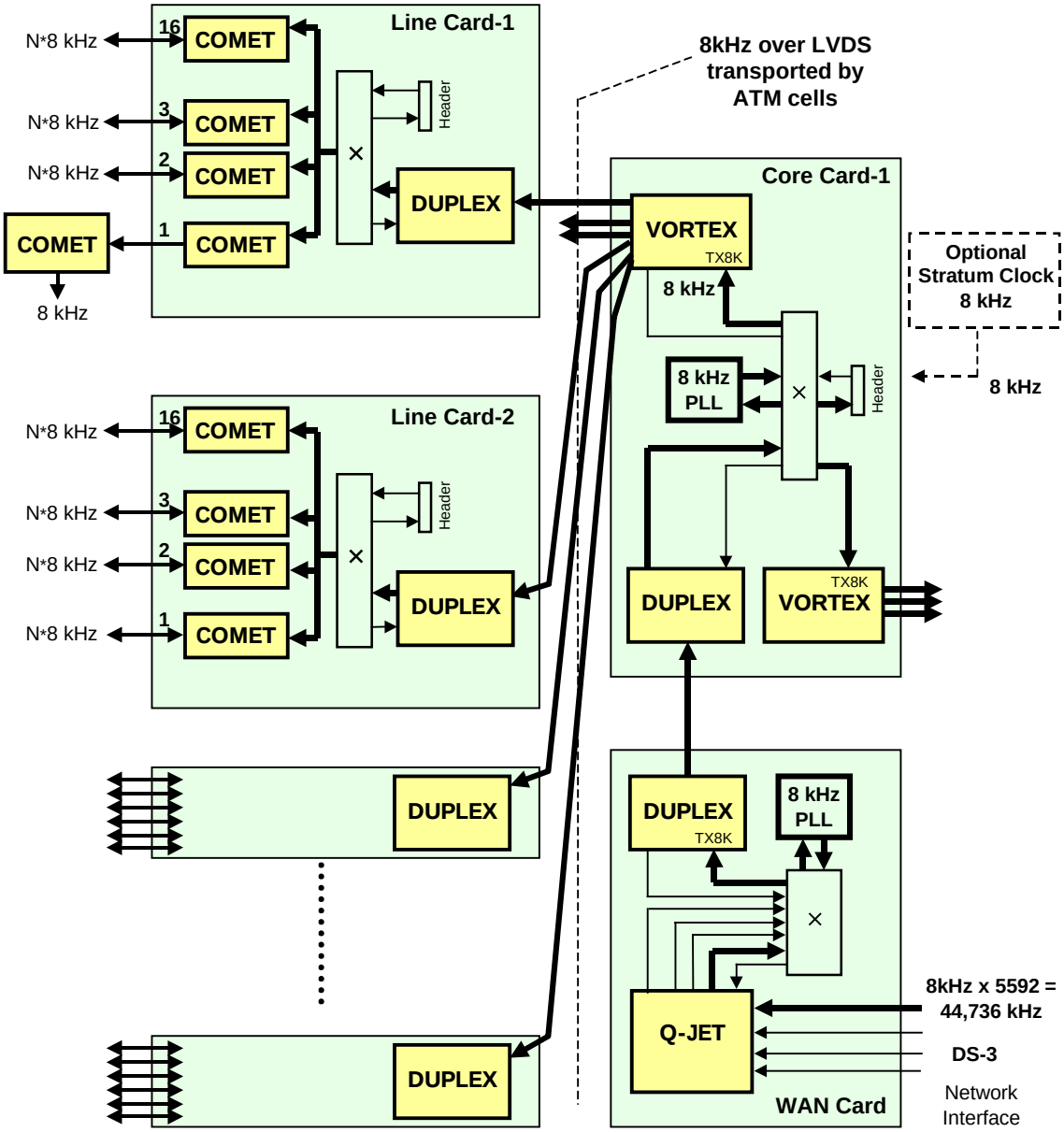
Figure 14 shows an example of the 8 kHz DSLAM network synchronization.

Figure 14. Example of 8kHz Synchronization



A brief description of the circuit is as follows. The DSLAM system can be synchronized to the network interface signal, shown in the lower-right corner of the diagram above, or to the Stratum Clock fed to the Core Card. Let's choose the network interface synchronization path, where the DSLAM entity is synchronized to the DS-3 line that interfaces through the Q-JET. The Q-JET outputs four 8 kHz signals. One of them must go through the 8kHz PLL to get rid

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of the jitter, before it is fed to the S/UNI-DUPLEX pin TX8K. The S/UNI-DUPLEX encodes the 8 kHz clock into the serial LVDS stream (prepend TREF[5:0]) and sends it over the high-speed LVDS connection to the Core Card. The Core Card runs the clock through the PLL and distributes the signal to all S/UNI-VORTEX multiplexers. Each S/UNI-VORTEX again encodes the 8 kHz clock into prepend and sends it over the LVDS interface to all Line Cards. The Line Cards have no 8 kHz PLLs as the COMETs have a built-in dejittering circuit. The received 8 kHz pulses are distributed to all COMETs. Every DS-1/E1 line interface can be frequency synchronized to the network interface signal at the WAN Card.

The Core Card is equipped with a pair of header connectors that allows the 8 kHz interface (headers accessible on the PCB only) to be tested. In the receive direction, the 8 kHz clock can be derived from the network. In the transmit direction, the Core Card can be a source of the synchronization signal by connecting the Stratum 8 kHz Clock and reprogramming the clock flow on the appropriate cards.

The DSLAM shelf can be synchronized to any DS-1/E1 interface by reversing the flow of the 8 kHz clock from the chosen COMET towards the shelf entities. The switching action on the Line Card and WAN Card is controlled by a local microprocessor, which can communicate with the host CPU through the communication channel over the high-speed LVDS link (not implemented in this Reference Design). The Core Card 8 kHz path is controlled through the cPCI bridge.

The 8 kHz switching is executed on each board with a CPLD device, marked “X” on the block diagram.

The received 8 kHz clock on the S/UNI-VORTEX/S/UNI-DUPLEX pin RX8K is a pulse that lasts for 16 clock cycles on the clock at the LVDS connection. If LVDS is at 200 MHz, then the pulse is 16 x 5 ns = 80 ns long, and repeats at 125 us (8 kHz).

The protection switching between two Core Cards performed in our lab showed no adverse effect on the 8 kHz clock phase and frequency synchronization.. Assume that the 8 kHz signal is inserted to the TX8K input on the WAN Card 1 and distributed towards two Core Cards. – see Figure 3 for test circuit. The 8 kHz timing stamp on both high-speed links is encoded within ± one octet. The LVDS links are running at the same synchronized clock speed (e.g. 200 MHz). Cells are send on both LVDS links with the same timing. Both Core Cards decode the time stamp within ± one octet Both cards run the clock through the 8 kHz PLL and filter out that jitter. At this point, clocks on both Core Cards are phase-aligned with the jitter less than ± one octet. Multiple protection switching did not create any noticeable phase jitter. Oscilloscope was not triggered with timing longer

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than 125 us, and that points to not even a single loss of the time stamp. It is possible that limited number of switching actions did not allow to capture timing loss. The clocks are now fed to the S/UNI-VORTEX devices on each Core Card. The time stamp is received on the Line Card 1 from both Core Cards. The stamps on the high-speed links are aligned again within ± one octet. Core Cards protection switching test was performed at PMC-Sierra. A number of protection switching actions did not create any noticeable phase jitter nor detected time stamp loss. The 8 kHz square wave at the Line card is always locked to the source at the WAN Card. If both clocks, one on the WAN-Line Card and other one on the Line Card were observed with an oscilloscope, the clocks were phase locked with minimum jitter, and a visible edge delay due to a signal propagation delay over the DSLAM entity.

Network synchronization and phase-frequency shift can be found in reference documents [5], [10], [11], and [12].

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3. REFERENCE DESIGN CARDS

This section presents a block diagram and a brief description for the Core Card, Line Card, and WAN Card.

3.1. Core Card

The Core Card is described in detail in the Core Card Reference Design document [1].

3.1.1. Block Diagram

The Core Card provides ATM traffic policing, ATM cell traffic management and ATM cell multiplexing. On the downstream side, the Core Card provides an interface through the S/UNI-VORTEX to the Line Cards. On the network side, the Core Card provides an interface through the S/UNI-DUPLEX to a WAN Card. Both interfaces are LVDS with data transfer up to 200 Mb/s.

The DSLAM Reference Design Core Card supports two S/UNI-VORTEX multiplexers, one S/UNI-APEX traffic manager, one S/UNI-ATLAS ATM layer solution device, and one S/UNI-DUPLEX multiplexer.

The LVDS interface to WAN Card and Line Card is accessible from the front panel or from the backplane. A set of headers is used for manual redirection of the interface.

The Core Card has no embedded microprocessor. Program control of the PMC-Sierra devices (VORTEX chipset) is achieved through the PCI bus host processor (CPU card). This is a register read/write and interrupt servicing interface. The cPCI bus does not carry payload data, which makes it easier for the CPU processor to maintain all DSLAM cards through the cPCI bus. However, cells can be entered to the network through the microprocessor interface on each VORTEX chipset device—the preferred gateway through the S/UNI-APEX.

The local bus is run in a multiplexing mode that supports primarily the S/UNI-APEX. Other devices are capable of communicating in that mode as well, with no data burst.

A CPLD is programmed for address and chip select control, and routing an 8 kHz signal.

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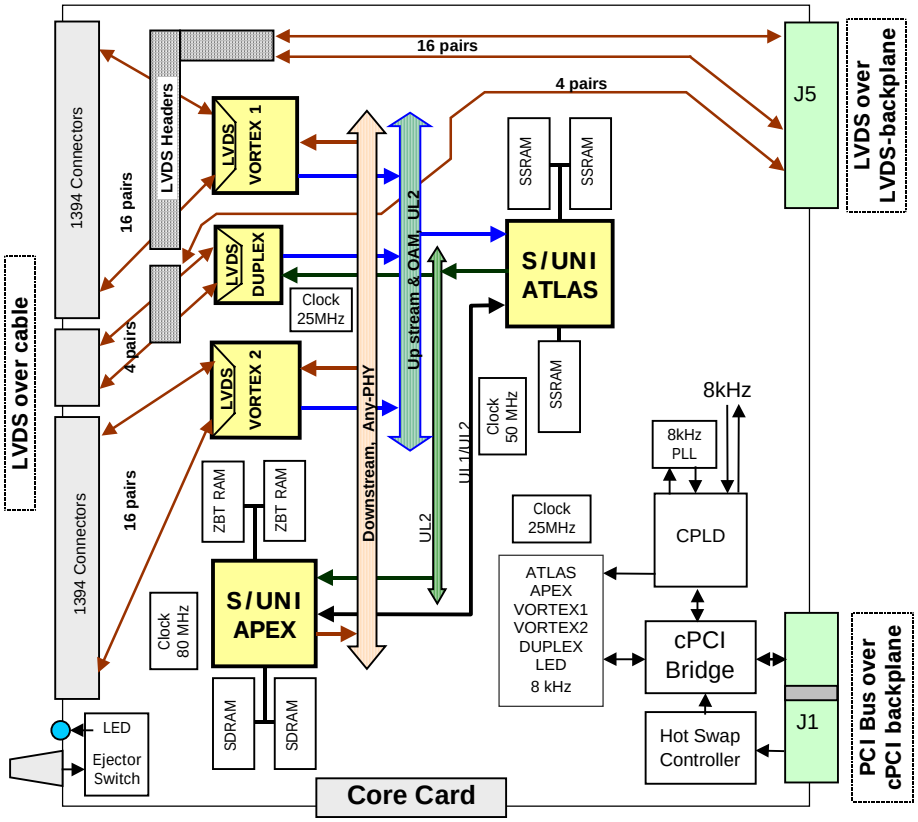
The Core Card is equipped with a micro-switch that is activated by ejector handle action. The host CPU detects the insertion or removal of the card and takes proper action preventing PCI bus corruption.

Figure 15 shows the Core Card block diagram.

Figure 15. Core Card Block Diagram



The Reference Design supports scaled-down DSLAM application; therefore, the size of RAMs supporting the S/UNI-ATLAS may be downsized appropriately. The Core Card is designed to support up to 16 k connections. This requires a total of three 512 KB SSRAM chips associated with the S/UNI-ATLAS. SRAMs operate at 50 MHz.

The S/UNI-APEX RAM size depends on applications and should be calculated according to the S/UNI-APEX data sheet and programmers guide [9]. The Core Card may have assembled oversized RAM due to test purposes, RAM availability and other reasons – check Core Card Reference Design document [1]. Both RAMs operate at 80 MHz.

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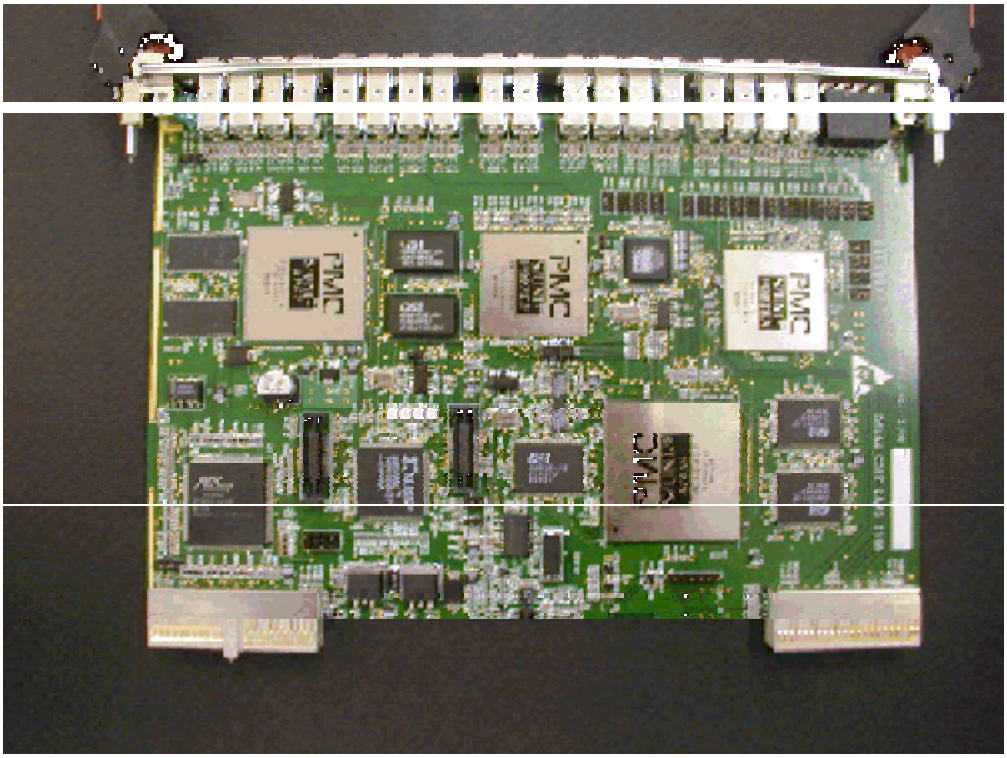
In the downstream direction, the S/UNI-APEX sends data to the S/UNI-VORTEX (and then to the Line Cards) through the Any-PHY interface that supports up to 800 Mbps and allows for 2048 channel addressing (logical PHYs). The data format is an ATM cell with a prepended single address word.

The Core Card picture is shown in Figure 16 below.

Figure 16. Core Card Top View



3.1.2. Core Card Software/Firmware

There is no microprocessor (firmware) dedicated to the VORTEX Chipset control on the card. Power-up and operating functions must be downloaded through the cPCI bridge from the host processor card.

The Core Card has a small serial EPROM (SEEP) for the PCI bridge chip configuration.

A programmable CPLD supports local bus functionality, chip select, interrupts, LED control, and 8 kHz clock routing. The CPLD controls enabling the interrupt line to the PCI bridge.

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The host processor card monitors alarm and interrupt signals from the Core Card through the cPCI bridge.

The Core Card can provide bi-directional communication channel for software control to the Line Cards and WAN Cards. That channel may allow temporary or permanent remote reprogramming of the DSLAM entities, if the appropriate hardware and software resides on the WAN or Line Card.

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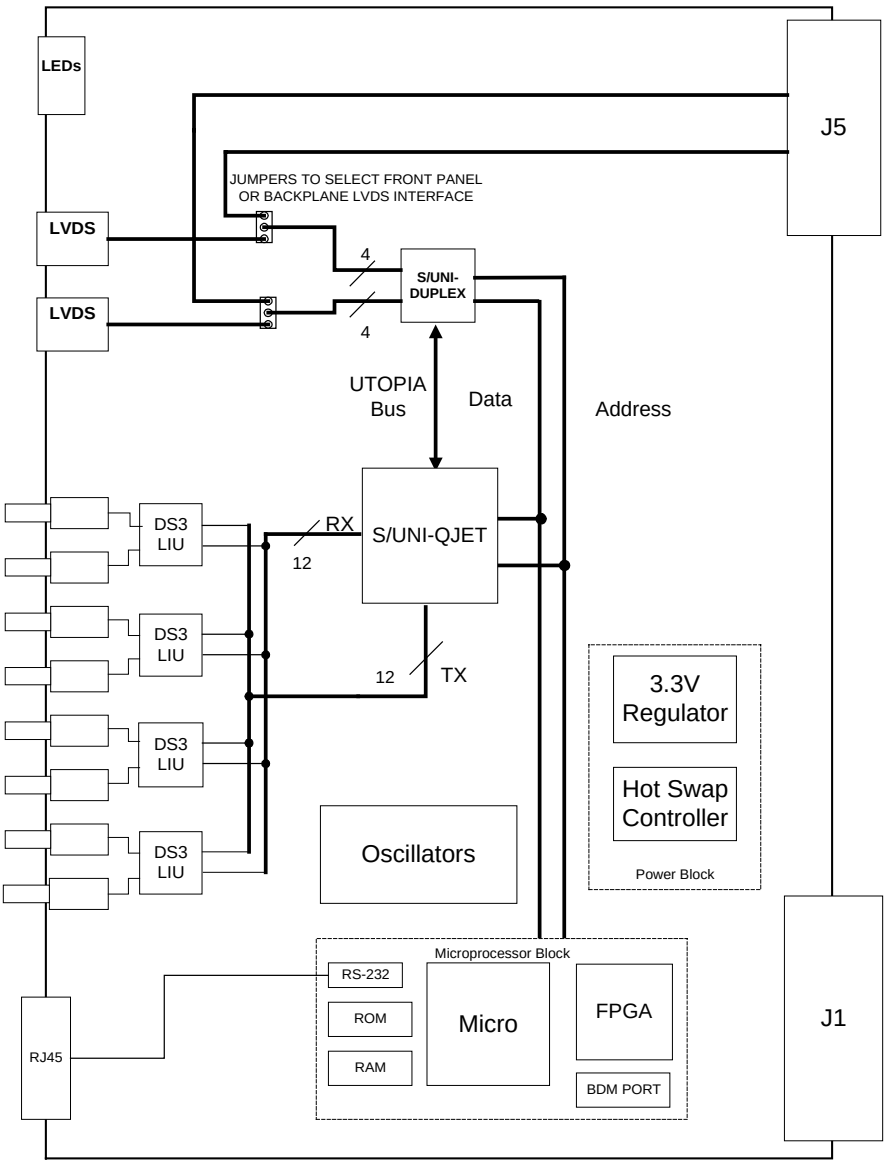
3.2. WAN Card

This section provides a brief introduction to the WAN Card. The WAN Card is described in detail in the WAN Card Reference Design document [3].

3.2.1. Block Diagram

Figure 16 shows the block diagram forthe WAN Card.

Figure 17. WAN Card Block Diagram



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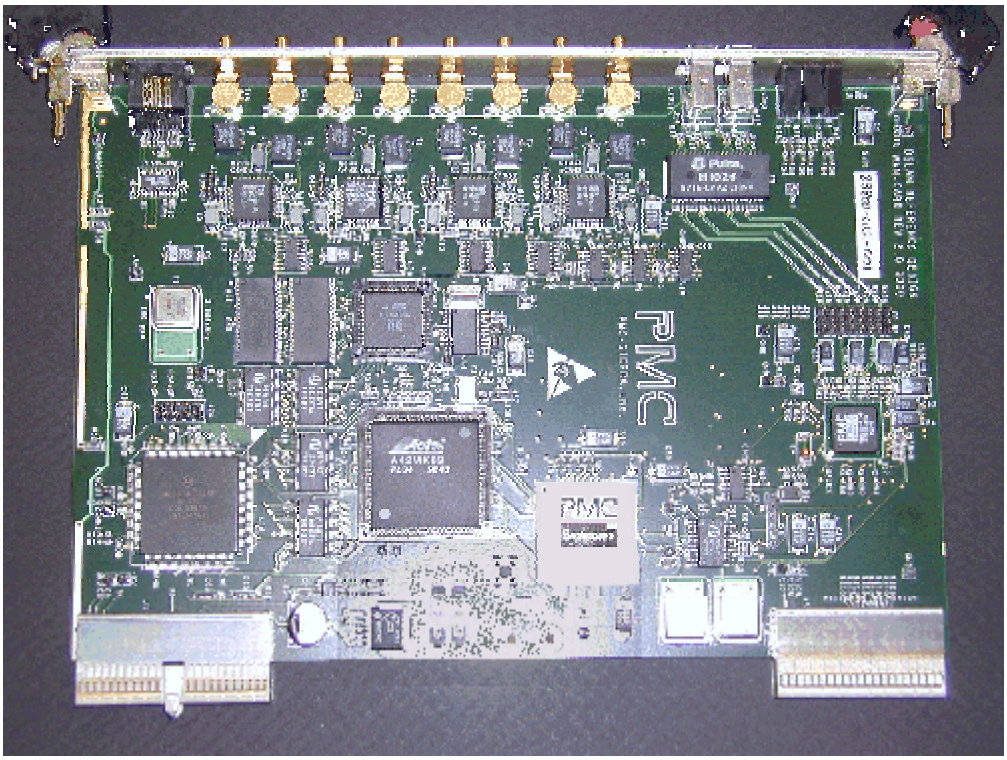
The S/UNI-DUPLEX provides an interface to the LVDS through the front or back connector. The S/UNI-DUPLEX is configured for a UTOPIA L2 bus, and it provides an interface to the S/UNI-QJET. Four DS3 line interfaces are on the network side of the S/UNI-QJET, allowing easy testing and enabling traffic generation. An LIU device is needed for the DS-3 physical interface. Eight SMB connectors allow the DS-3 to communicate over coaxial cable. Front plate also supports the LVDS connectors and the RJ-45 connector for microprocessor serial port.

WAN Card picture is shown in Figure 18 below.

Figure 18. WAN Card Top View



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3.2.2. WAN Card Software/Firmware

The boot-up and the default setup firmware for the VORTEX chipset resides on the WAN Card. Power-up and operating functions are executed by the embedded microprocessor.

The WAN Card is equipped with a push-button RESET switch accessible at the inside of the card, to avoid accidental activation while plugging connectors and other routine card/shelf maintenance. The RESET executes hardware reset to the entire board.

A BDM port on the card, accessible only from inside the shelf, allows the user to develop the software/firmware.

In general, DSLAM entities can be remotely controlled with Inband Communication Channel (ICC) run over high-speed link. Customer needs to implement communications protocol. The ICC communication may allow for remote card reprogramming, and alarm and interrupt servicing. Also, microprocessor re-boot to the card may be communicated through ICC.

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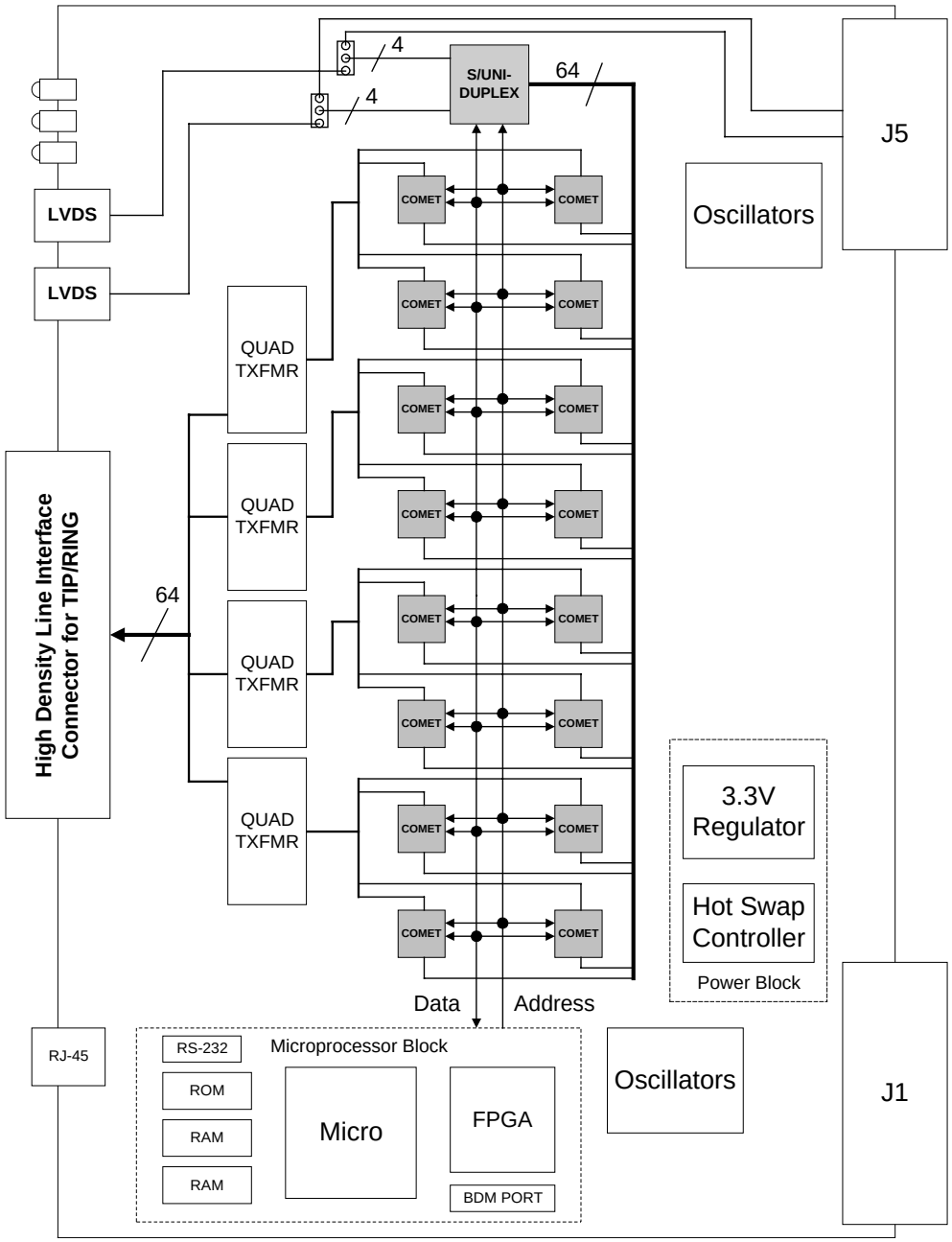
3.3. Line Card

The Line Card is described in detail in the Line Card Reference Design document [2]. Figure 17 shows the Line Card block diagram.

Figure 19. Line Card



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The DSLAM Reference Design supports Line Cards with sixteen COMETs. The Line Card provides sixteen DS-1/E1 interfaces to visualize fan-out of the DSLAM user line interface and to use all sixteen data-and-clock interfaces on the S/UNI-DUPLEX. High-speed link ATM cells are demultiplexed with the S/UNI-DUPLEX and addressed to sixteen COMET devices.

On the system side, the S/UNI-DUPLEX provides two serial LVDS interfaces one to the Operating Core Card and the other one to the Standby Core Card. The LVDS can be run through a backplane dedicated (point-to-point) transmission line, or it can be run through an external cable. Both ports on the S/UNI-DUPLEX are jumper configurable, allowing independent routing to the front connector or to the backplane.

The copper loop side on the COMET interfaces with the DS-1 or E1 physical layer through a front plate high-density connector.

A microprocessor and a hot swap circuit compliment the design. The Line Card has no data interface to the cPCI bus. Power is supplied with J1/P1 connectors. The Line Card has no 8 kHz PLL, as each COMET is equipped with a dejittering circuit.

3.3.1. Line Card Software/Firmware

The boot-up and the default setup firmware for the S/UNI-DUPLEX and COMETs resides on the Line Card. Power-up and operating functions are executed by the embedded microprocessor.

The Line Card is equipped with a push-button RESET switch that is accessed from inside the card, to avoid accidental activation while plugging connectors and during other routine card/shelf maintenance. The RESET executes hardware reset to the entire board.

The ICC communication to the Line Card allows for reprogramming, however, that functionality may or may not be implemented with released firmware (see the WAN Card documentation for the latest in-system programmability).

A BDM port on the card, accessible only from inside the shelf, allows the user to develop the software/firmware.

In general, DSLAM entities can be remotely controlled with Inband Communication Channel (ICC) run over high-speed link. Customer needs to implement communications protocol. The ICC communication may allow for remote card reprogramming, and alarm and interrupt servicing. Also, microprocessor re-boot to the card may be communicated through ICC.

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3.4. CPU Card

The CPU card is a stand-alone PC with the following specification:

- Pentium P55C (MMX) 233 MHz
- 512 kB L2 cache RAM
- a maximum of 384 MB RAM
- 3.2MB HD and a floppy DD installed as a sub-assembly (mezzanine) on top of the CPU card
- VGA, keyboard, mouse connectors
- Serial and parallel ports
- 10/100 Mb Ethernet
- cPCI bridge interface supporting 32 and 64 bit architecture
- OS compatibility with MS-DOS, Windows 98, Windows NT and VxWorks
- two-slot wide card
- multiple vendors.

The CPU card is always placed into slot-1 on the cPCI bacplane, marked with a triangle and “1” inside. The card width is equivalent to two cPCI slots, and the card extends into slot-2. The cPCI backplane is the “left-side system slot” type.

The operating system that runs the DSLAM Reference Design shelf is VxWorks.

PMC-Sierra provides software drivers for these individual devices: S/UNI-DUPLEX, S/UNI-VORTEX, S/UNI-APEX, and S/UNI-ATLAS; and a meta-driver for the VORTEX chipset (board driver). The drivers are configured to run on the VxWorks operating system.

3.5. LEDs on the Front Panel

The DSLAM cards are equipped with a set of LEDs for status indication mounted visible at the front plate. Core Card has additional LEDs inside the card.

The front panel LEDs on all cards are described in section 4 in this document.

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3.6. Card Hot-Swap

The cPCI shelf operation requires all DSLAM cards to have a mechanism for hot-swap ability. The hot swap addresses three major issues:

- Power rail issues – supply voltage glitches during card insertion/removal. The voltage glitch on a power rail may reset other cards (or create data corruption) and/or corrupt the cPCI bus data.
- CPCI interface issues – the Core Card is equipped with a hot swap bridge and a pre-biasing circuit, allowing live insertion on the cPCI bus. The WAN Card and Line Card has no cPCI bus interface.
- Software readiness issues – the Core Card has working ENUM# line, necessary for software hot swap. The ENUM# line, activated by a microswitch build-in into ejector handle, allows notification to the host processor card about Core Card removal or insertion. A blue led, required by cPCI hot swap standard, is ready to visualize software hot swap action.

Hot swap is advantageous in servicing DSLAM system. It allows removal of a malfunctioning card with minimal interruption to the system.

NOTE:
Hot swap software is not implemented in the VORTEX Chipset Driver. The hardware allows easy implementation of that functionality, if required by the customer.

3.6.1. Power Rail Hot Swap Control

The DSLAM cards are equipped with serial MOSFET transistors that control an inrush current and voltage spikes when performing a live insertion and removal of the card. The MOSFET transistors are gradually turned on, ramping the Vcc from 0 V to 5 V in about 50 ms. It allows “glitch-free” power rails during card maintenance. The Line Card and WAN Card control +5 V feeding rail. The Core Card controls +5 V and +3.3 V with two separate, very low Rdson MOSFET transistors.

The WAN and Line Cards use hot swap controller LTC1422. The Core Card board Rev. 3 uses LTC1645 – a dual line current sensing device. Both devices provide gate voltage ramp (for MOSFET transistors), and also current sensing for short circuit protection. The LTC1422 has a RESET pin for under-voltage detection. The Core Card board Rev. 3 uses LTC1326 for the RESET control.

Staged pins on the P1 connector that is mounted on the cPCI backplane detect card insertion and removal. The longest pins provide early voltage activating hot

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swap controller only. The medium length pins mate high current ground and power rails (with no current). The shortest pin, which mates the last or disconnects the first, controls on/off action of the serial MOSFET transistors. The turn off action is abrupt.

3.6.2. PCI Interface

The Core Card provides the means for data corruption free insertion onto the cPCI bus.

The cPCI data lines are pre-polarized with a 1.0 V bias voltage and 15 kohm resistors when the card is inserted (as required by “Hot Swap Recommendations”). The bias voltage is derived from the “early voltage” supplied by the longest pins on the P1 connector. The value of the “1.0 V” is a compromise minimizing a voltage glitch on active data lines, when the just-connected pin is charged to logic low or high. The data lines are held by PCI9054 in high-Z, until the local RESET line de-asserts. The host CPU is notified by the ENUM# line about shelf hardware/software change (some host cards may not be able to detect ENUM# line change).

On removal of the Core Card, the cPCI bridge is notified by the micro-switch in the ejector, and in turn, the bridge notifies the CPU card. The CPU shuts down communication and turns on the blue LED signaling to the operator readiness for card removal. For more information about the hot swap circuit, see the Core Card Reference Design.

The WAN Card and Line Card provide a means of hot swap on the power rails only. The cards do not provide an interface to the PCI data bus. The system can detect card insertion or removal indirectly from the Core Card through the high-speed link status or through the communication channel over the high-speed link.

3.6.3. LVDS Interface

The LVDS interface is generally hot-swap compatible, in a sense that connecting and disconnecting LVDS cables should not cause uncontrolled data corruption on the system side. The S/UNI-DUPLEX and S/UNI-VORTEX are able to discard invalid cells at the high-speed receiver. Cell corruption is expected, triggering the LCD or LOS alarm with a traffic cease in the “received data” direction.

The main issue, with in-system connecting and disconnecting LVDS cables, is possible damage due to an excessive ground loop voltage when the service crew maintains cables or cards. Another related issue is data corruption or electrical

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damage on an established connection due to excessive common mode noise, most likely from 60 Hz noise and the harmonics of AC power.

Ground differences between racks can easily reach single volts, and during a lightning strike it can go to tens of volts (or higher). That voltage, at best, will corrupt data, and may permanently damage the LVDS interface. Grounding problems can be resolved by using high-speed transformers. Lower cost solution is to use serial capacitors, which may help reject 60Hz (and harmonics) noise. Serial capacitors do not reject high frequency common mode voltage. The LVDS data is scrambled to avoid long runs of ones or zeros that can create baseline wander.

The Reference Design cards use transformers coupling on LVDS inputs on the WAN Card and Line Card (optionally, PCB allows serial capacitors). The Core Card uses serial capacitors due to real estate limitations. This allows to minimize 60 Hz ground loops on all cards. Capacitive coupling should be sufficient for the limited length of the LVDS interface in a shelf-to-shelf or rack-to-rack environment. System and facility design and appropriate grounding should prevent excessive common mode voltage between DSLAM entities.

WARNING: Transformers, together with too small value of the serial capacitors on another card, may have low frequency roll-off at a higher frequency, and may cause baseline wander and possible bit errors.

3.7. Power Supply Requirement

The WAN Card and Line Card are designed to operate with +5 V supply only. The +5 V is fed through the J1 connector. The +3.3 V, required to power some circuitry, is derived from +5 V with a linear regulator on each card.

Core Card requires +5V and 3.3V supply. Supply current on +3.3V is in a range of 4 A, and it is not feasible to regulate down from +5V with an on-board linear regulator. The +5 V rail supplies 8 kHz PLL and a +2.5 V linear regulator, which is needed for the S/UNI-APEX core. If 3.3 V PLL is available (or not needed) and +3.3 V to +2.5 V linear regulator is available, then designers can easily eliminate the +5 V rail (from J1/P1 cPCI backplane) and supply Core Card with +3.3 V only.

DSLAM cards shall operate when powered with a standard switching power supply found throughout the PC industry. DSLAM cards or the DSLAM development shelf do not support 48V Telco type of supply rails.

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The current was measured on the DSLAM development shelf populated with cards as shown in Figure 5 earlier. Total current for host processor card, two Core Cards, two WAN Cards and two Line Cards is:

- +5 V rail ~ 12.0 A
- +3.3 V rail ~ 6.5 A
- +12 V ~ 0.2 A
- -12 V 0 A

With moderate traffic current on +5 V rail goes to 13 A and on +3.3 V to 7.2 A.

The current per DSLAM Card is measured at about:

- Line Card +5 V rail ~ 1.8 A
- WAN Card +5 V rail ~ 1.7 A
- Core Card +5 V rail ~ 0.8 A
  +3.3 V rail ~ 4.1 A

Total power dissipation on the Core Card board Rev. 3 is estimated at P = (5.25 V * 0.8 A) + (3.6 V * 4.1 A) = 19 W. The Core Card requires forced airflow cooling system in enclosed shelves. While the Core Card board Rev. 3 was tested in an open development shelf, no excessive overheating was observed.

Supply current may vary at extreme voltage and temperature corners.

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4. FRONT PANEL LEDS

DSLAM cards are equipped with rows of LEDs for status indication visible on the front panel. The front panel LEDs for all cards are shown in Figure 20 (in following sections).

4.1. Core Card LEDs

Some LED functionality may not be implemented in the current software driver. The following description is the preferred functionality of the LED display.

The basic set of four LEDs provides visual information about power lines and basic condition of microprocessor interface to all components. The basic LEDs are:

- +5 V, green – indicates presence of +5 V
- +3.3 V, green – indicates presence of +3.3 V
- uP, red – may not be implemented in the Chipset Driver. The preferred functionality: ON indicates trouble at uP (power-up boot).
- Status, yellow – may not be implemented in Chipset Driver. The preferred functionality: flashing indicates an operating Core Card, steady indicates a hot stand-by Core Card, turned off for a malfunctioning Core Card. The LED flashes two times per second.

The preferred functionality for additional red LEDs may not be implemented in the metadriver. The LEDs are intended to indicate loss of signal (LOS) and loss of cell delineation (LCD) on the S/UNI-DUPLEX (from WAN Card) interface. Possible alarms are described as:

- LOS1, red – loss of signal at S/UNI-DUPLEX LVDS RXD1 Port[1]
- LCD1, red – loss of cell delineation at S/UNI-DUPLEX LVDS RXD1 Port[1]
- LOS2, red – loss of signal at S/UNI-DUPLEX LVDS RXD2 Port[2]
- LCD2, red – loss of cell delineation at LVDS RXD2 S/UNI-DUPLEX Port[2]

The preferred functionality for the LEDs in the next two rows shows an LVDS status on both the S/UNI-VORTEX-1 and S/UNI-VORTEX-2.

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4.2. Line Card LEDs

Some LED functionality may not be implemented in the current card firmware. The following description is the preferred functionality of the LED display.

The basic set of four LEDs provides visual information about power lines and basic condition of microprocessor interface to all components. The basic LEDS are:

- +5 V, green – indicates presence of +5 V
- +3.3 V, green – indicates presence of +3.3 V
- uP, red – ON indicates trouble at uP (power-up boot) or RESET
- System, yellow – indicates healthy uP interface to all components; (for information on other functionality, see the Card Reference Design).

Additional red LEDs, that indicate loss of signal (LOS) and loss of cell delineation (LCD) on the S/UNI-DUPLEX for for the Core Card to Line Card interface, are described as:

- LOS1, red – loss of signal at S/UNI-DUPLEX LVDS RXD1 Port[1]
- LCD1, red – loss of cell delineation at S/UNI-DUPLEX LVDS RXD1 Port[1]
- LOS2, red – loss of signal at S/UNI-DUPLEX LVDS RXD2 Port[2]
- LCD2, red – loss of cell delineation at LVDS RXD2 S/UNI-DUPLEX Port[2]

LEDs indicating loss of signal (LOS) and loss of frame on COMETs are grouped by four. That decreases the number of LEDs and allows to visualize status of COMET interfaces. LEDs are described as:

- C 1-4, red – loss of signal or frame at COMET 1 to 4
- C 5-8, red – loss of signal or frame at COMET 5 to 8
- C 9-12, red – loss of signal or frame at COMET 9 to 12
- C 13-16, red – loss of signal or frame at COMET 13 to 16

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4.3. WAN Card LEDs

Some LED functionality may not be implemented in the current card firmware. The following description is the preferred functionality of the LED display.

The basic set of four LEDs provides visual information about power lines and basic condition of microprocessor interface to all components. The basic LEDS are:

- +5 V, green – indicates presence of +5 V
- +3.3 V, green – indicates presence of +3.3 V
- uP, red – ON indicates trouble at uP (power-up boot)
- System, yellow – indicates healthy uP interface to all components; LED flashes twice per second (for information on other functionality, see the user software guide).

Additional red LEDs, indicating loss of signal (LOS) and loss of cell delineation (LCD) on the S/UNI-DUPLEX for the Core Card to the WAN Card interface, are described as:

- LOS1, red – loss of signal at S/UNI-DUPLEX LVDS RXD1 Port[1]
- LCD1, red – loss of cell delineation at S/UNI-DUPLEX LVDS RXD1 Port[1]
- LOS2, red – loss of signal at S/UNI-DUPLEX LVDS RXD2 Port[2]
- LCD2, red – loss of cell delineation at LVDS RXD2 S/UNI-DUPLEX Port[2]

LEDs indicating loss of signal (LOS) and loss of frame on Q-JETs are described as:

- QLOS 1, red – loss of signal or frame at Q-JET line 1
- QLOS 2, red – loss of signal or frame at Q-JET line 2
- QLOS 3, red – loss of signal or frame at Q-JET line 3
- QLOS 4, red – loss of signal or frame at Q-JET line 4

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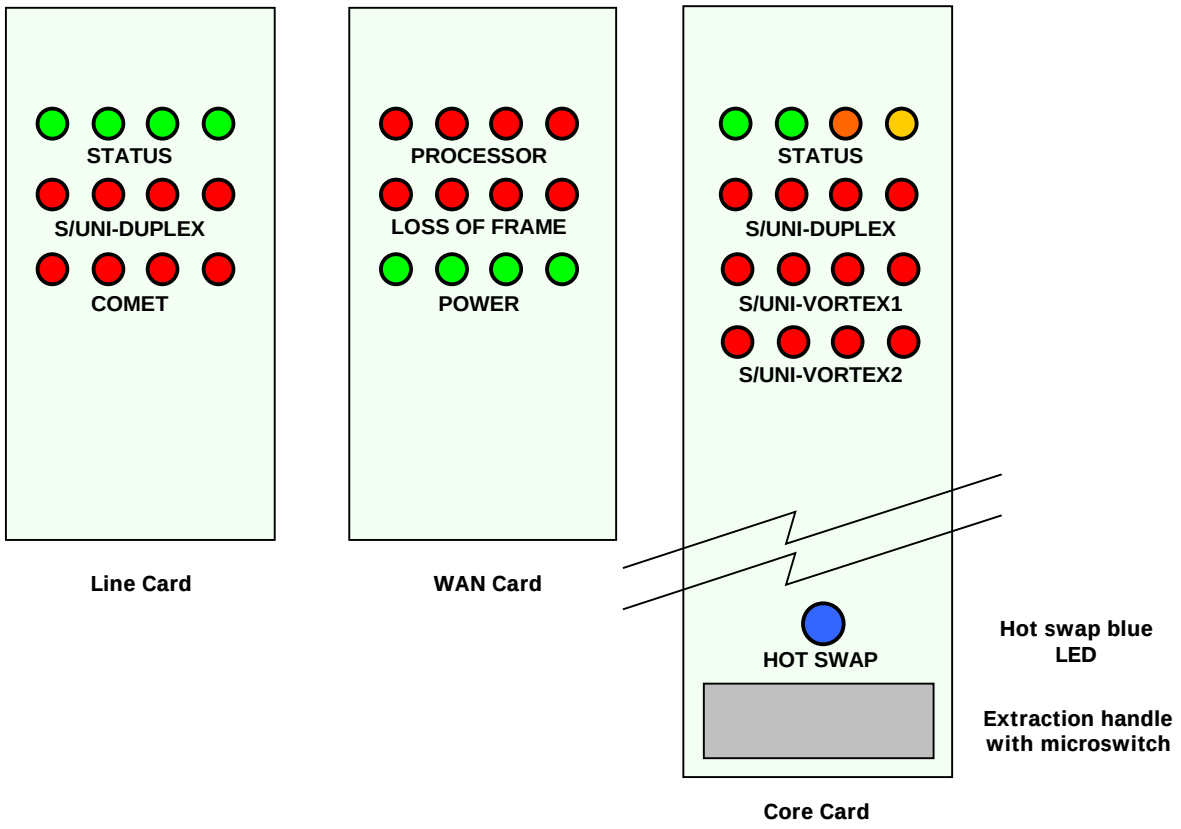
4.4. Example of the LED Placement

Figure 20 shows an example of LED placement on the front plate.

Figure 20. Example of LEDs Placement



The LEDs can be placed as close as 2.54 x 4.7 mm (0.1” x 0.185”). The part type shown in the example are LUMEX 4xTower LED:

- SSF-LXH5147YIGGD (yellow-red-green-green)
- SSF-LXH5147IIIID (red-red-red-red).

Each card may have additional LEDs placed on the printed circuit board, which are not visible at the front plate. Those LEDs can be used for troubleshooting and card/system indicators.

The presence of the supply voltages turns on two green LEDs. However, those LEDs should not be used as an indicator for accurate voltage level.

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The red alarm LEDs are controlled by a microprocessor or a cPCI host processor by writing to dedicated latches. Reading appropriate registers on each silicone device derives alarm conditions.

NOTE: The software LED control functionality is not implemented in the VORTEX Chipset Driver or applications test routines.

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5. DSLAM SHELF BACKPLANE

The DSLAM Reference Design document provides a detailed description of the DSLAM backplane, including:

- CompactPCI (cPCI) backplane overview
- Specification for LVDS-backplane
- Connector placement
- Pinout on each connector

5.1. Introduction

The CompactPCI standard is electrically a superset of the desktop PCI with a different physical connectorization, and minor signal line adjustments. The CompactPCI uses the Eurocard form factor. The PCI Industrial Computer Manufacturers Group (PICMG) is developing recommended practices for cPCI backplanes, for example, pin definition for a basic 3U high backplane, a recommendation for the 6U board pinout, bus definitions for VME-64, and telephony buses like SCSA and HMVIP.

The basic cPCI backplane supports eight card slots; with a single slot dedicated to the system host card. The cPCI connectors, with commercially available PCI-PCI bridge chips, can also be used to extend the CompactPCI bus in 8-slot increments. A CompactPCI system with 16, 24 or even 32 slots can be fabricated. This Reference Design uses an 8-slot, 3U high cPCI backplane.

The 3U cPCI processor boards use 220 pins for power, ground, and all 32- and 64-bit PCI signals. The connector consists of two halves. The lower half (110 pins) is called P1, and the upper half (also 110 pins) is called P2 (connectors on cPCI cards are called J1 and J2). Twenty pins (out of 220) are reserved for future use. The 6U boards can have up to three additional connectors (P3, P4 and P5) with a total of 315 pins. All connectors are 2 mm style.

The connectors can also be used for the rear panel I/O in a manner similar to VME. This approach, popular in the telecommunications industry, brings I/O wiring from the rear of the chassis. Eliminating front panel wiring can reduce the time required to replace a module in critical applications. The IEEE 1101.11 draft standard for rear panel I/O provides a standard method for doing this and works well with CompactPCI.

If the cPCI bus is run on the P1 and P2 connectors, then those connectors are not the rear panel I/O type. In this case, the power rails can be provided to the

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I/O card through the upper connectors. An example of selective assembly is shown in APPENDIX-B, with P3, P4, and P5 assembled as the rear panel I/O connectors.

5.2. Reference Design Backplane

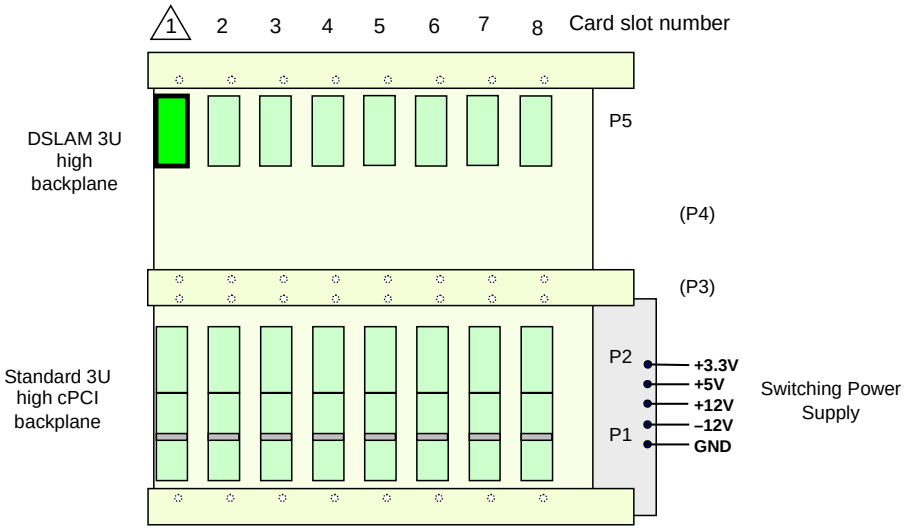
The DSLAM shelf backplane is a part of this DSLAM Reference Design. The DSLAM backplane consists of two printed circuit boards. The first one is a standard, off-the-shelf 3U cPCI backplane, used for the PCI bus interface and power supply to DSLAM cards. The second one is a custom backplane used to transport LVDS over it.

The DSLAM backplane is based on the CompactPCI (cPCI) shelf form that uses 2 mm grid connectors.

5.2.1. Example DSLAM Shelf Backplane

Figure 18 shows an example of a DSLAM development shelf backplane, consisting of two backplane boards.

Figure 21. Example DSLAM Backplane



The lower printed circuit board (PCB) supports cPCI bus with P1 and P2 assembled. That board is purchased on the market. The upper PCB is custom made and supports LVDS point-to-point lines. Mechanical construction of the dual backplane prevents standard cPCI P3 connector use due to split boards and a support bar across middle of the backplane. Connector P4 is not needed as

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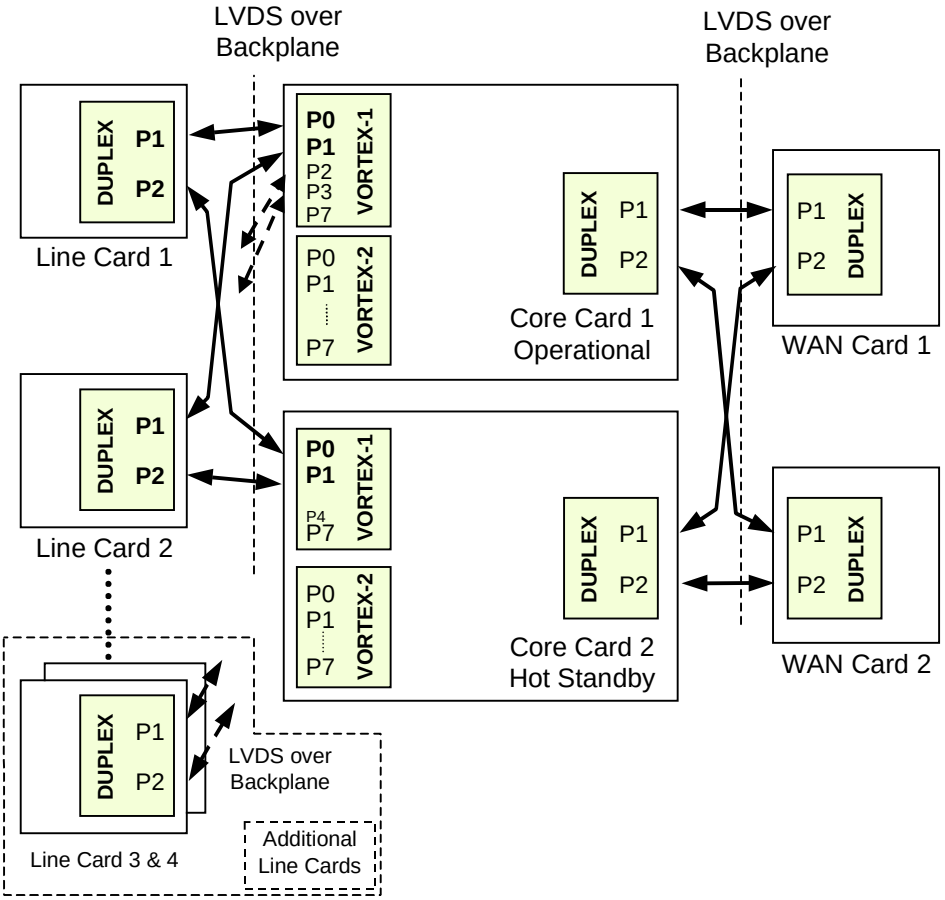
well. Slot counting on the cPCI backplane is from 1 to 8. Slot counting in VORTEX Chipset Driver is from 0 to 7.

5.2.2. LVDS–Backplane

Figure 19 shows the LVDS-backplane, which supports basic DSLAM configuration.

Figure 22. LVDS-backplane Basic Configuration



The main LVDS-backplane interface to Line Cards is done through ports P[0] and P[1] on S/UNI-VORTEX-1 on both Core cCards. Additional LVDS connections are wired to ports P[2] and P[3] (shown as dashed arrows in the diagram for picture clarity). Those connections support the DSLAM shelf with four Line Cards, if WAN Cards are not present.

The LVDS connections between the Core Cards and the WAN Cards are organized to ease protection switching between Core Cards. The DUPLEX on the Core Card 1 provides an interface to the P[1] ports on both WAN Cards,

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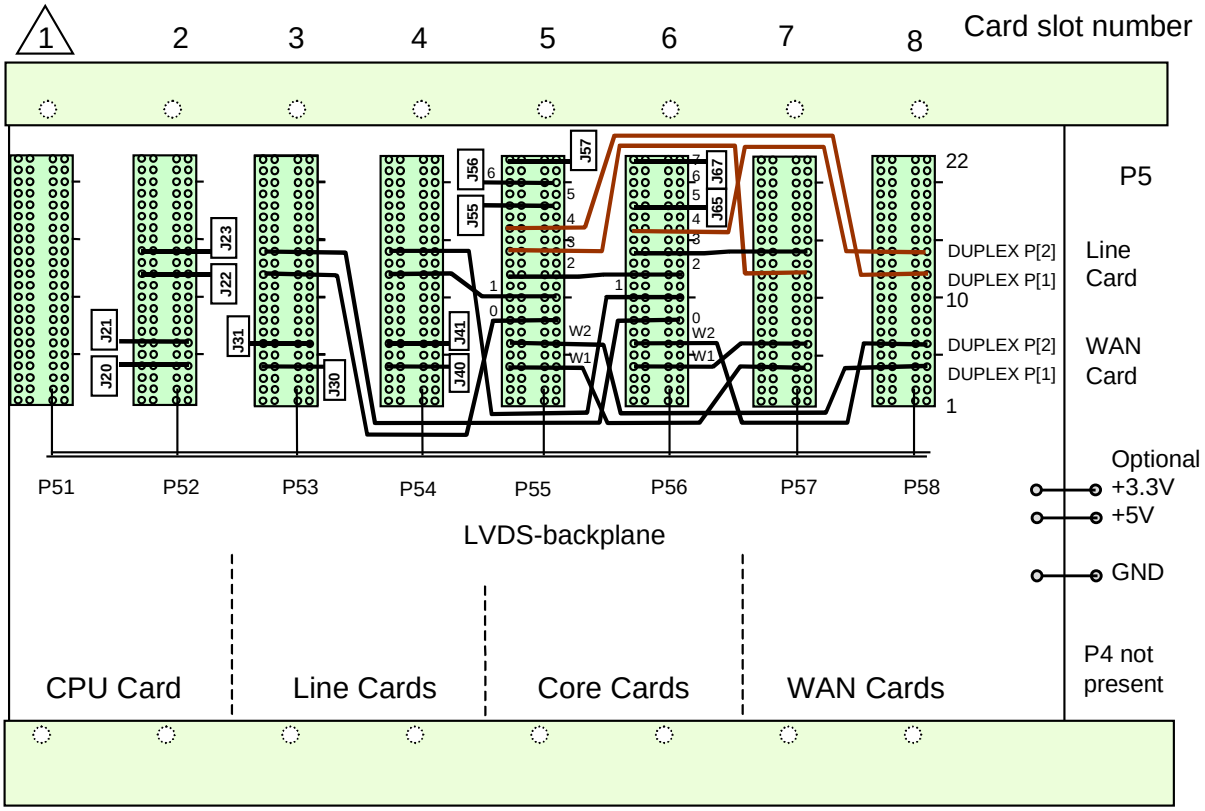
allowing an identical software setup on both Core Cards. If protection switching prefers network connections (broken network to one of two WAN Cards), then the LVDS interface between the Core Cards and WAN Cards may be organized in a different order. Those connections are hardwired on the printed circuit board backplane. All backplane LVDS configurations are permanent, and if other configuration is required, then external LVDS cables at the front panel can modify connections.

The LVDS-backplane requires the P5 row of connectors only. The P4s are not used. Figure 20 shows the LVDS-backplane block diagram.

Figure 23. LVDS-Backplane



Slot assignment to each of the DSLAM cards is the preferred one, and it can be changed within some limits. The P5x connector designation is derived from the cPCI standard, where the connector at the fifth row is called P5.The second digit points to card slot.

The LVDS interface is focussed on connectors P55 and P56. The P55 connector supports the operating Core Card 1. The P56 connector supports the standby

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Core Card 2. Each connector supports up to ten LVDS interfaces. The lower two, marked as W1 and W2, are dedicated to WAN Cards, placed at slots 7 and 8. The middle LVDS's on S/UNI-VORTEX-1, from P[0] to P[4] are wired to P53, P54, P56, P57, and P58. Connector P52 is usually obstructed with host CPU and has no LVDS lines running to P55/P56. The P52 connector has optional headers (J20, J21, J22 and J23) at pins where the Line Card or WAN Card have S/UNI-DUPLEX ports wired. Slots 1 through 8 use standard 22-row cPCI connectors with a DSLAM-specific pin configuration.

The CPU card is supported on the LVDS-backplane at slot 1 with P51 connector. This connector is used as a rear panel I/O interface to peripheral devices.

As a primary configuration, the LVDS-backplane supports two WAN Cards, two Line Cards, and two Core Cards. Core Cards must be associated with a host CPU card on the same shelf. The shelf is not limited to the above configuration and may contain, for example, up to eight Line Cards.

The LVDS interface on the backplane is designed to support the following configuration:

- slot 5 – Core Card 1, and optionally, Line Card or WAN Card
- slot 6 – Core Card 2, and optionally, Line Card or WAN Card
- slot 3 and 4 – primary use for Line Cards and, optionally, WAN Card
- slot 7 and 8 – primary use for WAN Card and, optionally, Line Card
- slot 1 and 2 – host CPU; if not present, then Line Card or WAN Card.

The optionally placed card will not have the proper LVDS interface over the LVDS-backplane and must use the front panel FireWire connectors. The P51 connector is dedicated to the host card rear panel I/O peripheral interface and is assembled on the LVDS-backplane with the extended connector. This connector may be optional depending on the host processor card.

Connectors P55 and P56 support multiple LVDS interfaces; therefore, it is not recommended to support rear panel I/O extension. For a pinout diagram of all the connectors, see section 6 in this document.

If a host CPU is not present on the shelf, then all eight slots can be populated with Line Cards (LC) or WAN Cards (WC).

5.3. DSLAM Cards vs. LVDS-Backplane

The Core Card, Line Card and WAN Card must not have conflicting pinout with the P1x mounted on the cPCI backplane and the P5x mounted on the LVDS-

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backplane. The mating connectors on the DSLAM cards are J1 and J5 respectively. The J1 is defined in CompactPCI specification [13]. The J5 connector must be compatible for each DSLAM card with the pinouts defined in section 7.

The Core Card complies with pinouts for P55 and P56 (at slots 5 and 6).

The Line Card pinout on J5 is primarily compatible with P53 and P54 on the LVDS-backplane. The Line Card can be placed on any slot without causing a short circuit or damage to the card itself or to the system.

The WAN Card pinout on J5 is primarily compatible with P57 and P58. The WAN Card can be placed on any slot without causing a short circuit or damage to the card itself or to the system.

DSLAM cards are supplied with +5 V and/or +3.3 V through the P1/J1 connectors.

5.4. Example of a Card Interface to LVDS-Backplane

Figure 21 shows a block diagram, with an example of DSLAM Cards interfacing with LVDS-backplane. The diagram shows the Line Card at slot 3 and the Core Card at slot-5 or at slot-6.

NOTE:
Port names (numbers) on the S/UNI-VORTEX and S/UNI-DUPLEX follow their corresponding data sheets. S/UNI-VORTEX ports are named as Port[7:0], and S/UNI-DUPLEX ports are named Port[2:1]. Port names may also be abbreviated to P[1], P[2], etc.

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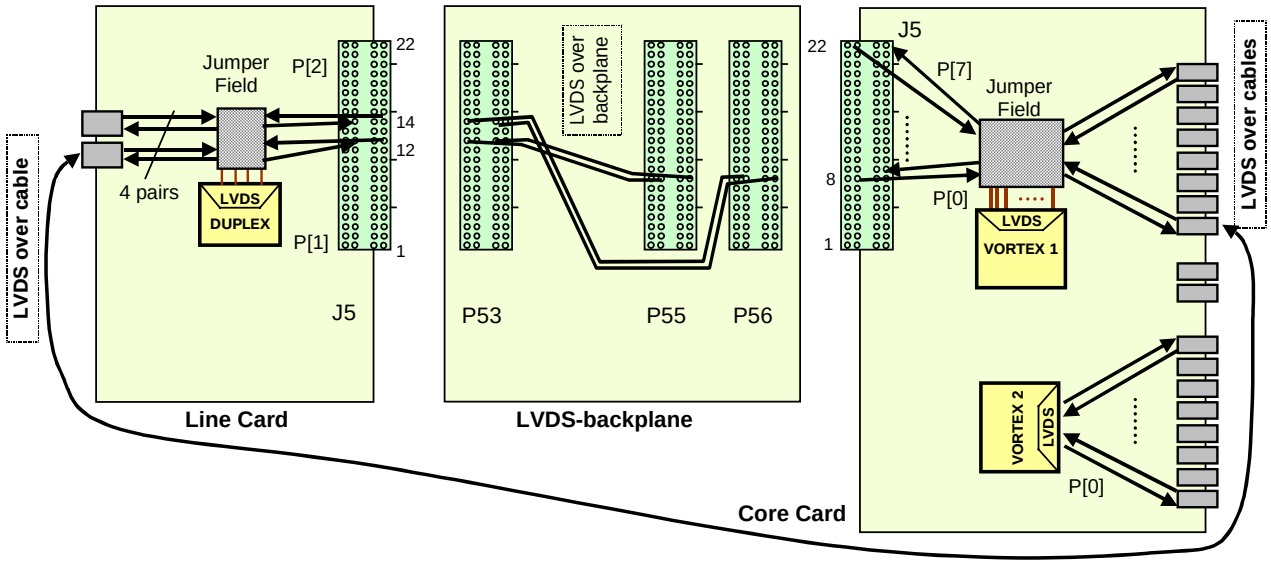
Figure 24. Line Card and Core Card interface to LVDS-Backplane



The Line Card at slot 3 provides an interface to the S/UNI-DUPLEX through rows 12 and 14 at J5/P53 to the LVDS-backplane. Port P[1] is wired from P53 row-12 to P55 at row-8. Core Card 1 at slot-5 can interface those lines to the S/UNI-VORTEX-1 port P[0]. Line Card S/UNI-DUPLEX Port P[2] is wired from P53 row-14 to P56 at row-8. Core Card 2 at slot-6 can interface those lines to S/UNI-VORTEX-1 port P[0] as well. The jumper fields associated with the described LVDS paths are set to the backplane interface.

You can execute the same path, from S/UNI-DUPLEX_P[1] to S/UNI-VORTEX-1_P[0] using an external cable, as shown in the above diagram. The jumper fields associated with S/UNI-DUPLEX and S/UNI-VORTEX-1 have to be configured appropriately. S/UNI-VORTEX-1 and 2 on CC can have all the LVDS lines connected through a front plate LVDS interface using dedicated IEEE 1394 connectors and cables.

Figure 22 shows an example of a WAN Card placement at slot 7/8 and a Core Card at slot 5/6.

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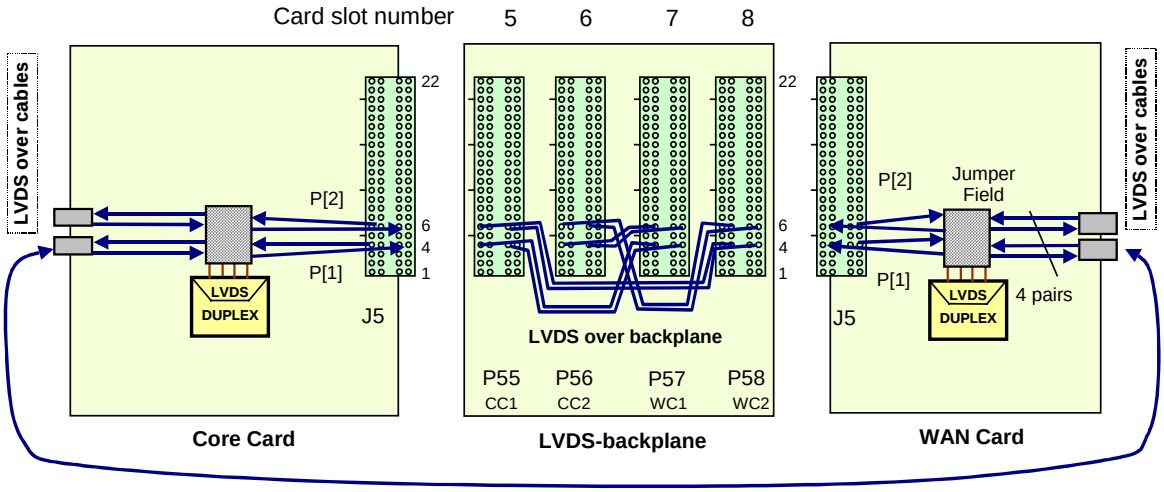
Figure 25. Example of WAN Card and Core Card Connection



The WAN Cards can be placed at slot-7 and slot-8. WAN Card at Slot-8 provides an interface to the S/UNI-DUPLEX through rows 4 and 6 at J5/P58 to the LVDS-backplane. Slot-8 Port[1] on the WAN Card is wired over the LVDS-backplane to P55 row 6 (at slot-5), and Port[2] is wired to P56 row 6 (at slot-6). If the WAN Card is at Slot-7, then the S/UNI-DUPLEX Port[1] is wired to P55 row 4, and Port[2] is wired to P56 row 4.

Jumper fields associated with the described LVDS path are set to the backplane interface.

The same path S/UNI-DUPLEX- S/UNI-DUPLEX can be executed with an external cable (as shown in Figure 25). In this case, jumper fields have to be configured before the card is inserted into the DSLAM shelf.

5.5. LVDS Termination on DSLAM Shelf

The ability to select between backplane or front panel LVDS connections allows for possible misconfiguration that results in unterminated lines. Theoretically, unused inputs and outputs can be left unterminated, but it is always good engineering practice to terminate floating lines. Figure 23 shows how the unconnected lines can be terminated with resistor networks to minimize back reflections and interference.

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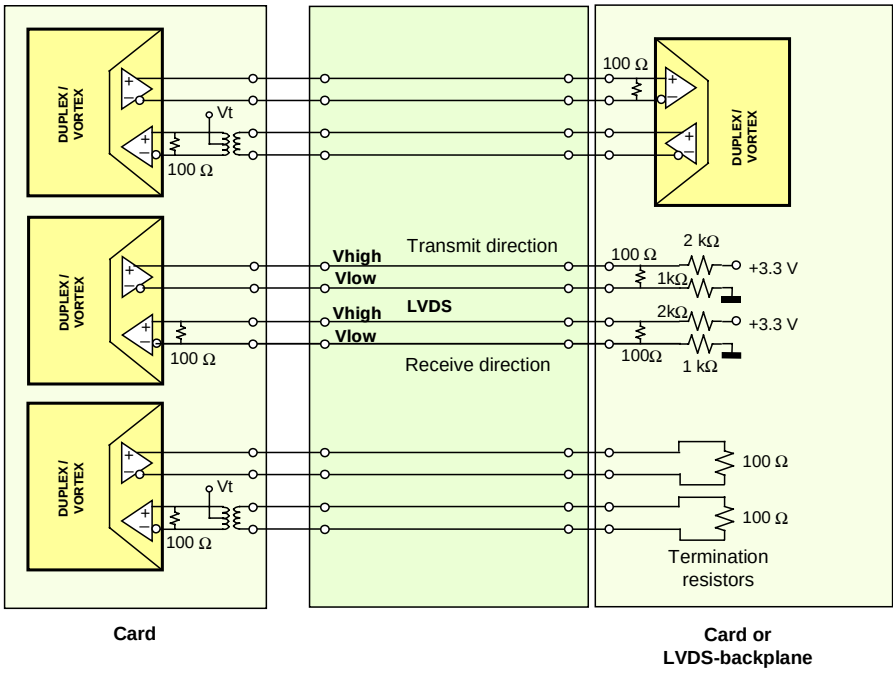
Figure 26. Unconnected LVDS Termination



The unused LVDS output drivers should be terminated with 100 ohm resistor. The unused LVDS inputs have bias voltage derived from a resistor network consisting of a 2.2 kohm, a 1 kohm, and a 100 ohm resistors. The 2.2 kohm resistors pulls up the “+” input to 3.3 V, and the 1 kohm pulls down the “-“ input to ground. The resistive divider creates about 60 mV of differential voltage (across pins Vhigh and Vlow above). Input termination prevents noise and interference pick-up. The output termination prevents back reflections, and may reduce crosstalk and total board noise.

NOTE: The S/UNI-DUPLEX and S/UNI-VORTEX LVDS receivers have build-in hysteresis, which helps to prevent transitions on unconnected ports with moderate interference coupling.

Designs supporting transformer or capacitive coupling can have the input termination with a single 100 ohm resistor across the LVDS lines. Consequently, the hysteresis at the LVDS input may prevent noise from generating valid transitions. This is important, as the loss of signal (LOS) at the S/UNI-DUPLEX and S/UNI-VORTEX LVDS interface is declared after a specific number of missing transitions (steady logic “high” or “low”). The noise pick-up may prevent or delay declaration of the LOS alarm. However, the S/UNI-DUPLEX or S/UNI-

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VORTEX internal cell processor should be able to detect the Loss of Cell Delineation (LCD) and declare an LCD alarm in that case.

It was chosen for this DSLAM application to terminate all types of floating inputs and outputs with the same type of the three-resistor network. That terminates adequately DC, capacitive and transformer coupled interfaces (may create small DC current across transformer coil). Termination resistors may be assembled on WAN and Line Cards to provide termination to most unterminated LVDS lines.

Configuration of cable interfaces cannot be determined the same way as the backlplane interface; therefore, the front panel LVDS lines may be left floating depending on the cable connection. The system management entity can disable LVDS transmitters on specific, unconnected LVDS ports. If interference is suspected, connectors with termination resistors may be plugged into LVDS front panel interfaces, as an option.

5.5.1. Power Rails on the LVDS-Backplane

The LVDS-backplane provides optional screw terminals for +5 V, +3.3 V, and ground. Terminals are not assembled as standard parts. For a specific development needs, power rails can supply current to a rear panel I/O, as the hot swap compatibility may require the front card to feed power to the rear panel I/O.

Power coupling capacitors are associated with power pins on each connected connector.

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6. CONNECTOR PINOUT ON DSLAM BACKPLANE

This section defines the pinout on P5x connectors mounted on the LVDS-backplane.

Pins are defined for each P5x connector separately and are presented in their corresponding tables. The pin naming convention for LVDS interfaces is referred after S/UNI-VORTEX and S/UNI-DUPLEX ports present on the Core Card. The Core Card can be inserted at slot 5 and slot 6, and all LVDS lines terminate into one of these card slots.

The pin naming convention is explained by the following examples. TABLE 4 (page 58) names connector P53 pin A14 as ”RXDN0 P56-A8”. The ”RXDN0” name refers to the S/UNI-VORTEX-1 RXDN0 negative input. This S/UNI-VORTEX is mounted on the Core Card. The ”P56-A8” points to connector P56 pin A8, where Core Card 2 is sitting and terminating the LVDS interface. A copper trace connects pins P53-A14 and P56-A8 TABLE 7 (on page 61) names connector P56 pin A8 as ”RXDN0 P53-A14”. The ”RXDN0” name points again to S/UNI-VORTEX-1 RXDN0 input at the Core Card, and ”P53-A14” points to connector P53 pin A14. The RXDN0 input at Core Card 2 (S/UNI-VORTEX-1), which is placed at slot 6 (connector P56), needs the corresponding S/UNI-DUPLEX LVDS output at the Line Card, which is placed at slot 3 (connector P53).

Every active LVDS connection has a S/UNI-VORTEX or S/UNI-DUPLEX port number and a destination connector pin typed into the corresponding table. The *S/UNI-DUPLEX* ports are distinct by *italic* font.

LVDS-backplane connector names are derived by taking CompactPCI connector names and adding the slot position, for example: P51 is the P5 connector at slot 1. DSLAM cards must have connectors named J1, J2 … J5. The pin assignment on the backplane is a front view (top view). Pin rows are ZABCDEF, and cards have pin rows mirrored to FEDCBAZ. Designers must ensure the connector interface is properly wired.

Row numbering on all cPCI connectors starts from high to low, as described in PICMG standard [13].

DSLAM cards and the cPCI backplane may use color and number coded keys at J1/P1 connector only. The main goal of keying is to make sure the +3.3 V and +5 V PCI cards operate in an appropriate environment. This Reference Design backplane P5 connector has no key coding; therefore, the DSLAM cards can not be keyed for any specific slot.

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6.1. P51 at Slot 1

TABLE 2 shows the P51 connector pinout.

TABLE 2. P51 at Slot-1

	Pin						
Row	Z	A	B	C	D	E	F
22	GND	x	X	x	x	x	GND
21	GND	x	X	x	x	x	GND
20	GND	x	X	x	x	x	GND
19	GND	x	X	x	x	x	GND
18	GND	x	X	x	x	x	GND
17	GND	x	X	x	x	x	GND
16	GND	x	X	x	x	x	GND
15	GND	x	x	x	x	x	GND
14	GND	x	x	x	x	x	GND
13	GND	x	x	x	x	x	GND
12	GND	x	x	x	x	x	GND
11	GND	x	x	x	x	x	GND
10	GND	x	x	x	x	x	GND
9	GND	x	x	x	x	x	GND
8	GND	x	x	x	x	x	GND
7	GND	x	x	x	x	x	GND
6	GND	x	x	x	x	x	GND
5	GND	x	x	x	x	x	GND
4	GND	x	x	x	x	x	GND
3	GND	x	x	x	x	x	GND
2	GND	x	x	x	x	x	GND
1	GND	x	x	x	x	x	GND

Most pins are left unconnected.

The P51 connector supports the host CPU rear panel I/O card that interfaces to the peripheral hardware.

The connector should be assembled with the rear panel I/O option, if access to peripheral components is anticipated during development and shelf operation.

The DSLAM Reference Design LVDS-backplane is assembled with a connector for a rear panel I/O (extended length pins and additional plastic shell).

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6.2. P52 at Slot 2

TABLE 3 shows the pinout for the P52 connector at slot 2.

TABLE 3. P52 at slot-2

	Pin							(Line or WAN Card Interface)
Row	Z	A	B	C	D	E	F	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	x	x	x	x	x	GND	
17	GND	x	x	x	x	x	GND	
16	GND	x	x	x	x	x	GND	
15	GND	x	x	x	x	x	GND	
14	GND	*(TXD2-) J23-4*	*(TXD2+) J23-3*	x	*(RXD2+) J23-6*	*(RXD2-) J23-5*	GND	(S/UNI-DUPLEX P[2]) Connector
13	GND	GND	GND	x	GND	GND	GND	
12	GND	*(TXD1-) J22-4*	*(TXD1+) J22-3*	x	*(RXD1+) J22-6*	*(RXD1-) J22-5*	GND	(S/UNI-DUPLEX P[1]) Connector
11	GND	x	x	x	x	x	GND	
10	GND	x	x	x	x	x	GND	
9	GND	x	x	x	x	x	GND	
8	GND	x	x	x	x	x	GND	
7	GND	x	x	x	x	x	GND	
6	GND	*(TXD2-) J21-4*	*(TXD2+) J21-3*	x	*(RXD2+) J21-6*	*(RXD2-) J21-5*	GND	(S/UNI-DUPLEX P[2]) Connector
5	GND	GND	GND	x	GND	GND	GND	
4	GND	*(TXD1-) J20-4*	*(TXD1+) J20-3*	x	*(RXD1+) J20-6*	*(RXD1-) J20-5*	GND	(S/UNI-DUPLEX P[1]) Connector
3	GND	S2 P55-	Card20 P55-x	Card21 P55-x x	x	x	GND	Slot and Card Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

Connector P52 is usually obstructed with the host CPU card. This connector has no rear panel I/O extension.

If a Line Card or WAN Card is placed at slot 2, the connected pins provide optional test termination for the S/UNI-DUPLEX interface onthe Line Card or WAN Card that is used.

NOTE: LVDS interfaces shown in brackets refer to S/UNI-DUPLEX ports on the Line Card or WAN Card, which can be placed at slot 2, as an option.

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6.3. P53 at Slot 3

TABLE 4 shows the pinout for the P53 connector at slot 3.

TABLE 4. P53

	Pin							Core Card LVDS
Row	Z	A	B	C	D	E	F	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	x	x	x	x	x	GND	
17	GND	x	x	x	x	x	GND	
16	GND	x	x	x	x	x	GND	
15	GND	x	x	x	x	x	GND	
14	GND	RXDN0 P56-A8	RXDP0 P56-B8	x	TXDP0 P56-D8	TXDN0 P56-E8	GND	S/UNI-VORTEX-1 P[0] on CC2
13	GND	GND	GND	x	GND	GND	GND	
12	GND	RXDN0 P55-A8	RXDP0 P55-B8	x	TXDP0 P55-D8	TXDN0 P55-E8	GND	S/UNI-VORTEX-1 P[0] on CC1
11	GND	x	x	x	x	x	GND	
10	GND	x	x	x	x	x	GND	
9	GND	x	x	x	x	x	GND	
8	GND	x	x	x	x	x	GND	
7	GND	x	x	x	x	x	GND	
6	GND	*J31-4*	*J31-3*	x	*J31-6*	*J31-5*	GND	Connector
5	GND	GND	GND	x	GND	GND	GND	
4	GND	*J30-4*	*J30-3*	x	*J30-6*	*J30-5*	GND	Connector
3	GND	S3 P55-	Card30 P55-x	Card31 P55-x x	x	x	GND	Slot and Card Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

NOTE: For pins that are dedicated to the LVDS, refer to the S/UNI-VORTEX-1 and S/UNI-DUPLEX LVDS interfaces on the Core Card.

Rows 12 and 14 provide an interface to the S/UNI-DUPLEX on the Line Card to the LVDS-backplane, and then to S/UNI-VORTEX-1 on the Core Card. Rows 4 and 6 provide optional termination on the S/UNI-DUPLEX interface for the WAN Card into a header pin, if WAN Card is placed at slot 3. Row 3 terminates Slot and Card Type optional lines.

Connector P53 usually mates with a Line Card.

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6.4. P54 at Slot 4

TABLE 5 shows the pinout for the P54 connector at slot 4.

TABLE 5. P54 at Slot 4

	Pin							Core Card LVDS
Row	Z	A	B	C	D	E	F	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	x	x	x	x	x	GND	
17	GND	x	x	x	x	x	GND	
16	GND	x	x	x	x	x	GND	
15	GND	x	x	x	x	x	GND	
14	GND	RXDN0 P56-A8	RXDP0 P56-B8	x	TXDP0 P56-D8	TXDN0 P56-E8	GND	S/UNI-VORTEX-1 P[0] on CC2
13	GND	GND	GND	x	GND	GND	GND	
12	GND	RXDN0 P55-A8	RXDP0 P55-B8	x	TXDP0 P55-D8	TXDN0 P55-E8	GND	S/UNI-VORTEX-1 P[0] on CC1
11	GND	x	x	x	x	x	GND	
10	GND	x	x	x	x	x	GND	
9	GND	x	x	x	x	x	GND	
8	GND	x	x	x	x	x	GND	
7	GND	x	x	x	x	x	GND	
6	GND	*J41-4*	*J41-3*		*J41-6*	*J41-5*	GND	Connector
5	GND	GND	GND		GND	GND	GND	
4	GND	*J40-4*	*J40-3*		*J40-6*	*J40-5*	GND	Connector
3	GND	S4 P55-	Card40 P55-x	Card41 P55-x x	x	x	GND	Slot and Card Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

NOTE: For pins dedicated to the LVDS, refer to the S/UNI-VORTEX-1 and S/UNI-DUPLEX LVDS interfaces on the Core Card.

Connector P54 usually mates with a Line Card.

Rows 12 and 14 provide an interface to the S/UNI-DUPLEX on the Line Card to the LVDS-backplane and then to the S/UNI-VORTEX-1 on the Core Card. Rows 4 and 6 provide optional termination on the S/UNI-DUPLEX interface for a WAN Card into a header connector, if the WAN Card is placed at slot 3._Row 3 terminates Slot and Card Type optional lines.

The connector is assembled with the rear panel I/O option.

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6.5. P55 at Slot 5

TABLE 6 shows the pin description for P55 at slot 5.

TABLE 6. P55 at Slot 5

	Pin							Core Card 1 LVDS
Row	Z	A	B	C	D	E	F	
22	GND	RXDN7 J57-4	RXDP7 J57-3	GND	TXDP7 J57-6	TXDN7 J57-5	GND	S/UNI-VORTEX-1
21	GND	GND	GND	tbd	GND	GND	GND	
20	GND	RXDN6 J56-4	RXDP6 J56-3	GND	TXDP6 J56-6	TXDN6 J56-5	GND	S/UNI-VORTEX-1
19	GND	GND	GND	tbd	GND	GND	GND	
18	GND	RXDN5 J55-4	RXDP5 J55-3	GND	TXDP5 J55-6	TXDN5 J55-5	GND	S/UNI-VORTEX-1
17	GND	GND	GND		GND	GND	GND	
16	GND	RXDN4 P58-A12	RXDP4 P58-B12	GND	TXDP4 P58-D12	TXDN4 P58-E12	GND	S/UNI-VORTEX-1
15	GND	GND	GND	S2 P52-A3	GND	GND	GND	
14	GND	RXDN3 P57-A12	RXDP3 P57-B12	GND	TXDP3 P57-D12	TXDN3 P57-E12	GND	S/UNI-VORTEX-1
13	GND	GND	GND	S3 P53-A3	GND	GND	GND	
12	GND	RXDN2 P56-A12	RXDP2 P56-B12	GND	TXDP2 P56-D12	TXDN2 P56-E12	GND	S/UNI-VORTEX-1
11	GND	GND	GND	S4 P54-A3	GND	GND	GND	
10	GND	RXDN1 P54-A12	RXDP1 P54-B12	GND	TXDP1 P54-D12	TXDN1 P54-E12	GND	S/UNI-VORTEX-1
9	GND	GND	GND	S6 P56-A3	GND	GND	GND	
8	GND	RXDN0 P53-A12	RXDP0 P53-B12	GND	TXDP0 P53-D12	TXDN0 P53-E12	GND	S/UNI-VORTEX-1
7	GND	GND	GND	S7 P57-A3	GND	GND	GND	
6	GND	*RXD2- P58-A4*	*RXD2+ P58-B4*	GND	*TXD2+ P58-D4*	*TXD2+ P58-E4*	GND	S/UNI-DUPLEX P[2] to WAN
5	GND	GND	GND	S8 P58-A3	GND	GND	GND	
4	GND	*RXD1- P57-A4*	*RXD1+ P57-B4*	GND	*TXD1+ P57-D4*	*TXD1- P57-E4*	GND	S/UNI-DUPLEX P[1] to WAN
3	GND	x	x	x	Card81 P58-B3	Card80 P58-C3	GND	Optional backplane Lines
2	GND	Card21 P52-B3	Card31 P53-B3	Card41 P54-B3	Card61 P56-B3	Card71 P57-B3	GND	
1	GND	Card20 P52-C3	Card30 P53-C3	Card40 P54-C3	Card60 P56-C3	Card70 P57-C3	GND	

P55 supports the LVDS interface on the S/UNI-VORTEX-1 P[7:0] and S/UNI-DUPLEX (WAN interface) that is mounted on Core Card 1. Rows 8 through 22 provide an interface to other P5x slots to S/UNI-VORTEX-1 on Core Card 1. Rows 4 and 6 provide an interface to the S/UNI-DUPLEX on Core Card 1. P56

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allows connection to all eight LVDS ports P[7:0] from the S/UNI-VORTEX-1 to the LVDS-backplane.

The optional lines, at rows 1, 2, and 3, and column C, are not critical for the design.

6.6. P56 at Slot 6

TABLE 7 shows the pin description for P56 at slot 6.

TABLE 7. P56 at Slot-6

	Pin							Core Card LVDS
Row	Z	A	B	C	D	E	F	
22	GND	RXDN7 J67-4	RXDP7 J67-3	GND	TXDP7 J67-6	TXDN7 J67-5	GND	S/UNI-VORTEX-1
21	GND	GND	GND	x	GND	GND	GND	
20	GND	RXDN6 J66-4	RXDP6 J66-3	GND	TXDP6 J66-6	TXDN6 J66-5	GND	S/UNI-VORTEX-1
19	GND	GND	GND	x	GND	GND	GND	
18	GND	RXDN5 J65-4	RXDP5 J65-3	GND	TXDP5 J65-6	TXDN5 J55-5	GND	S/UNI-VORTEX-1
17	GND	GND	GND	x	GND	GND	GND	
16	GND	RXDN4 P58-A14	RXDP4 P58-B14	GND	TXDP4 P58-D14	TXDN4 P58-E14	GND	S/UNI-VORTEX-1
15	GND	GND	GND	x	GND	GND	GND	
14	GND	RXDN3 P57-A14	RXDP3 P57-B14	GND	TXDP3 P57-D14	TXDN3 P57-E14	GND	S/UNI-VORTEX-1
13	GND	GND	GND	x	GND	GND	GND	
12	GND	RXDN2 P55-A14	RXDP2 P55-B12	GND	TXDP2 P55-D12	TXDN2 P55-E12	GND	S/UNI-VORTEX-1 (to Line Card)
11	GND	GND	GND	x	GND	GND	GND	
10	GND	RXDN1 P54-A14	RXDP1 P54-B14	GND	TXDP1 P54-D14	TXDN1 P54-E14	GND	S/UNI-VORTEX-1
9	GND	GND	GND	x	GND	GND	GND	
8	GND	RXDN0 P53-A14	RXDP0 P53-B14	GND	TXDP0 P53-D14	TXDN0 P53-E14	GND	S/UNI-VORTEX-1
7	GND	GND	GND	x	GND	GND	GND	
6	GND	*RXD2- P58-A6*	*RXD2+ P58-B6*	GND	*TXD2+ P58-D6*	*TXD2+ P58-E6*	GND	*S/UNI-DUPLEX P[2] to WAN*
5	GND	GND	GND	x	GND	GND	GND	
4	GND	*RXD1- P57-A6*	*RXD1+ P57-B6*	GND	*TXD1+ P57-D6*	*TXD1- P57-E6*	GND	*S/UNI-DUPLEX P[1] to WAN*
3	GND	P55-C9	P55-D2	P55-D1	x	x	GND	Card Present and Card Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

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NOTE: For pins dedicated to the LVDS, refer to the S/UNI-VORTEX-1 and S/UNI-DUPLEX LVDS interfaces on the Core Card.

P56 supports the LVDS interface on the S/UNI-VORTEX-1 P[7:0] and S/UNI-DUPLEX (WAN interface) that is mounted on Core Card 2. Rows 8 through 16, excluding row 12, provide an interface to other P5x slots to the S/UNI-VORTEX-1 on Core Card 2. Row 12 is dedicated to the optionally placed Line Card at this slot. The Line Card provides an interface to its S/UNI-DUPLEX to the S/UNI-DUPLEX on Core Card 1. Rows 18, 20, and 22 terminate S/UNI-VORTEX-1 into optional header connectors. Rows 4 and 6 interface S/UNI-DUPLEX on Core Card 2. To WAN cards at slot- 7 and 8.

P56 allows connection to all eight LVDS ports P[7:0] from the S/UNI-VORTEX-1 to the LVDS-backplane.

Connector P56 usually mates with Core Card 2.

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6.7. P57 at Slot 7

TABLE 8shows the pin description for the P57 connector at slot 7.

TABLE 8. P57 at Slot 7

	Pin							Core Card LVDS
Row	Z	A	B	C	D	E	F	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	x	x	x	x	x	GND	
17	GND	x	x	x	x	x	GND	
16	GND	x	x	x	x	x	GND	
15	GND	x	x	x	x	x	GND	
14	GND	RXDN3 P56-A14	RXDP3 P56-B14	x	TXDP3 P56-D14	TXDN3 P56-E14	GND	S/UNI-VORTEX-1 on CC2
13	GND	GND	GND	x	GND	GND	GND	
12	GND	RXDN3 P55-A14	RXDP3 P55-B14	x	TXDP3 P55-D14	TXDN3 P55-E14	GND	S/UNI-VORTEX-1 on CC1
11	GND	x	x	x	x	x	GND	
10	GND	x	x	x	x	x	GND	
9	GND	x	x	x	x	x	GND	
8	GND	x	x	x	x	x	GND	
7	GND	x	x	x	x	x	GND	
6	GND	*RXD2- P56-A4*	*RXD2+ P56-B4*	x	*TXD2+ P56-D4*	*TXD2+ P56-E4*	GND	*S/UNI-DUPLEX P[2] on CC2*
5	GND	GND	GND	x	GND	GND	GND	
4	GND	*RXD1- P55-A6*	*RXD1+ P55-B6*	x	*TXD1+ P55-D6*	*TXD1+ P55-E6*	GND	*S/UNI-DUPLEX P[1] on CC1*
3	GND	S7 P55-C7	Card71 P55-E2	Card70 P55-E1	x	x	GND	Slot and Card Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

NOTE: For pins dedicated to the LVDS, refer to the S/UNI-VORTEX-1 and S/UNI-DUPLEX LVDS interfaces on the Core Card.

Rows 12 and 14 provide an optional interface to the S/UNI-DUPLEX on the Line Card, if the Line Card is placed at slot 7. Rows 4 and 6 terminate the S/UNI-DUPLEX on a WAN Card Core Cards 1 or 2. Row 3 terminates “Slot” and “Card Type” optional lines.

Connector P57 usually mates with a WAN Card.

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6.8. P58 at Slot 8

TABLE 9 shows the pinout for the P58 connector at slot 8.

TABLE 9. P58 at slot-8

	Pin							Core Card LVDS
Row	Z	A	B	C	D	E	F	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	x	x	x	x	x	GND	
17	GND	x	x	x	x	x	GND	
16	GND	x	x	x	x	x	GND	
15	GND	x	x	x	x	x	GND	
14	GND	RXDN4 P56-A16	RXDP4 P56-B16	x	TXDP4 P56-D16	TXDN4 P56-E16	GND	S/UNI-VORTEX-1 on CC2
13	GND	GND	GND	x	GND	GND	GND	
12	GND	RXDN4 P55-A16	RXDP4 P55-B16	x	TXDP4 P55-D16	TXDN4 P55-E16	GND	S/UNI-VORTEX-1 on CC1
11	GND	x	x	x	x	x	GND	
10	GND	x	x	x	x	x	GND	
9	GND	x	x	x	x	x	GND	
8	GND	x	x	x	x	x	GND	
7	GND	x	x	x	x	x	GND	
6	GND	*RXD2- P56-A6*	*RXD2+ P56-B6*	x	*TXD2+ P56-D6*	*TXD2+ P56-E6*	GND	*S/UNI-DUPLEX P[2] on CC1*
5	GND	GND	GND	x	GND	GND	GND	
4	GND	*RXD1- P55-A6*	*RXD1+ P55-B6*	x	*TXD1+ P55-D6*	*TXD1+ P55-E6*	GND	*S/UNI-DUPLEX P[1] on CC2*
3	GND	S8 P55-C5	Card81 P55-D3	Card80 P55-E3	x	x	GND	Slot and Card Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

NOTE: For pins dedicated to the LVDS refer to the S/UNI-VORTEX-1 and S/UNI-DUPLEX LVDS interfaces on Core Card 1.

Rows 12 and 14 optionally interface the S/UNI-DUPLEX on a Line Card, if the Line Card is placed at slot-8. Rows 4 and 6 terminate the S/UNI-DUPLEX on a WAN Card through the backplane to S/UNI-VORTEX-1 on both Core Cards. Row 3 terminates “Slot” and “Card Type” optional lines.

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Connector P58 is usually populated with a WAN Card.

NOTE: LVDS pinout assigned for each card may create very small trace length difference (about 0.1 inch) due to different pin length in Z-pack connector.

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7. PINOUT ON DSLAM CARDS

This section specifies the pinout on selected connectors for the Core Card, Line Card, and WAN Card. This section describes the cPCI backplane interface, the LVDS-backplane on J5, and the LVDS front plate interface. The DS-3, E1/DS-1, and microprocessor serial port interface, specific to the WAN Card and Line Card, is described in the Reference Design documents for each card. The 8 kHz interface on the Core Card is described in the Core Card Reference Design document.

NOTE: All connectors that mate with the backplane must follow the cPCI backplane convention. Connectors on each card are named J1, J2, J3, J4, and J5. If one or more connectors are not populated, then the name should be retired. This requirement is imposed to avoid confusion and bring uniform connector naming.

Pins are defined for each J5 connector per card type and are presented in corresponding tables. Connectors J1 through J4 are referred in general terms and have no pinout shown.

The LVDS interface associated with pins refer to LVDS interfaces on the S/UNI-VORTEX or S/UNI-DUPLEX that is mounted on the particular card. (The LVDS-backplane pinout shown in the previous section was referred to the LVDS on the Core Card.)

Some connectors may have pins with reference to the terminating resistors for floating LVDS interfaces. Those terminating networks are referred to as “Vhigh” and “Vlow”.

Figure 26 (page 53) shows the resistor connections for each pin type. For example, TABLE 10 (next page) shows pin A18 with the name ”RN11_Vlow”, which points to a negative nod in the resistive network, as explained and shown in Figure 26. The ”RN11_Vhigh” name points to the positive nod in the same network. Resistor network number is inserted only to identify two corresponding nodes. All resistors are optionally mounted at the WAN and Line Cards.

The WAN and Line Cards placed on a shelf without the LVDS-backplane and/or without a Core Card should be configured to the front panel LVDS interfaces and properly terminated through shelf cabling.

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7.1. Line Card Backplane Conenctors

This section specifies the pinout on the J5 connector and describes other cPCI connectors.

7.1.1. J5 on Line Card

TABLE 10 shows the Line Card components that are connected to J5.

NOTE: All pin names refer to components that are placed on the Line Card.

TABLE 10. Pinout on J5 on the Line Card

	Pin							LVDS on WAN Card
Row	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	RN11_Vlow	RN11_Vhigh	GND	RN12_ Vhigh	RN12_ Vlow	GND	
17	GND	x	x	x	x	x	GND	
16	GND	RN9_ Vlow	RN9_ Vhigh	GND	RN10_ Vhigh	RN10_ Vlow	GND	
15	GND	x	x	x	x	x	GND	
14	GND	*TXD2-DPLX-P[2]*	*TXD2+ DPLX-P[2]*	GND	*RXD2+ DPLX-P[2]*	*RXD2- DPLX-P[2]*	GND	*S/UNI-DUPLEX P[2]*
13	GND	GND	GND	x	GND	GND	GND	
12	GND	*TXD1-DPLX-P[1]*	*TXD1+ DPLX-P[1]*	GND	*RXD1+ DPLX-P[1]*	*RXD1- DPLX-P[1]*	GND	*S/UNI-DUPLEX P[1]*
11	GND	x	x	x	x	x	GND	
10	GND	RN7_Vlow	RN7_ Vhigh	GND	RN8_ Vhigh	RN8_ Vlow	GND	
9	GND						GND	
8	GND	RN5_ Vlow	RN5_ Vhigh	GND	RN6_ Vhigh	RN6_ Vlow	GND	
7	GND	GND	GND	x	GND	GND	GND	
6	GND	RN3_ Vlow	RN3_ Vhigh	GND	RN4_ Vhigh	RN4_ Vlow	GND	Connector
5	GND	GND	GND	x	GND	GND	GND	
4	GND	RN1_ Vlow	RN1_ Vhigh	GND	RN2_ Vhigh	RN2_ Vlow	GND	Connector
3	GND	200Ω to +3.3V	200Ω to +3.3V	-	x	x	GND	Card Presence and Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

DPLX-P[1] – means S/UNI-DUPLEX Port[1], etc.

NOTE: The rows are marked as “ZABCDEF”, which may be mirrored on the Line Card printed circuit board (and schematic). Care must be taken to wire the J5 connector properly on the Line Card.

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The resistor network that terminate the LVDS lines are optional on the Line Card (and WAN Card). If the resistor network is not assembled, it should have no adverse effect on DSLAM shelf performance.

7.1.2. J4 on Line Card

The J4 connector is not needed on the DSLAM Reference Design Line Card.

7.1.3. J3 on Line Card

The J3 connector is not needed on the DSLAM Reference Design Line Card.

J3 must not exist on any card that mates with the DSLAM development shelf. If J3 is present, the metal rail will prevent card insertion.

7.1.4. J2 on Line Card

The J2 connector is not needed on the Line Card.

7.1.5. J1 on Line Card

The J1 connector that mates with P1 on the 3U cPCI backplane provides power to the Line Card. The cPCI bus has no connection and all digital lines must be left unconnected.

J1 must be used to provide hot-swap capability by staggered pins, which are sensed when inserting and removing the Line Card from the DSLAM shelf.

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7.2. WAN Card Pinout

This section specifies the pinout on the J5 connector and describes other cPCI connectors.

7.2.1. J5 on WAN Card

TABLE 11 shows the WAN Card components that are connected to J5..

TABLE 11. Pinout on J5 on WAN Card

	Pin							LVDS on WAN Card
Row	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	
22	GND	x	x	x	x	x	GND	
21	GND	x	x	x	x	x	GND	
20	GND	x	x	x	x	x	GND	
19	GND	x	x	x	x	x	GND	
18	GND	x	x	x	x	x	GND	
17	GND	x	x	x	x	x	GND	
16	GND	x	x	x	x	x	GND	
15	GND	x	x	x	x	x	GND	
14	GND	RN3_Vlow	RN3_ Vhigh	x	RN4_ Vhigh	RN4_Vlow	GND	
13	GND	GND	GND	x	GND	GND	GND	
12	GND	RN1_Vlow	RN1_ Vhigh	x	RN2_ Vhigh	RN2_Vlow	GND	
11	GND	x	x	x	x	x	GND	
10	GND	x	x	x	x	x	GND	
9	GND	x	x	x	x	x	GND	
8	GND	x	x	x	x	x	GND	
7	GND	GND	GND	x	GND	GND	GND	
6	GND	*TXD2-DPLX-P[2]*	*TXD2+ DPLX-P[2]*	GND	*RXD2+ DPLX-P[2]*	*RXD2-DPLX-P[2]*	GND	*S/UNI-DUPLEX P[2]*
5	GND	GND	GND	x	GND	GND	GND	
4	GND	*TXD1-DPLX-P[1]*	*TXD1+ DPLX-P[1]*	GND	*RXD1+ DPLX-P[1]*	*RXD1-DPLX-P[1]*	GND	*S/UNI-DUPLEX P[1]*
3	GND	200Ω to +3.3V	200Ω to +3.3V	200Ω to +3.3V	x	x	GND	Card Presence and Type
2	GND	x	x	x	x	x	GND	
1	GND	x	x	x	x	x	GND	

DPLX-P[1] – means S/UNI-DUPLEX Port[1], etc.

All pin names refer to the components placed on the WAN Card.

NOTE: The rows that are marked above in order as *ZABCDEF* may be mirrored on the WAN Card schematic. Care must be taken towire the J5 connector properly on the WAN Card.

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7.2.2. J4 on WAN Card

The J4 connector is not needed on the DSLAM Reference Design WAN Card.

7.2.3. J3 on WAN Card

The J3 connector is not needed on the DSLAM Reference Design WAN Card.

J3 must not exist on any card that mates with the DSLAM shelf. If J3 is present, the metal rail will prevent card insertion.

7.2.4. J2 on WAN Card

The J2 connector is not needed on the DSLAM Reference Design WAN Card.

Most cPCI backplanes are assembled with the P2 connector.

7.2.5. J1 on WAN Card

The J1 connector that mates with P1 on the 3U cPCI backplane provides power to the WAN Card. The cPCI bus has no connection, and all digital lines must be left unconnected.

J1 must be used to provide hot-swap capability by staggered pins, which are sensed when inserting and removing the WAN Card from the DSLAM-shelf.

7.3. Core Card Pinout

This section specifies the pinout on the J5 connector and describes other cPCI connectors.

7.3.1. J5 on Core Card

TABLE 12 shows the pin description for J5.

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TABLE 12. J5 at the Core Card

	Pin							Core Card Devices
Row	Z	A	B	C	D	E	F	
22	GND	RXDN7	RXDP7	GND	TXDP7	TXDN7	GND	Header V-1
21	GND	GND	GND	x	GND	GND	GND	
20	GND	RXDN6	RXDP6	GND	TXDP6	TXDN6	GND	S/UNI-VORTEX-1
19	GND	GND	GND	x	GND	GND	GND	
18	GND	RXDN5	RXDP5	GND	TXDP5	TXDN5	GND	S/UNI-VORTEX-1
17	GND	GND	GND		GND	GND	GND	
16	GND	RXDN4	RXDP4	GND	TXDP4	TXDN4	GND	S/UNI-VORTEX-1
15	GND	GND	GND	S2	GND	GND	GND	
14	GND	RXDN3	RXDP3	GND	TXDP3	TXDN3	GND	S/UNI-VORTEX-1
13	GND	GND	GND	S3	GND	GND	GND	
12	GND	RXDN2	RXDP2	GND	TXDP2	TXDN2	GND	S/UNI-VORTEX-1
11	GND	GND	GND	S4	GND	GND	GND	
10	GND	RXDN1	RXDP1	GND	TXDP1	TXDN1	GND	S/UNI-VORTEX-1
9	GND	GND	GND	S6	GND	GND	GND	
8	GND	RXDN0	RXDP0	GND	TXDP0	TXDN0	GND	S/UNI-VORTEX-1
7	GND	GND	GND	S7	GND	GND	GND	
6	GND	*RXD2-*	*RXD2+*	GND	*TXD2+*	*TXD2-*	GND	S/UNI-DUPLEX P[2]
5	GND	GND	GND	S8	GND	GND	GND	
4	GND	*RXD1-*	*RXD1+*	GND	*TXD1+*	*TXD1-*	GND	S/UNI-DUPLEX P[1]
3	GND	200Ω to +3.3V	x	200Ω to +3.3V	(Optional Card8)	(Optional Card8)	GND	Optional backplane Lines
2	GND	(Optional Card2)	(Optional Card3)	(Optional Card4)	(Optional Card6)	(Optional Card7)	GND	
1	GND	(Optional Card2)	(Optional Card3)	(Optional Card4)	(Optional Card6)	(Optional Card7)	GND	

Pin description in rows 4 through 22 corresponds to the LVDS interface on the Core Card. The optional interface lines in rows 1, 2, and 3, and also in column C are not critical for the design.

The pinout on J5 is compatible with the P55 and P56 connectors on the LVDS-backplane.

The J5 connector is mostly dedicated to the LVDS interfaces on the S/UNI-VORTEX-1 P[7:0] (Line interface) and S/UNI-DUPLEX (WAN interface). Optional control lines terminate on J5 as well. If those lines are not used, there is no adverse effect to card performance.

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The Core Card is intended for placement on the DSLAM shelf at slots 5 or 6.To prevent any damage, the Core Card should not be placed into the shelf with a backplane that supports the P5 connector with an unknown pinout. The LVDS interface is done with the S/UNI-DUPLEX supplied at 3.3 V. A +5 V rail may cause a high current through the clamping diodes, causing damage to the LVDS interface and the entire device. J5 has some pins connected to ground, which may cause a short circuit on a foreign backplane.

The Core Card is not equipped with a connector key that is designed to help prevent improper insertion on a cPCI backplane only.

7.3.2. J4 on Core Card

The J4 connector is not needed on the DSLAM Reference Design Core Card.

7.3.3. J3 on Core Card

The J3 connector on the Core Card is not needed.

7.3.4. J2 on Core Card

The J2 connector is not needed on the DSLAM Reference Design Core Card.

7.3.5. J1 on Core Card

The J1 connector that mates with P1 on the 3U cPCI backplane provides power to the Core Card for both +5 V and +3.3 V.

J1 is used to connect the 32-bit cPCI bus between the host CPU and the Core Card.

J1 must be used to provide hot-swap capability by staggered pins, which are sensed when inserting and removing the Core Card from the DSLAM shelf. J1 is equipped with a key to prevent improper insertion of the card .

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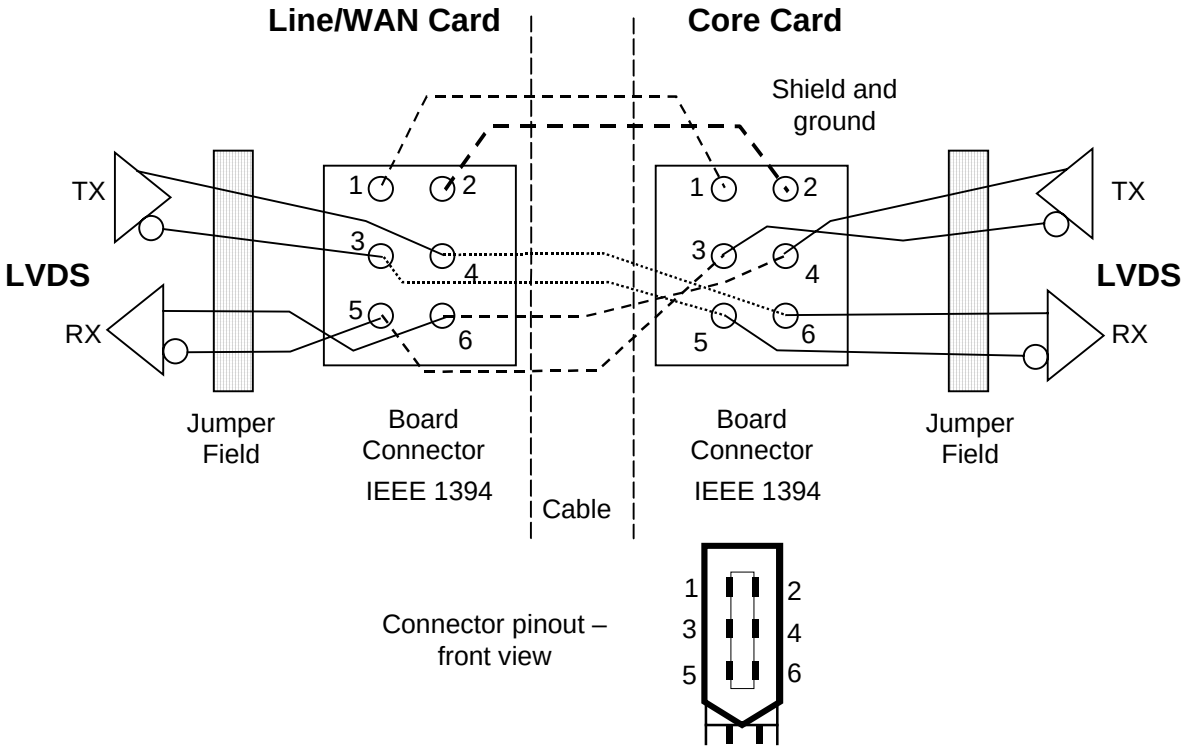
7.4. LVDS Interface on Card Front

Figure 27shows the LVDS connector pinout on the DSLAM cards.

Figure 27. LVDS Pinout on DSLAM Cards



The pinout is functional only. The physical interfaces have transformer or 0.22 uF to 1.0 uF serial capacitors on input and output. Inputs are biased with a resistive divider and line termination. Capacitors are permanently soldered without the bypass option. The transformer coupling on the Line Cards and WAN Cards can be modified for capacitor coupling through transformer de-soldering only. Jumper fields allow for the front panel or backplane interface.

The IEEE 1394 cable is wired with pins swapped on each end. That allows the same pinout on the Core Card and Line/WAN Cards. The IEEE-1394 cable crosses connections 3 to 5 and 4 to 6.

The pin numbered as “2” is connected to the chassis ground on all DSLAM cards.

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8. HARDWARE

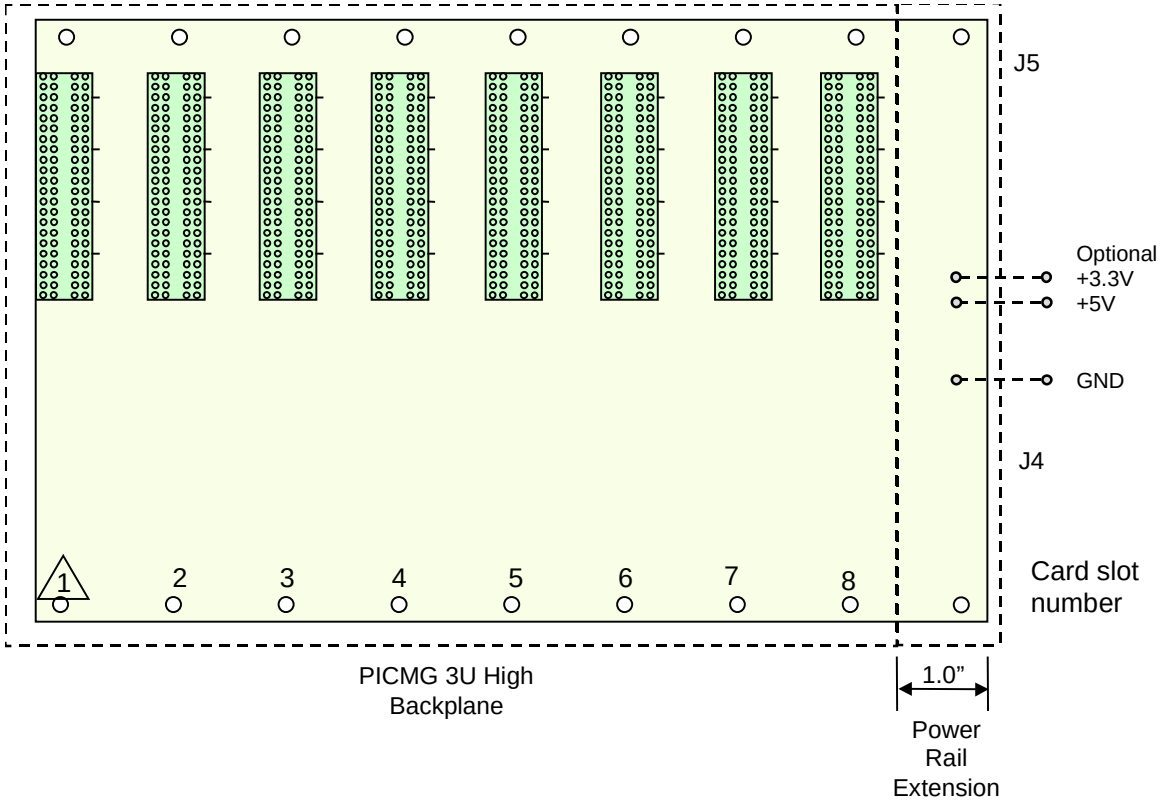
This section describes some hardware issues, mostly related to the mechanics of the LVDS-backplane and DSLAM shelf.

8.1. LVDS-backplane

The LVDS-backplane board dimensions must comply with the PICMG 2.0 Revision 2.1 CompactPCI standard for connectors and mounting holes placement. The LVDS-backplane follows 3U high dimensioning from that document. The Reference Design development shelf allows room for custom dimensioning on the right side, where optional power connectors can be assembled.

Figure 28 shows the physical dimensions of the LVDS board.

Figure 28. PCB



The power rail connectors require the board to be extended by 1 inch, as shown. Two mounting holes are also added. Screw terminals connect the power rail,

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which may be needed for application specific cards. If that option is not present, then the power supply is not needed forthe backplane.

8.2. Shelf Metal-work

The DSLAM development shelf is assembled with standard cPCI type aluminum rails and plates readily available from many vendors. Some rework is required.

The aluminum front plates are standard off-the-shelf plates with custom holes punched to accommodate front connectors and LEDs. Silkscreen labeling is applied onto the front plate.

8.3. Switching Power Supply

The DSLAM shelf is supplied with a switching power supply (SPS) available throughout the PC industry.

The DSLAM development shelf has provision for a permanent attachment of the SPS. The SPS can be mechanically detached to ease access to the shelf. The SPS can be electrically detached from the backplane allowing regulated power supply with current indicators to be attached for troubleshooting and test.

The switching power supply is powered with 110 VAC 60 Hz. The power supply may allow a 220 VAC 50 Hz feed (check your SPS specification).

The DSLAM cards derive supply voltages from the cPCI backplane through the J1/P1 connector only. Core Cards require +5 V and 3.3 V rails. The WAN Card and Line Card require only +5 V. Both cards use on-board linear regulators to get +3.3 V rail. The host CPU card derives power from the cPCI backplane and needs +3.3 V, +5 V, and +12 V. All three rails are fed from the DSLAM shelf SPS.

The LVDS-backplane may have an optional +5 V and 3.3 V screw terminal as required by the application.

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9. SOFTWARE

9.1. Drivers for the VORTEX chipset

PMC-Sierra provides, on request, drivers for each chip and a meta-driver for the VORTEX chipset.

A software user guide PMC-1991216 "VORTEX Chipset Driver Design Specification" is available. Document describes the features and functionality provided by the chipset driver, the software architecture, and the external interfaces of the chipset driver software. The document also provides limited guidance, how the chipset driver can be ported to a different platform.

The VORTEX Chipset Driver is optimized for VxWorks. PMC-Sierra does not support metadriver for any other operating system.

9.2. Microprocessor Firmware

The WAN Card and Line Card have one-time programmable ROM installed into socket.

9.3. Programmable Logic Devices

The WAN Card and Line Card have one-time programmable PALs installed into socket.

The Core Card has permanently soldered an in-circuit erasable/programmable CPLD.

PMC-Sierra provides a soft copy of JEDEC files for the external programmer or VHDL text files for programmable devices.

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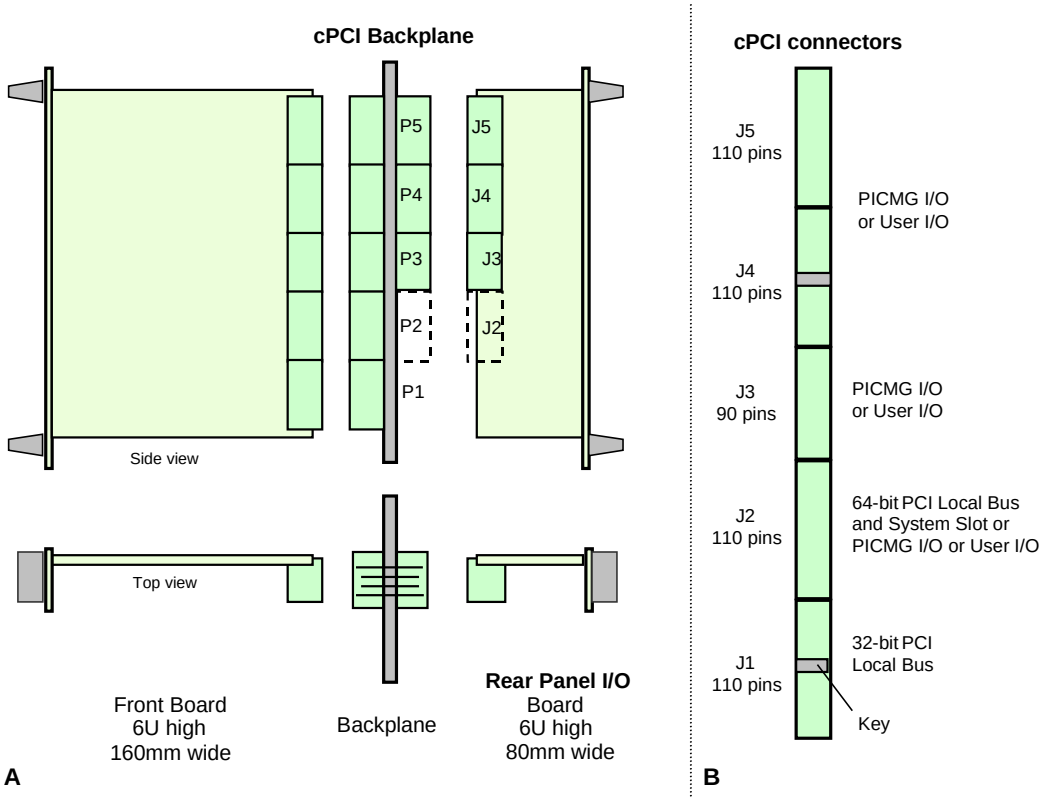
10. APPENDIX – A: REAR PANEL I/O

Rear panel I/O provides the option for board connectivity without complicating the front panels of the DSLAM cards. The I/O connectors can be placed on a passive rear card allowing quick access to the silicone-loaded front card, which reduces service time and eliminates cable reconnection errors. The I/O card is about half the width of the front one.

The rear panel I/O is one of the most important features of the cPCI type backplanes and shelves.

Figure 29 shows a rear panel I/O concept that consists of a side view and a cross section of a backplane.

Figure 29. Rear Panel I/O



The cPCI connectors, port assignment, and pin counts are shown above.

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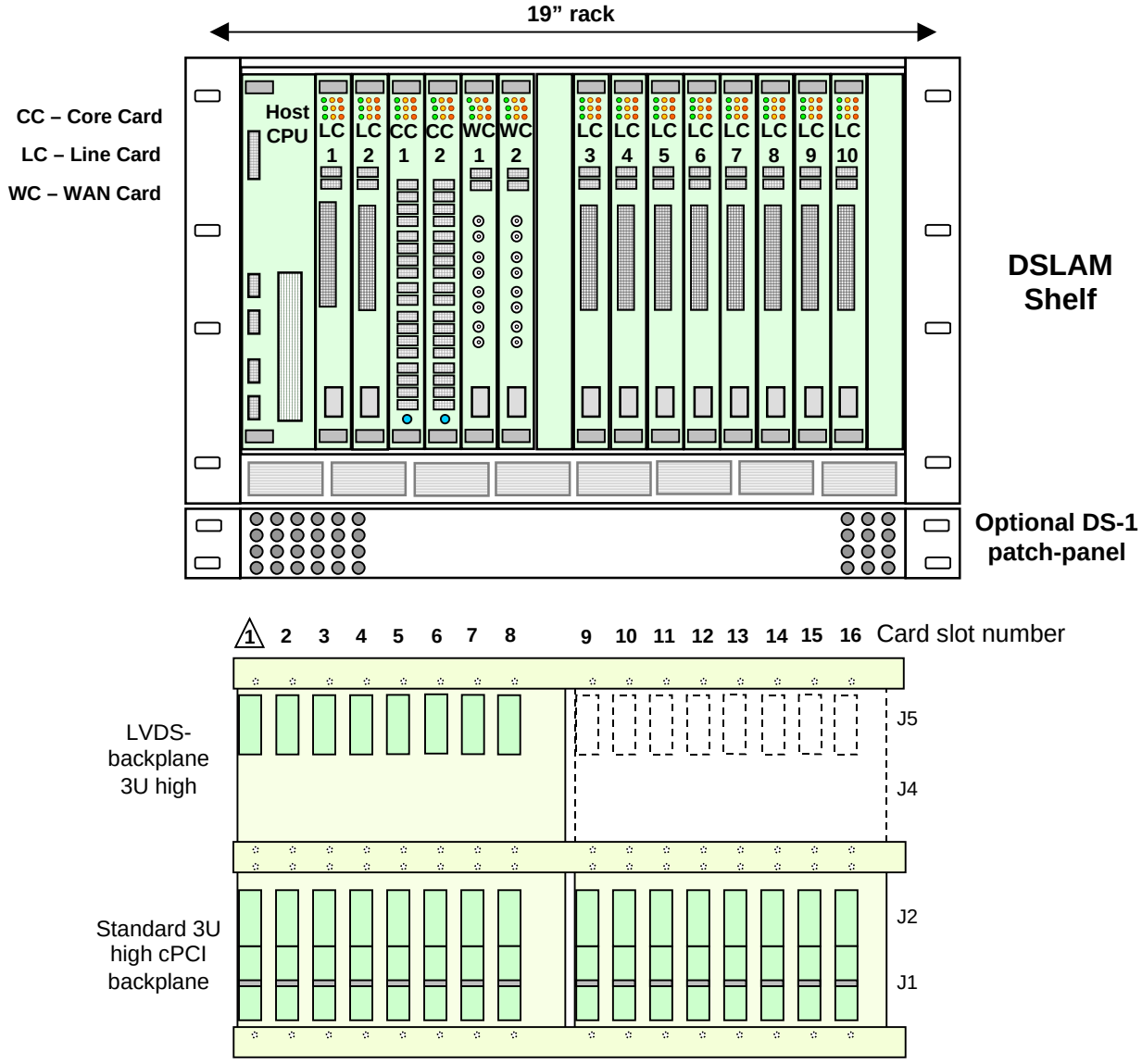
11. APPENDIX– B: DSLAM DUAL-BACKPLANE SHELF

This section presents an easy way to enlarge the DSLAM system based on the cards built for this DSLAM Reference Design. However, this Reference Design *does not* support the 19-inch, rack-mounted shelf.

11.1. DSLAM Demonstration Shelf

A demonstration shelf can be assembled with two cPCI 3U high backplanes and a single LVDS-backplane. Figure 30shows the demonstration shelf.

Figure 30. Optional Demonstration DSLAM Shelf



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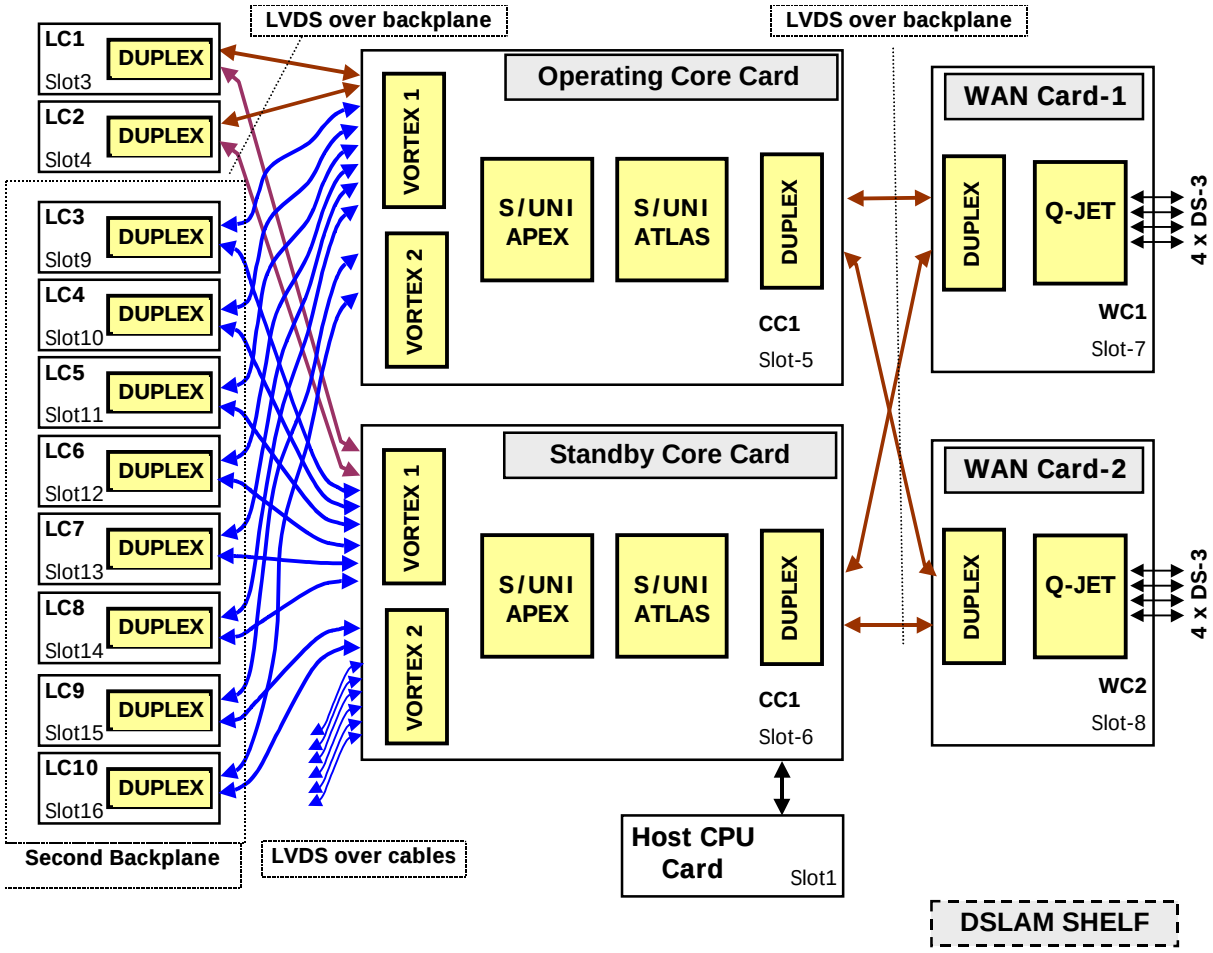
The dual-backplane_single-shelf configuration is based on the single backplane DSLAM shelf described in the previous sections. The difference is basically in the quantity of cards and LVDS cables. Both shelves are controlled from a single host CPU. The dual-backplane shelf configuration supports up to 176 DS-1 loops. A larger system can be built with two dual-backplane shelves that use all 16 LVDS interfaces on both the S/UNI-VORTEX multiplexers that are mounted on the Core Card.

A forced air flow cooling system is recommended with a fully populated or partially populated shelf, due to an enclosed construction that obstructs air flow.

11.2. Example Dual Backplane Shelf Connection Diagram

Figure 31 shows an example of a dual backplane on a single shelf Reference Design, also depicting the major components and connections.

Figure 31. Dual Backplane Shelf Connection Diagram



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The dual backplane DSLAM shelf assembly, shown above (and in Figure 31), consists of the following entities:

- DSLAM Shelf with one LVDS-backplane and two 3U high cPCI backplanes
- Two Core Cards,
- Ten Line Cards,
- Two WAN Cards
- A host CPU
- LVDS cabling
- Optional DS-1 patch-panel

The main purpose of the dual shelf is to demonstrate higher bandwidth, LVDS over cables, and the ability of Core Cards to control Line Cards over the communication channels. Both Core Cards have a mirrored software setup at to allow quick switching at any given point in time.

NOTE: The DSLAM Reference Design does not support the Inband Communication Channel.

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12. GLOSSARY

ADSL	Asymmetric Digital Subscriber Line
ATM	Asynchronous Transfer Mode
ATU-C	Central Office ADSL transceiver
ATU-R	Remote ADSL transceiver
DSLAM	Digital Subscriber Line Access Multiplexer
ICC	Inband Communication Channel
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signaling
PCB	Printed Circuit Board
POTS	Plain Old Telephony System
SONET	Synchronous Optical NETwork
S/UNI	SATURN User Network Interface
Telco	Telephone Company, Telecommunication Company
VCC	Virtual Connection connection
VPC	Virtual Path connection

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