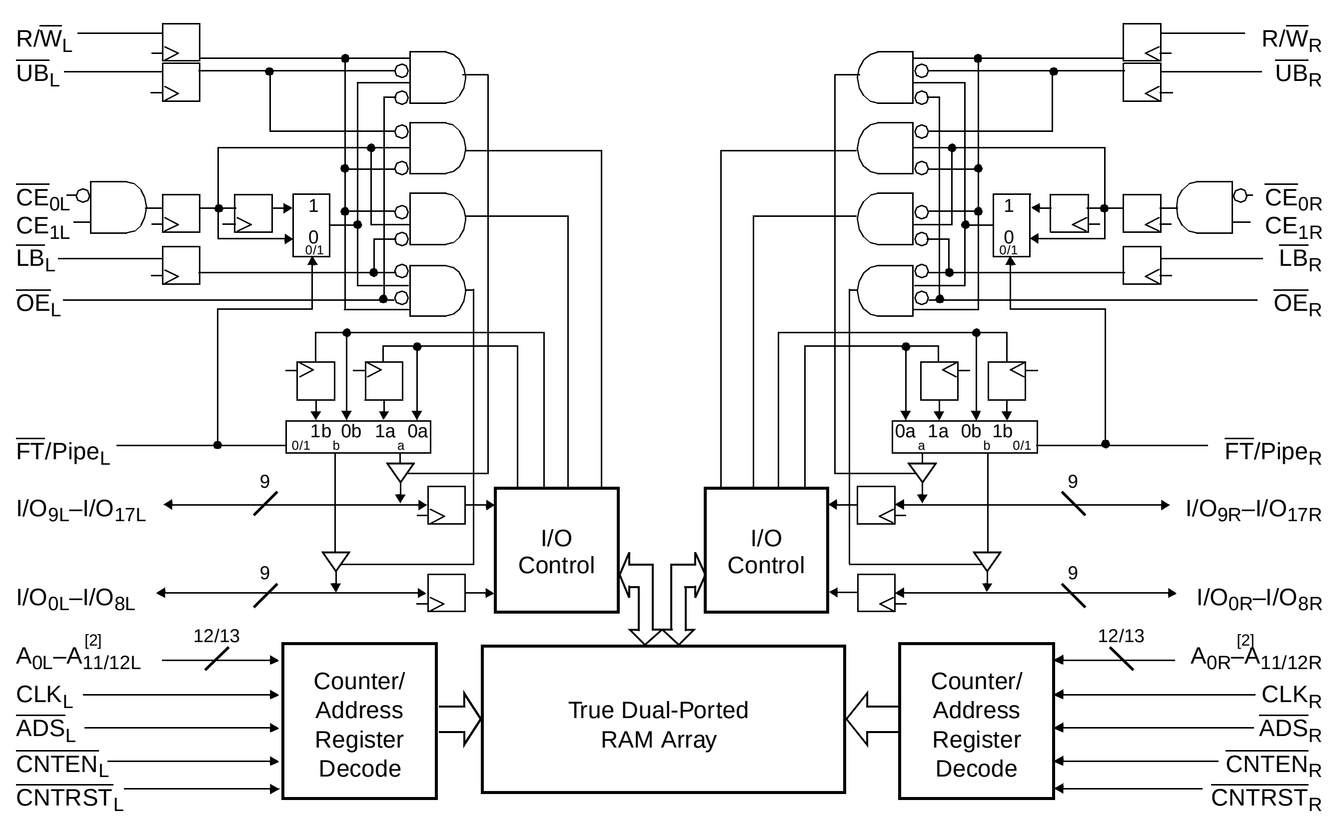
4K/8K x 18 Synchronous Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- Two Flow-Through/Pipelined devices
  - — 4K x 18 organization (CY7C09349)
  - — 8K x 18 organization (CY7C09359)
- Three Modes
  - — Flow-Through
  - — Pipelined
  - — Burst
- Pipelined output mode on both ports allows fast 100-MHz cycle time
- 0.35-micron CMOS for optimum speed/power
- High-speed clock to data access 6.5[1]/7.5/9/12 ns (max.)
- Low operating power
  - — Active = 200 mA (typical)
  - — Standby = 0.05 mA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
  - — Shorten cycle times
  - — Minimize bus noise
  - — Supported in Flow-Through and Pipelined modes
- Dual Chip enables for easy depth expansion
- Upper and lower byte controls for bus matching
- Automatic power-down
- Commercial and Industrial temperature ranges
- Available in 100-pin TQFP

Logic Block Diagram



Notes:

1. See page 6 for Load Conditions.
2. A_0–A_{11} for 4K; A_0–A_{12} for 8K devices.

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Functional Description

The CY7C09349 and CY7C09359 are high-speed synchronous CMOS 4K and 8K x 18 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.[3] Registers on control, address, and data lines allow for minimal set-up and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid t_{CD2} = 6.5 ns[1] (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available t_{CD1} = 15 ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the $\overline{FT}$/Pipe pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE}_0$ or LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables allows easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with $\overline{CE}_0$ LOW and CE_1 HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe ($\overline{ADS}$). When the port's Count Enable ($\overline{CNTEN}$) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array and will loop back to the start. Counter Reset ($\overline{CNTRST}$) is used to reset the burst counter.

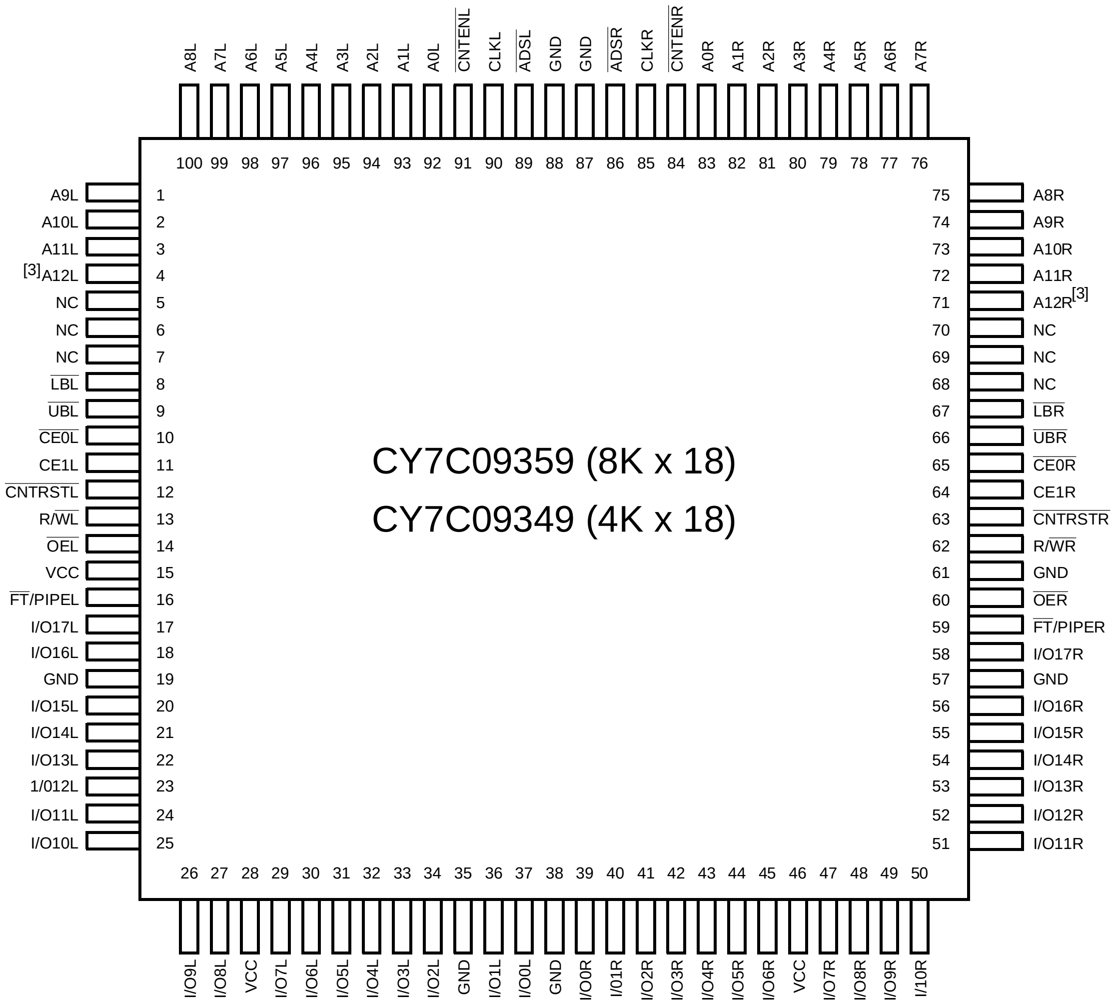
All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

Note:

3. When simultaneously writing to the same location, final value cannot be determined.

Pin Configuration

100-Pin TQFP (Top View)



Selection Guide

	CY7C09349 CY7C09359 -6[1]	CY7C09349 CY7C09359 -7	CY7C09349 CY7C09359 -9	CY7C09349 CY7C09359 -12
f_{MAX2} (MHz) (Pipelined)	100	83	67	50
Max. Access Time (ns) (Clock to Data, Pipelined)	6.5	7.5	9	12
Typical Operating Current I_{CC} (mA)	250	235	215	195
Typical Standby Current for I_{SB1} (mA) (Both Ports TTL Level)	45	40	35	30
Typical Standby Current for I_{SB3} (mA) (Both Ports CMOS Level)	0.05	0.05	0.05	0.05

Note:
4. This pin is NC for CY7C09349.

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{12L}	A_{0R}–A_{12R}	Address Inputs (A_0–A_{11} for 4K, A_0–A_{12} for 8K devices).
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW during normal read or write transactions. Asserting this signal LOW also loads the burst address counter with data present on the I/O pins.
$\overline{CE}_{0L}$,CE_{1L}	$\overline{CE}_{0R}$,CE_{1R}	Chip Enable Input. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).
CLK_L	CLK_R	Clock Signal. This input can be free running or strobed. Maximum clock input rate is f_{MAX}.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. $\overline{CNTEN}$ is disabled if $\overline{ADS}$ or $\overline{CNTRST}$ are asserted LOW.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. $\overline{CNTRST}$ is not disabled by asserting $\overline{ADS}$ or $\overline{CNTEN}$.
I/O_{0L}–I/O_{17L}	I/O_{0R}–I/O_{17R}	Data Bus Input/Output (I/O_0–I/O_{15} for x16 devices).
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select Input. Asserting this signal LOW enables read and write operations to the lower byte (I/O_0–I/O_8 for x18, I/O_0–I/O_7 for x16) of the memory array. For read operations both the $\overline{LB}$ and $\overline{OE}$ signals must be asserted to drive output data on the lower byte of the data pins.
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select Input. Same function as $\overline{LB}$, but to the upper byte ($I/O_{8/9L}$–$I/O_{15/17L}$).
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable Input. This signal must be asserted LOW to enable the I/O data pins during read operations.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
GND		Ground Input.
NC		No Connect.
V_{CC}		Power Input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied ..–55°C to +125°C

Supply Voltage to Ground Potential .... –0.3V to +7.0V

DC Voltage Applied to
Outputs in High Z State .... –0.5V to +7.0V

DC Input Voltage... –0.5V to +7.0V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage .... >2001V

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range

Parameter	Description		CY7C09349 CY7C09359												Unit
			-6[1]			-7			-9			-12			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{CC} = Min., I_{OH} = –4.0 mA)		2.4			2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{CC} = Min., I_{OH} = +4.0 mA)				0.4			0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.2			2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	–10		10	µA
I_{CC}	Operating Current (V_{CC} = Max, I_{OUT} = 0 mA) Outputs Disabled	Com'l.		250	450		235	420		215	360		195	300	mA
		Ind.					260	445		240	410		225	375	mA
I_{SB1}	Standby Current (Both Ports TTL Level)[5] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		45	115		40	105		35	95		30	85	mA
		Ind.					55	120		50	110		45	100	mA
I_{SB2}	Standby Current (One Port TTL Level)[5] $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		175	235		160	220		145	205		125	190	mA
		Ind.					175	235		160	220		140	205	mA
I_{SB3}	Standby Current (Both Ports CMOS Level)[5] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2V, f = 0	Com'l.		0.05	0.5		0.05	0.5		0.05	0.5		0.05	0.5	mA
		Ind.					0.05	0.5		0.05	0.5		0.05	0.5	mA
I_{SB4}	Standby Current (One Port CMOS Level)[5] $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		160	200		145	185		130	170		110	150	mA
		Ind.					160	200		145	185		125	165	mA

Shaded areas contain advance information.

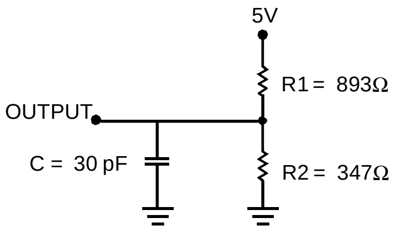
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

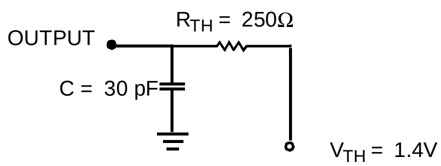
Note:

5. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).

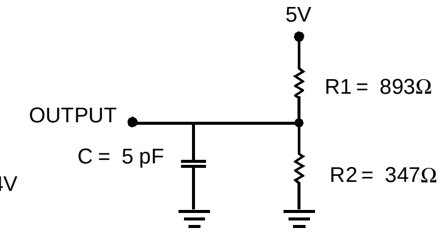
AC Test Loads



(a) Normal Load (Load 1)

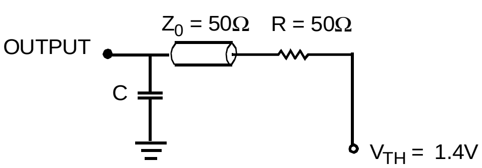


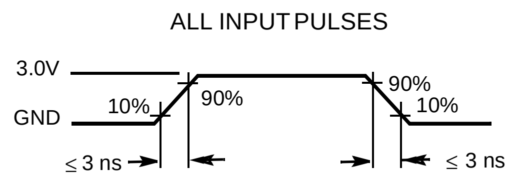
(b) Thévenin Equivalent (Load 1)



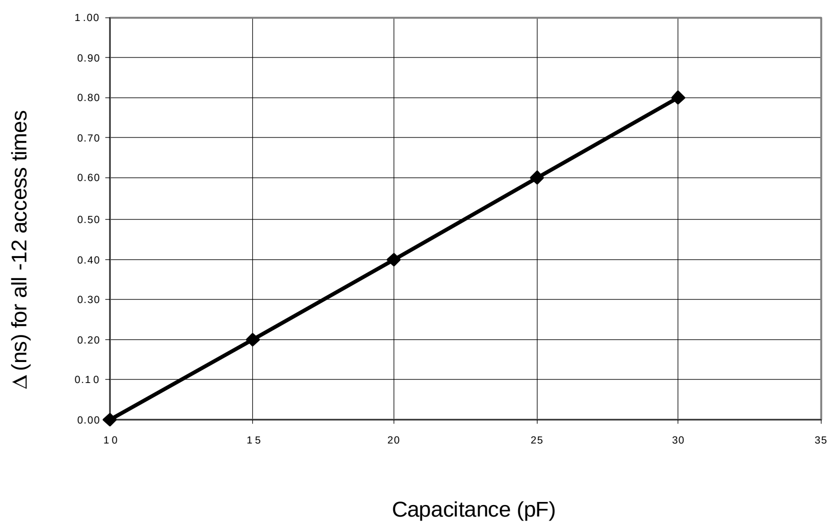
(c) Three-State Delay (Load 2)
(Used for t_{CKLZ}, t_{OLZ}, & t_{OHZ} including scope and jig)

AC Test Loads (Applicable to -6 only)[6]





(a) Load 1 (-6 only)



(b) Load Derating Curve

Note:
6. Test Conditions: C = 10 pF.

Switching Characteristics Over the Operating Range

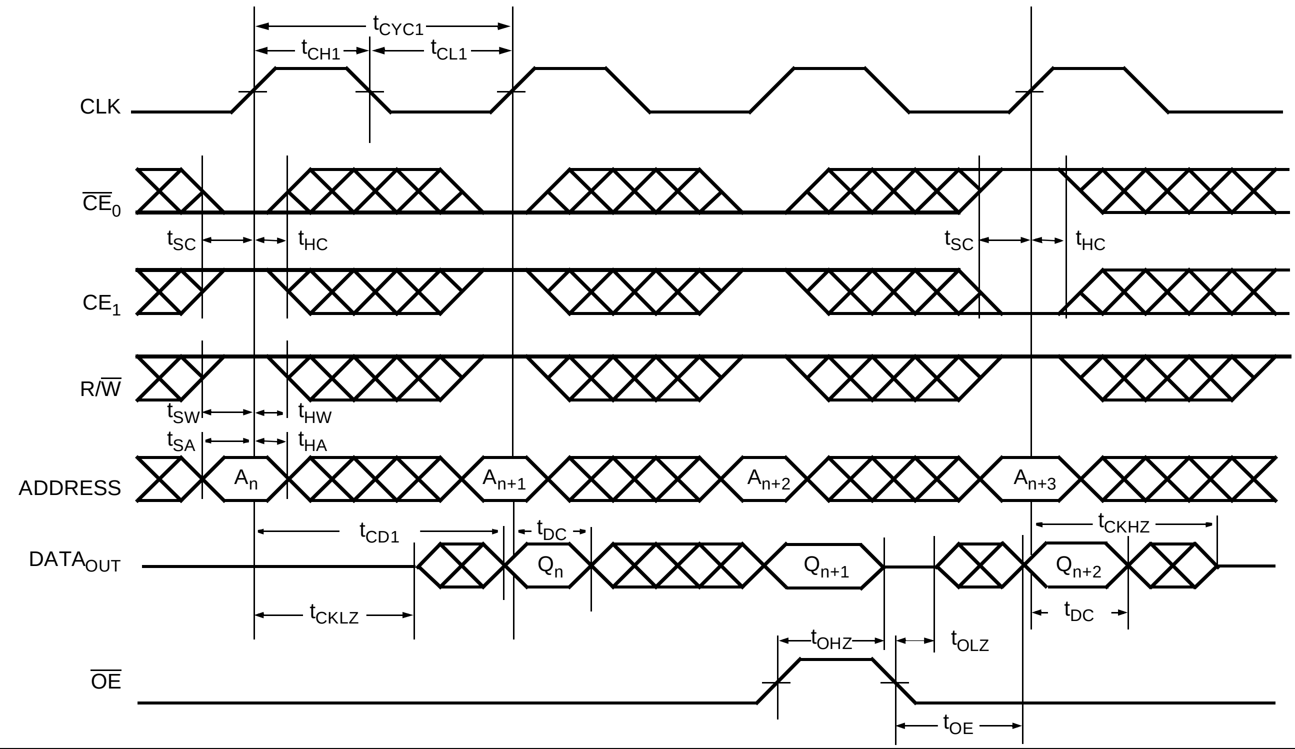
Parameter	Description	CY7C09349 CY7C09359								Unit
		-6[1]		-7		-9		-12		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX1}	f_{Max} Flow-Through		53		45		40		33	MHz
f_{MAX2}	f_{Max} Pipelined		100		83		67		50	MHz
t_{CYC1}	Clock Cycle Time - Flow-Through	19		22		25		30		ns
t_{CYC2}	Clock Cycle Time - Pipelined	10		12		15		20		ns
t_{CH1}	Clock HIGH Time - Flow-Through	6.5		7.5		12		12		ns
t_{CL1}	Clock LOW Time - Flow-Through	6.5		7.5		12		12		ns
t_{CH2}	Clock HIGH Time - Pipelined	4		5		6		8		ns
t_{CL2}	Clock LOW Time - Pipelined	4		5		6		8		ns
t_R	Clock Rise Time		3		3		3		3	ns
t_F	Clock Fall Time		3		3		3		3	ns
t_{SA}	Address Set-up Time	3.5		4		4		4		ns
t_{HA}	Address Hold Time	0		0		1		1		ns
t_{SC}	Chip Enable Set-up Time	3.5		4		4		4		ns
t_{HC}	Chip Enable Hold Time	0		0		1		1		ns
t_{SW}	R/$\overline{\text{W}}$ Set-up Time	3.5		4		4		4		ns
t_{HW}	R/$\overline{\text{W}}$ Hold Time	0		0		1		1		ns
t_{SD}	Input Data Set-up Time	3.5		4		4		4		ns
t_{HD}	Input Data Hold Time	0		0		1		1		ns
t_{SAD}	$\overline{\text{ADS}}$ Set-up Time	3.5		4		4		4		ns
t_{HAD}	$\overline{\text{ADS}}$ Hold Time	0		0		1		1		ns
t_{SCN}	$\overline{\text{CNTEN}}$ Set-up Time	3.5		4		4		4		ns
t_{HCN}	$\overline{\text{CNTEN}}$ Hold Time	0		0		1		1		ns
t_{SRST}	$\overline{\text{CNTRST}}$ Set-up Time	3.5		4		4		4		ns
t_{HRST}	$\overline{\text{CNTRST}}$ Hold Time	0		0		1		1		ns
t_{OE}	Output Enable to Data Valid		8		9		10		12	ns
t_{OLZ}[7]	$\overline{\text{OE}}$ to Low Z	2		2		2		2		ns
t_{OHZ}[7]	$\overline{\text{OE}}$ to High Z	1	7	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid - Flow-Through		15		18		20		25	ns
t_{CD2}	Clock to Data Valid - Pipelined		6.5		7.5		9		12	ns
t_{DC}	Data Output Hold After Clock HIGH	2		2		2		2		ns
t_{CKHZ}	Clock HIGH to Output High Z	2	9	2	9	2	9	2	9	ns
t_{CKLZ}[7]	Clock HIGH to Output Low Z	2		2		2		2		ns
Port to Port Delays										
t_{CWDD}	Write Port Clock HIGH to Read Data Delay		30		35		40		40	ns
t_{CCS}	Clock to Clock Set-up Time		9		10		15		15	ns

Notes:

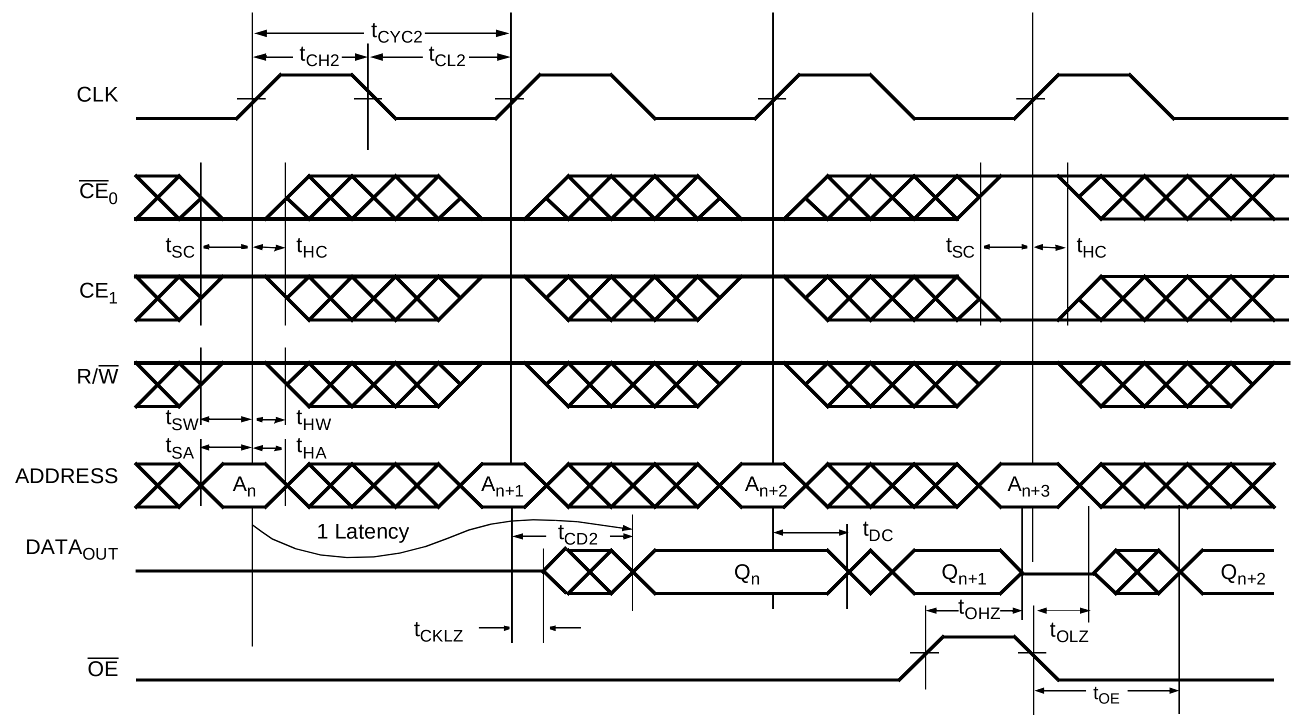
7. Test conditions used are Load 2.

Switching Waveforms

Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE = V_{IL})[8, 9, 10, 11]



Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = V_{IH})[8, 9, 10, 11]

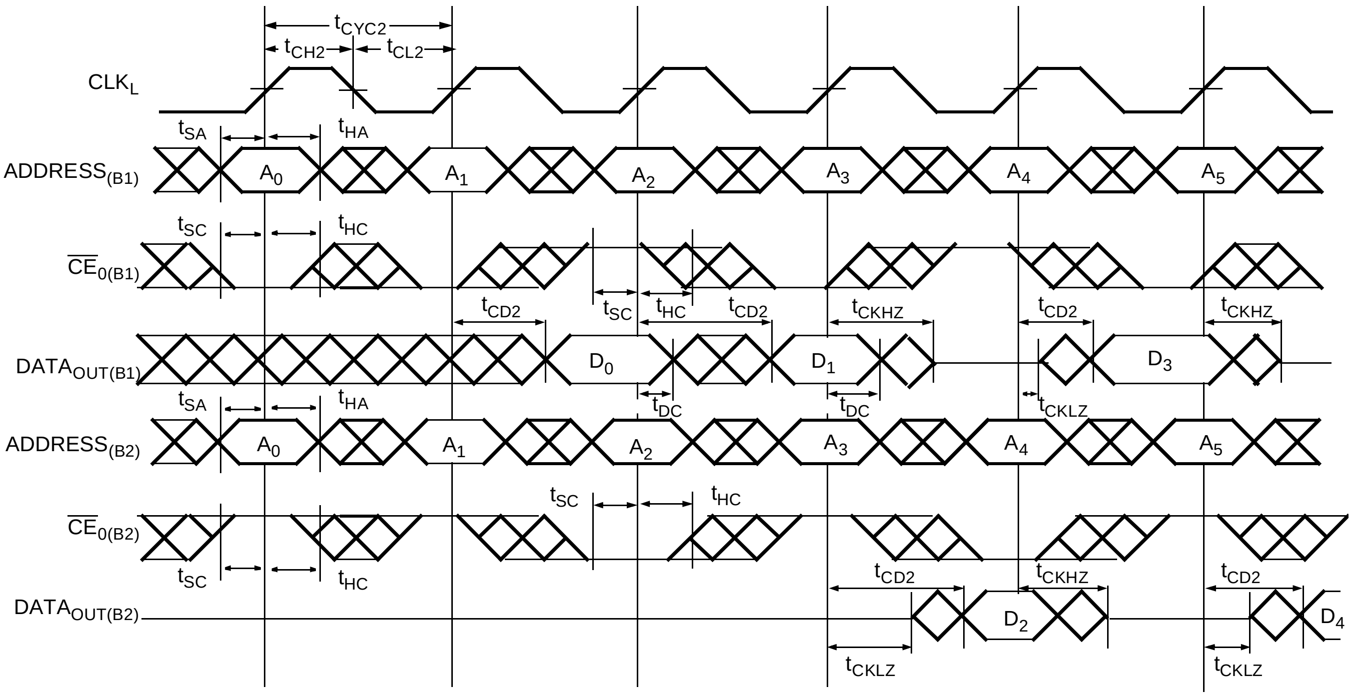


Notes:

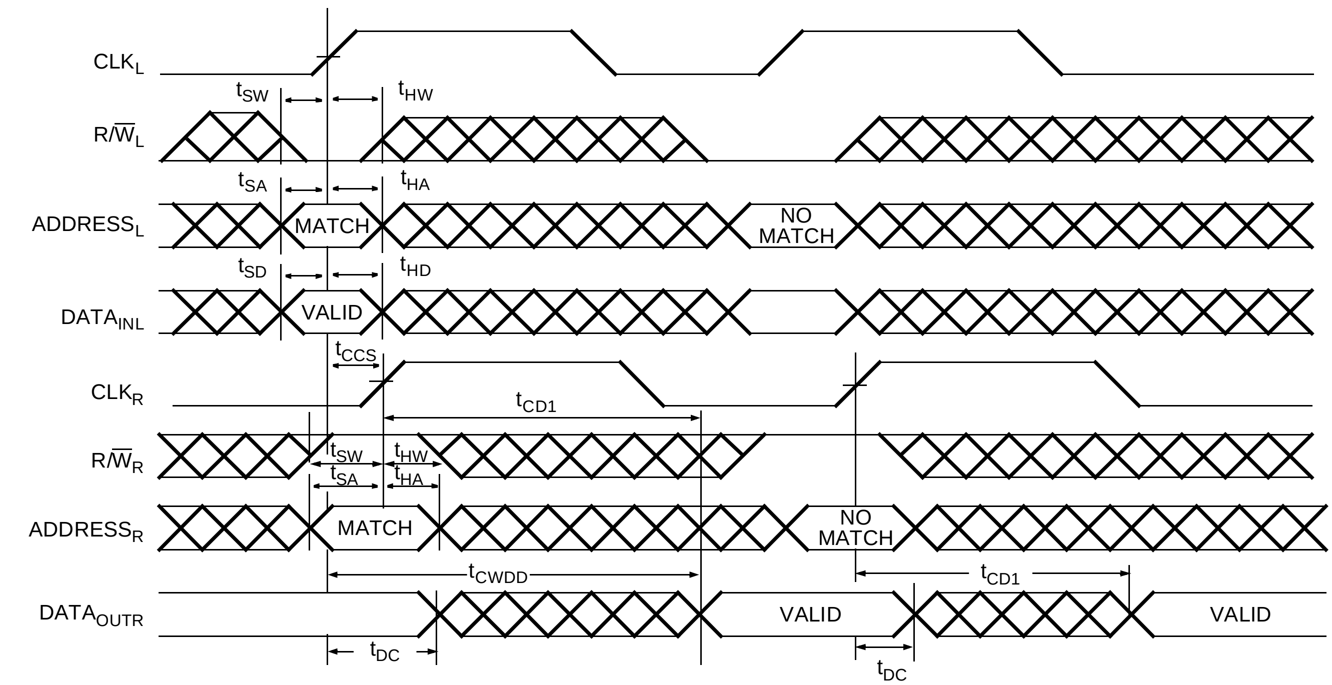
8. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
9. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
10. The output is disabled (high-impedance state) by $\overline{CE}_0$=V_{IH} or CE_1 = V_{IL} following the next rising edge of the clock.
11. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Bank Select Pipelined Read[12, 13]



Left Port Write to Flow-Through Right Port Read[14, 15, 16, 17]

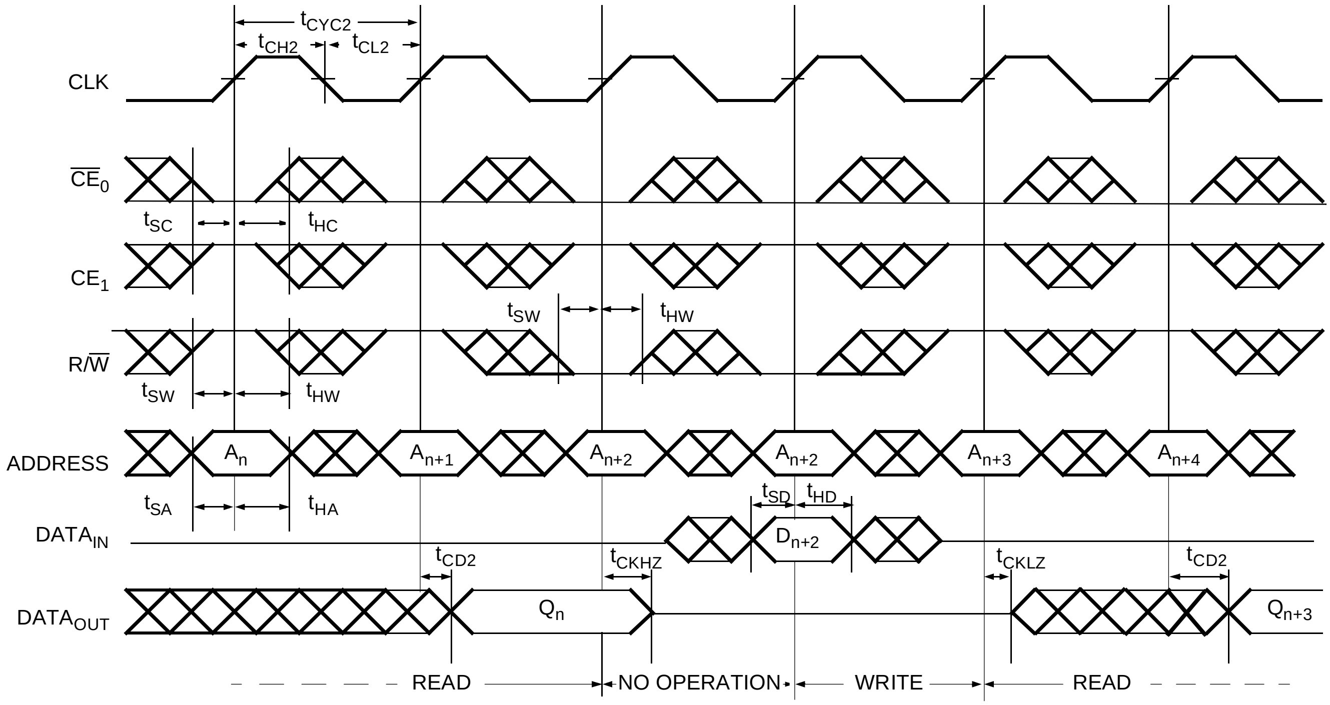


Notes:

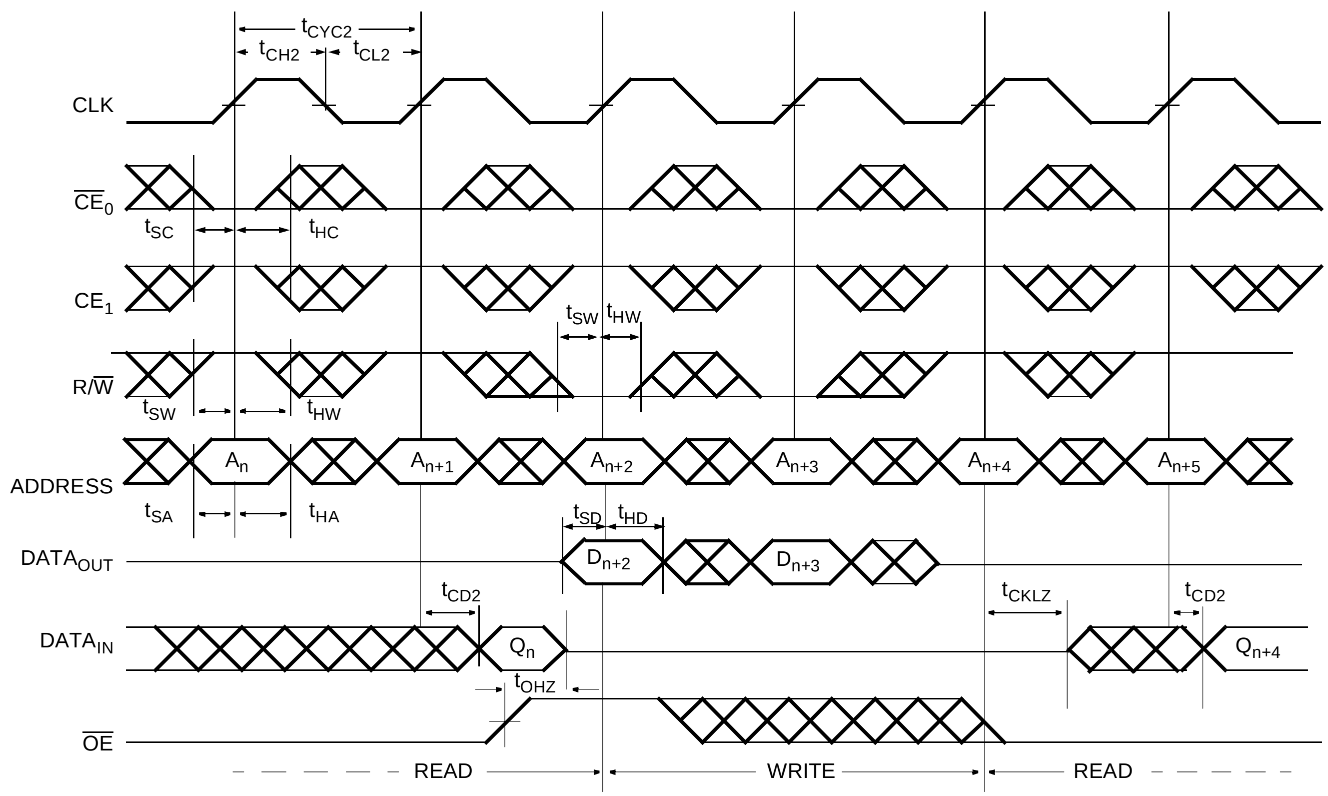
12. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
13. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$ and $\overline{ADS} = V_{IL}$; $\overline{CE}_{1(B1)}$, $CE_{1(B2)}$, $R/\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
14. The same waveforms apply for a right port write to flow-through left port read.
15. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
16. $\overline{OE} = V_{IL}$ for the right port, which is being read from. $\overline{OE} = V_{IH}$ for the left port, which is being written to.
17. It $t_{CCS} \le$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS}>maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

Switching Waveforms (continued)

Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[11, 18, 19, 20]



Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[11, 18, 19, 20]

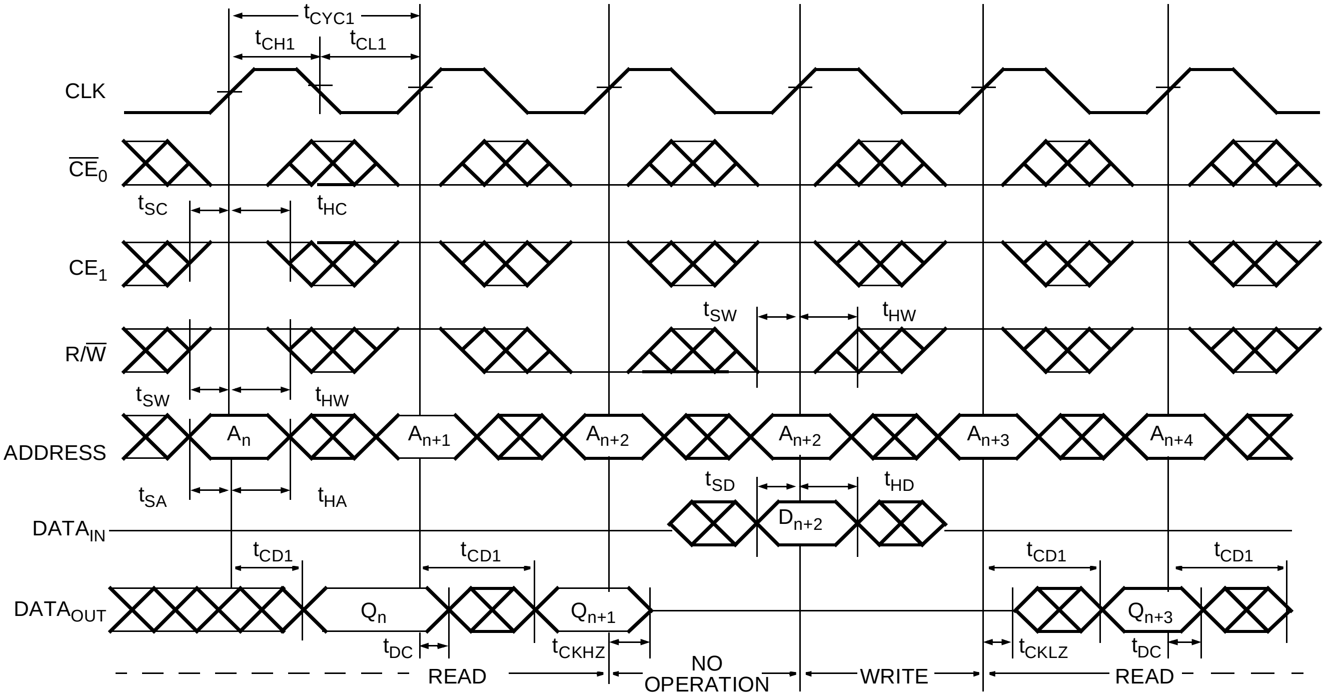


Notes:

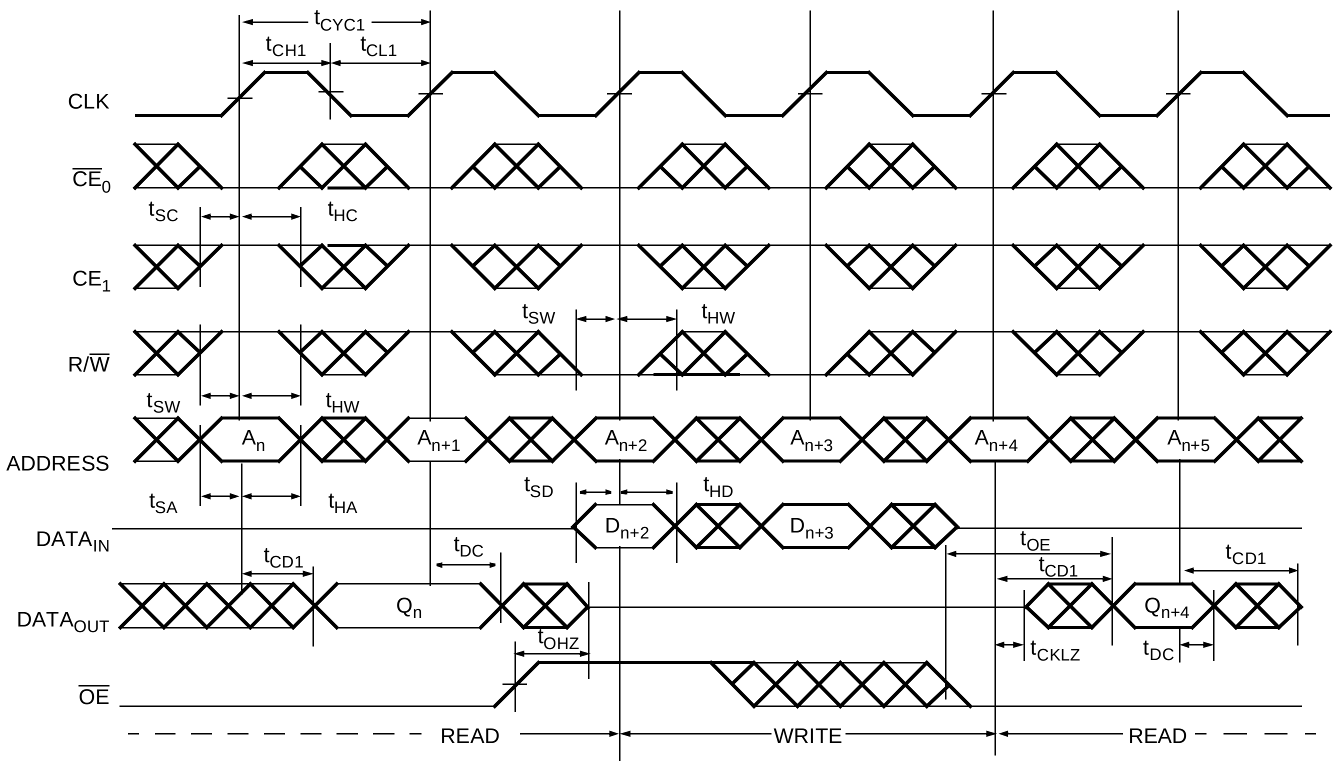
18. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
19. $\overline{CE}_0$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
20. During “No operation,” data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms (continued)

Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)[9, 11, 18, 19]

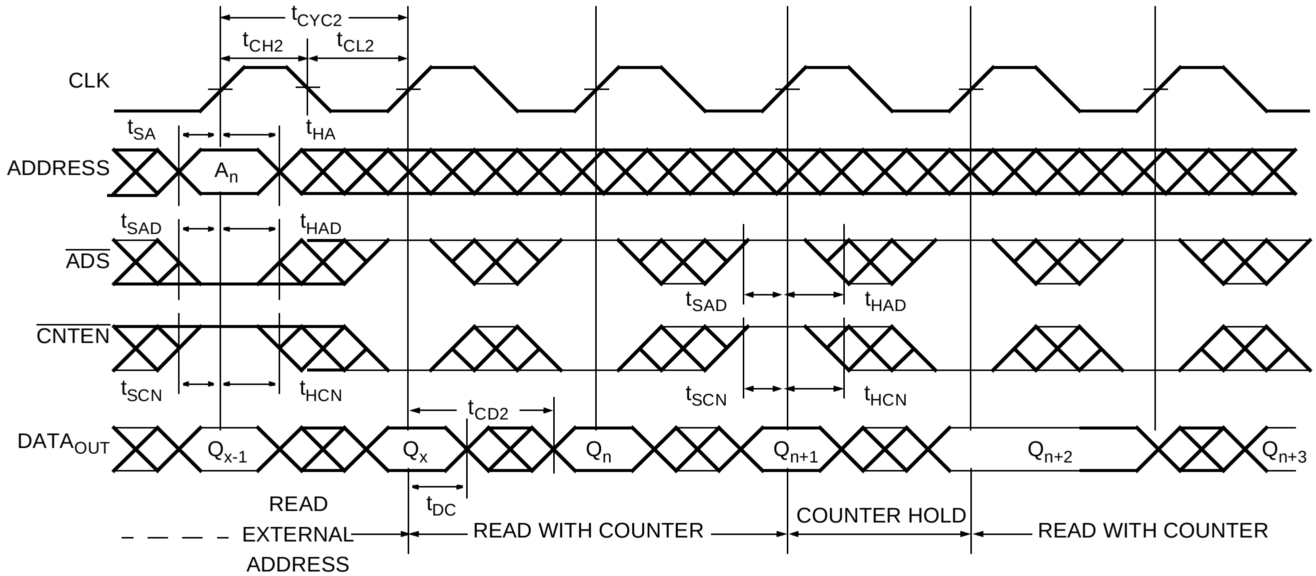


Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)[9, 11, 18, 19]

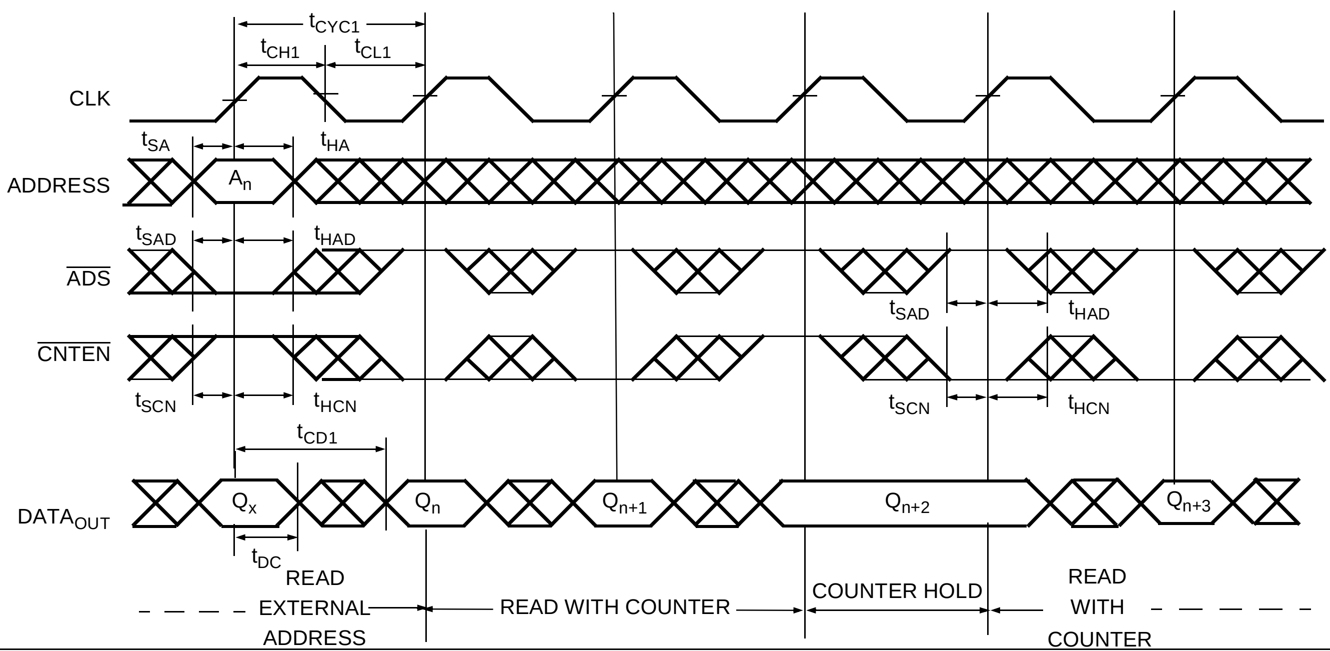


Switching Waveforms (continued)

Pipelined Read with Address Counter Advance[21]



Flow-Through Read with Address Counter Advance[21]

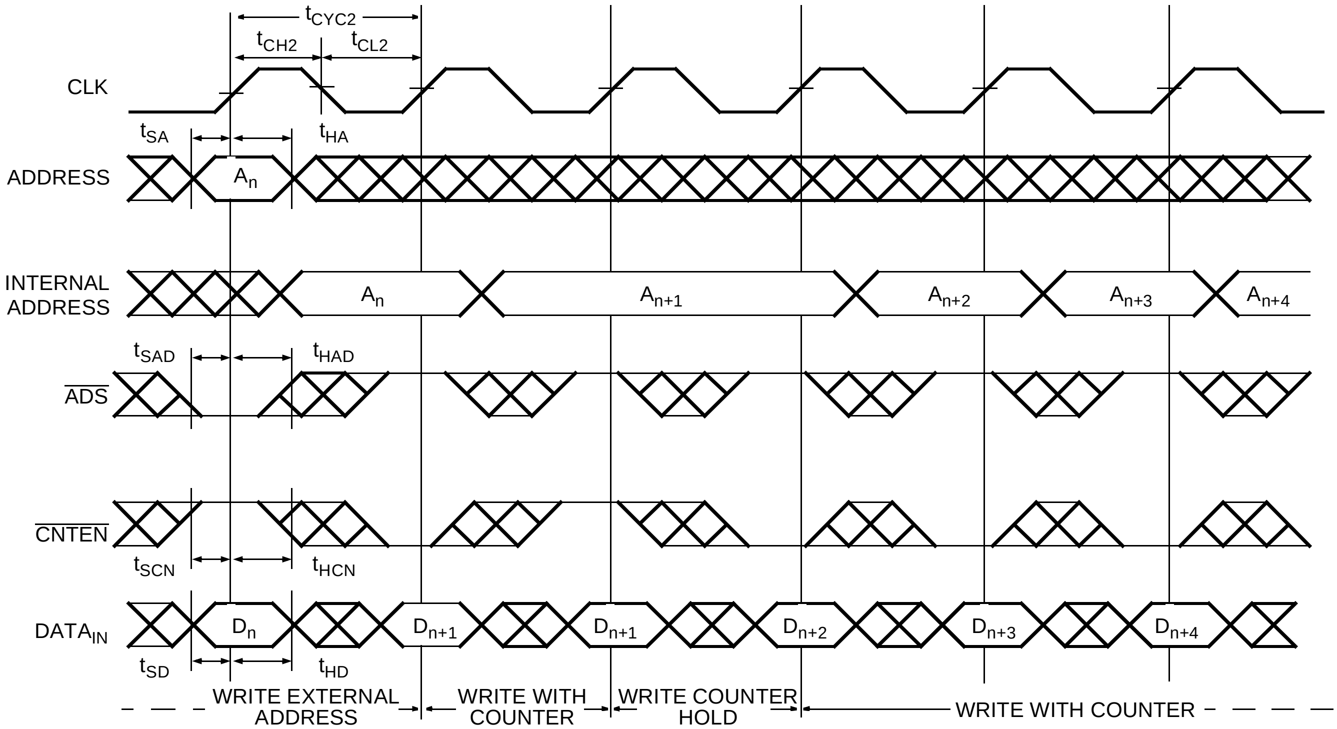


Note:

21. $\overline{CE_0}$ and $\overline{OE}$ = V_{IL}; CE_1, $R/\overline{W}$ and $\overline{CNTRST}$ = V_{IH}.

Switching Waveforms (continued)

Write with Address Counter Advance (Flow-Through or Pipelined Outputs)[22, 23]

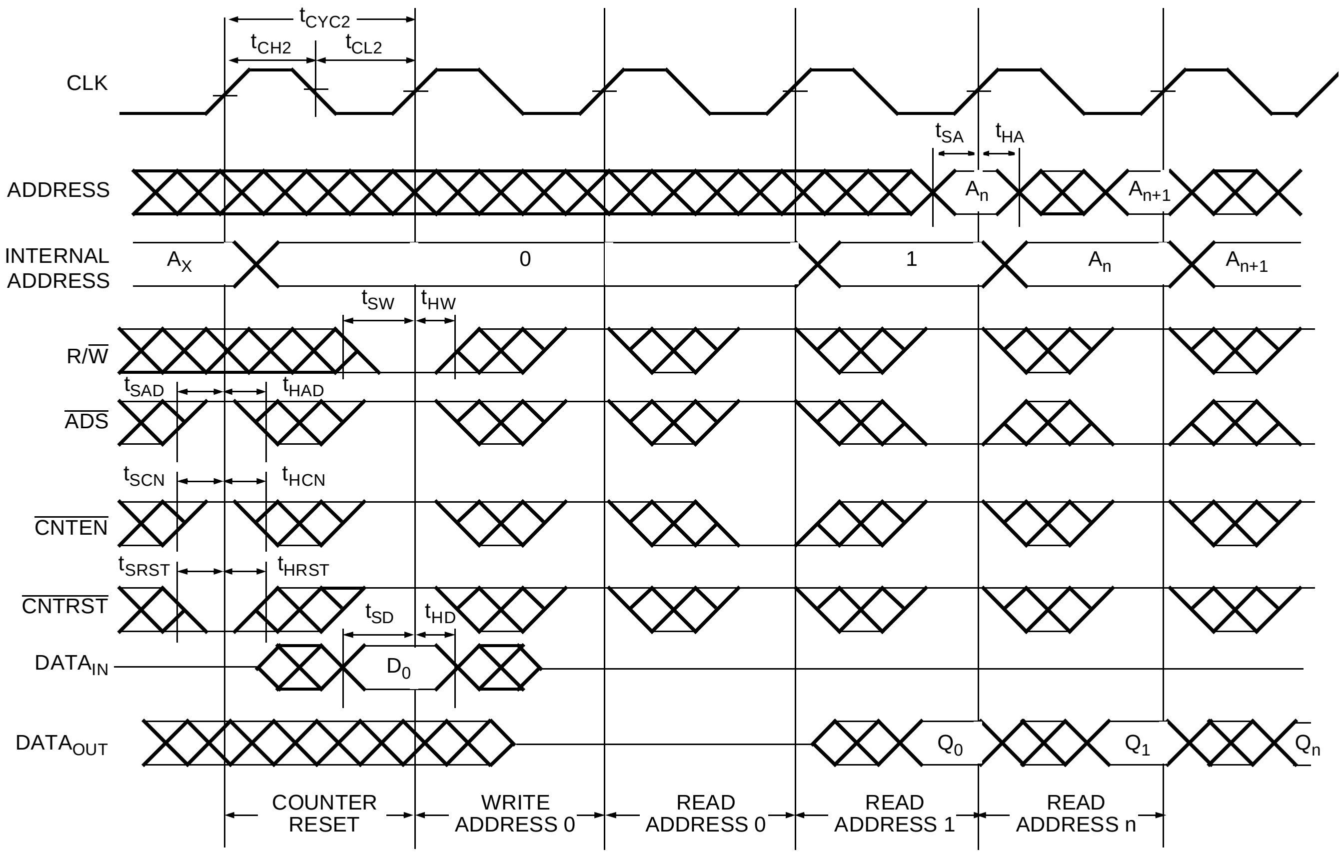


Notes:

22. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
23. The “Internal Address” is equal to the “External Address” when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.

Switching Waveforms (continued)

Counter Reset (Pipelined Outputs)[11, 18, 24, 25]



Notes:

24. $\overline{CE}_0$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}; CE_1 = V_{IH}.
25. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

Read/Write and Enable Operation[26, 27, 28]

Inputs					Outputs	
$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$R/\overline{W}$	$I/O_0–I/O_{17}$	Operation
X		H	X	X	High-Z	Deselected[29]
X		X	L	X	High-Z	Deselected[29]
X		L	H	L	D_{IN}	Write
L		L	H	H	D_{OUT}	Read[29]
H	X	L	H	X	High-Z	Outputs Disabled

Address Counter Control Operation[26,30,31,32]

Address	Previous Address	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O	Mode	Operation
X	X		X	X	L	$D_{out(0)}$	Reset	Counter Reset to Address 0
A_n	X		L	X	H	$D_{out(n)}$	Load	Address Load into Counter
X	A_n		H	H	H	$D_{out(n)}$	Hold	External Address Blocked—Counter Disabled
X	A_n		H	L	H	$D_{out(n+1)}$	Increment	Counter Enabled—Internal Address Generation

Notes:
26. "X" = "don't care," "H" = V_{IH}, "L" = V_{IL}.
27. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = "don't care."
28. $\overline{OE}$ is an asynchronous input signal.
29. When $\overline{CE}$ changes state in the pipelined mode, deselection and read happen in the following clock cycle.
30. $\overline{CE}_0$ and $\overline{OE}$ = V_{IL}; CE_1 and $R/\overline{W}$ = V_{IH}.
31. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
32. Counter operation is independent of $\overline{CE}_0$ and CE_1.

Ordering Information

4K x18 Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09349-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
7.5	CY7C09349-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09349-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
9	CY7C09349-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09349-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09349-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09349-12AI	A100	100-Pin Thin Quad Flat Pack	Industrial

8K x18 Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5[1]	CY7C09359-6AC	A100	100-Pin Thin Quad Flat Pack	Commercial
7.5	CY7C09359-7AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09359-7AI	A100	100-Pin Thin Quad Flat Pack	Industrial
9	CY7C09359-9AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09359-9AI	A100	100-Pin Thin Quad Flat Pack	Industrial
12	CY7C09359-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C09359-12AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Shaded areas contain advance information.

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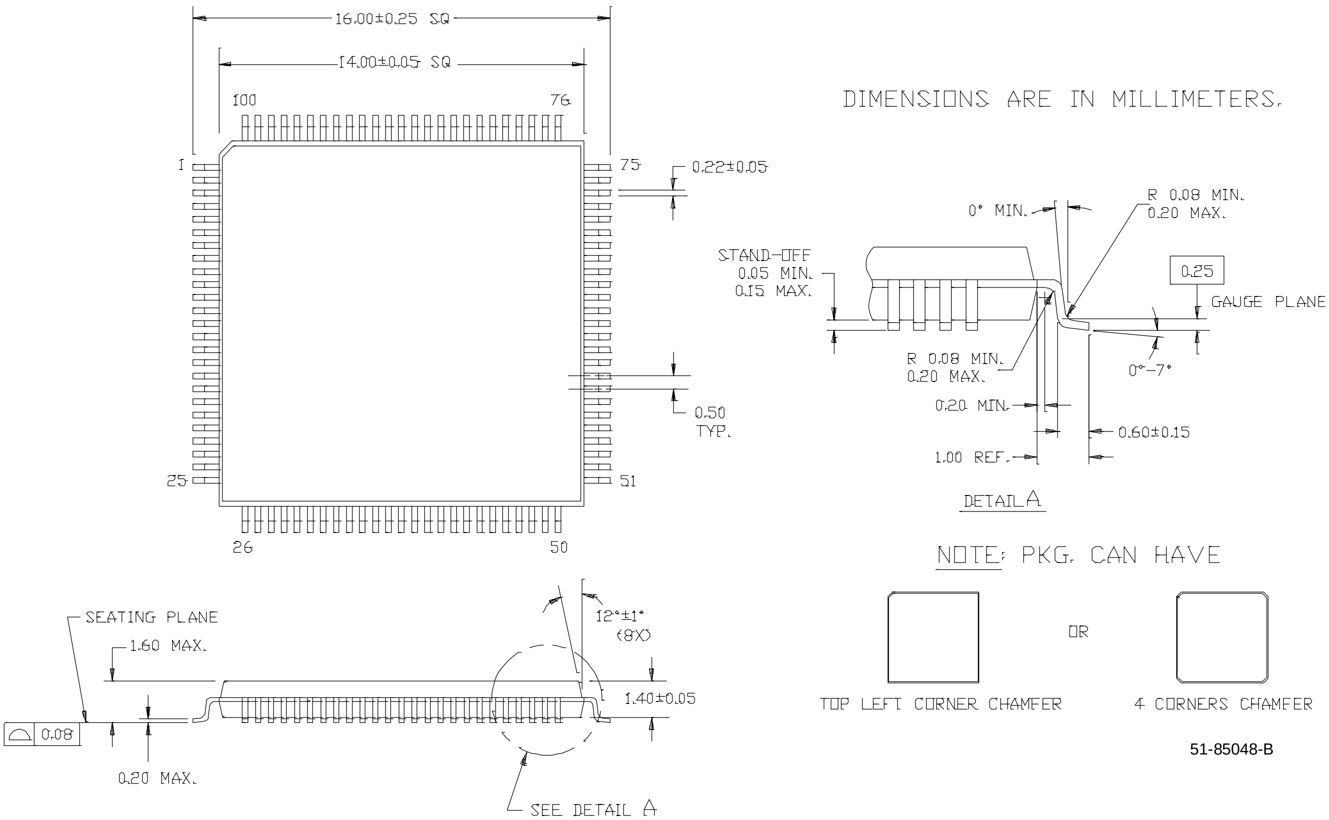
Package Diagram

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



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CY7C036 Dual Port Design Consideration – Data Sheet Addendum

This design consideration applies to the Internal Power-On-Reset (POR) circuit used on the CY7C036 and its derivatives listed below.

Power supply ramp—The devices will function properly and meet all data sheet specifications if the power supply ramp rate is greater than 100 ns. If ramp is less than 100 ns, you may see a non-destructive failure in which the device will not respond to changes in address or clock, but the I/Os will respond to the output enable.

Applications consideration—If the power supply ramps in less than 100 ns, a small resistor (20–50Ω), a large capacitor, or an RC network can be connected at the output of the power supply to ground. The addition of a resistor will help clean up the power lines, while the capacitor will slow down the ramp rate without the loss of any power. Contact your local Cypress FAE for assistance as needed.

Troubleshooting—If a problem occurs with the part, power down the device to ground and then power up again at slower ramp rate (greater than 100 ns) in order to confirm that the problem might be due to the POR circuit. If the dual-port functions properly once the ramp rate is slowed to 100 ns or greater, then the POR circuit is at fault.

Applicable devices—All speed/package/temperature combinations of the following:

- CY7C09349
- CY7C09359

Cypress design change—Cypress design team has identified the root cause. A permanent circuit change and die revision will be available beginning in October and will be identified by the letter “A” in the part number.