TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 16-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55W800XB is a 8,388,608-bit static random access memory (SRAM) organized as 524,288 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.3 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.5 μA standby current (at V_{DD} = 3 V, Ta = 25°C, maximum) when chip enable ($\overline{CE1}$) is asserted high or (CE2) is asserted low. There are three control inputs. $\overline{CE1}$ and CE2 are used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of −40° to 85°C, the TC55W800XB can be used in environments exhibiting extreme temperature conditions. The TC55W800XB is available in a plastic 48-ball BGA.

FEATURES

- Low-power dissipation
  Operating: 9.9 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.3 V
- Power down features using $\overline{CE1}$ and CE2
- Data retention supply voltage of 1.5 to 3.3 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of −40° to 85°C
- Standby Current (maximum):

3.3 V	10 μA
3.0 V	5 μA

- Access Times (maximum at V_{DD} = 2.7 to 3.3 V):

	TC55W800XB	
	7	8
Access Time	70 ns	85 ns
$\overline{CE1}$ Access Time	70 ns	85 ns
CE2 Access Time	70 ns	85 ns
$\overline{OE}$ Access Time	35 ns	45 ns

- Package:
  P-TFBGA48-0811-0.75AZ (Weight: 0.21 g typ)

PIN ASSIGNMENT (TOP VIEW)

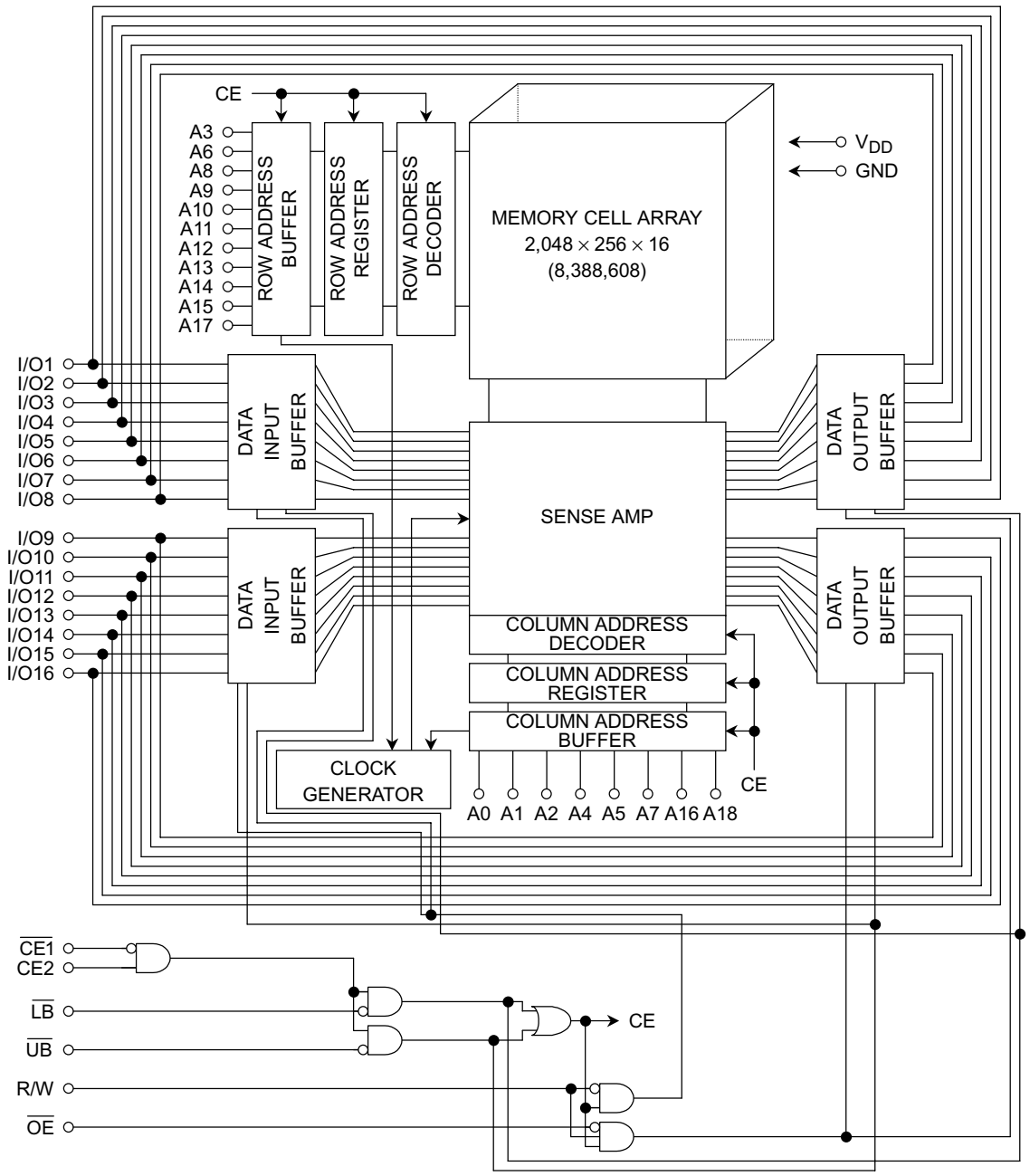
48 PIN BGA

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DD}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	R/W	I/O8
H	A18	A8	A9	A10	A11	NC

PIN NAMES

A0~A18	Address Inputs
$\overline{CE1}$, CE2	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	H	L	H	L	L	Output	Output	I_{DDO}
	L	H	L	H	H	L	High-Z	Output	I_{DDO}
	L	H	L	H	L	H	Output	High-Z	I_{DDO}
Write	L	H	*	L	L	L	Input	Input	I_{DDO}
	L	H	*	L	H	L	High-Z	Input	I_{DDO}
	L	H	*	L	L	H	Input	High-Z	I_{DDO}
Output Deselect	L	H	H	H	*	*	High-Z	High-Z	I_{DDO}
Standby	H	*	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	L	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	*	*	*	H	H	High-Z	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	−0.3~4.2	V
V_{IN}	Input Voltage	−0.3*~4.2	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55~125	°C
T_{opr}	Operating Temperature	−40~85	°C

*: −2.0 V when measured at a pulse width of 25ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = −40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage		2.3	—	3.3	V
V_{IH}	Input High Voltage	V_{DD} = 2.3 V~3.3 V	2.0	—	V_{DD} + 0.3	V
		V_{DD} = 2.7 V~3.3 V	2.2			
V_{IL}	Input Low Voltage		−0.3*	—	V_{DD} × 0.22	V
V_{DH}	Data Retention Supply Voltage		1.5	—	3.3	V

*: −2.0 V when measured at a pulse width of 25ns

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 2.3 to 3.3 V)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{DD}				—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} – 0.5 V				–0.5	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V				2.1	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{LB}$ and $\overline{UB}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V~V_{DD}				—	—	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and $\overline{LB}$ and $\overline{UB}$ = V_{IL} and R/W = V_{IH} and I_{OUT} = 0 mA and Other Input = V_{IH}/V_{IL}		t_{cycle}	min	—	—	50	mA
					1 μs	—	—	10	
I_{DDO2}		$\overline{CE1}$ = 0.2 V and CE2 = V_{DD} – 0.2 V and $\overline{LB}$ and $\overline{UB}$ = 0.2 V, R/W = V_{DD} – 0.2 V and I_{OUT} = 0 mA, Other Input = V_{DD} – 0.2 V/0.2 V		t_{cycle}	min	—	—	45	mA
					1 μs	—	—	5	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{LB}$ and $\overline{UB}$ = V_{IH}				—	—	2	mA
I_{DDS2} (Note)		$\overline{CE1}$ = V_{DD} – 0.2 V or CE2 = 0.2 V or $\overline{LB}$ and $\overline{UB}$ = V_{DD} – 0.2 V, V_{DD} = 1.5 V~3.3 V	V_{DD} = 3.0 V ± 10%	Ta = 25°C		—	—	1	μA
				Ta = –40~85°C		—	—	10	
			V_{DD} = 3.0 V	Ta = 25°C		—	0.05	0.5	
				Ta = –40~40°C		—	—	1	
				Ta = –40~85°C		—	—	5	

Note • In standby mode with $\overline{CE1}$ ≥ V_{DD} – 0.2 V, these limits are assured for the condition CE2 ≥ V_{DD} – 0.2 V or CE2 ≤ 0.2 V.

• In standby mode with $\overline{LB}$ and $\overline{UB}$ ≥ V_{DD} – 0.2 V, these limits are assured for the condition $\overline{CE1}$ ≥ V_{DD} – 0.2 V or $\overline{CE1}$ ≤ 0.2 V and CE2 ≥ V_{DD} – 0.2 V or CE2 ≤ 0.2 V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.7 to 3.3 V)

READ CYCLE

SYMBOL	PARAMETER	TC55W800XB				UNIT
		7		8		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	—	85	—	ns
t_{ACC}	Address Access Time	—	70	—	85	
t_{CO1}	Chip Enable($\overline{CE1}$) Access Time	—	70	—	85	
t_{CO2}	Chip Enable(CE2) Access Time	—	70	—	85	
t_{OE}	Output Enable Access Time	—	35	—	45	
t_{BA}	Data Byte Control Access Time	—	70	—	85	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	0	—	0	—	
t_{OD}	Chip Enable High to Output High-Z	—	30	—	35	
t_{ODO}	Output Enable High to Output High-Z	—	30	—	35	
t_{BD}	Data Byte Control High to Output High-Z	—	30	—	35	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55W800XB				UNIT
		7		8		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	—	85	—	ns
t_{WP}	Write Pulse Width	50	—	55	—	
t_{CW}	Chip Enable to End of Write	60	—	70	—	
t_{BW}	Data Byte Control to End of Write	60	—	70	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	30	—	35	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	30	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	$V_{DD} \times 0.5$
Reference level	$V_{DD} \times 0.5$
t_R, t_F	5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.3 to 3.3 V)

READ CYCLE

SYMBOL	PARAMETER	TC55W800XB				UNIT
		7		8		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	85	—	100	—	ns
t_{ACC}	Address Access Time	—	85	—	100	
t_{CO1}	Chip Enable($\overline{CE1}$) Access Time	—	85	—	100	
t_{CO2}	Chip Enable(CE2) Access Time	—	85	—	100	
t_{OE}	Output Enable Access Time	—	45	—	50	
t_{BA}	Data Byte Control Access Time	—	85	—	100	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	0	—	0	—	
t_{OD}	Chip Enable High to Output High-Z	—	35	—	40	
t_{ODO}	Output Enable High to Output High-Z	—	35	—	40	
t_{BD}	Data Byte Control High to Output High-Z	—	35	—	40	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

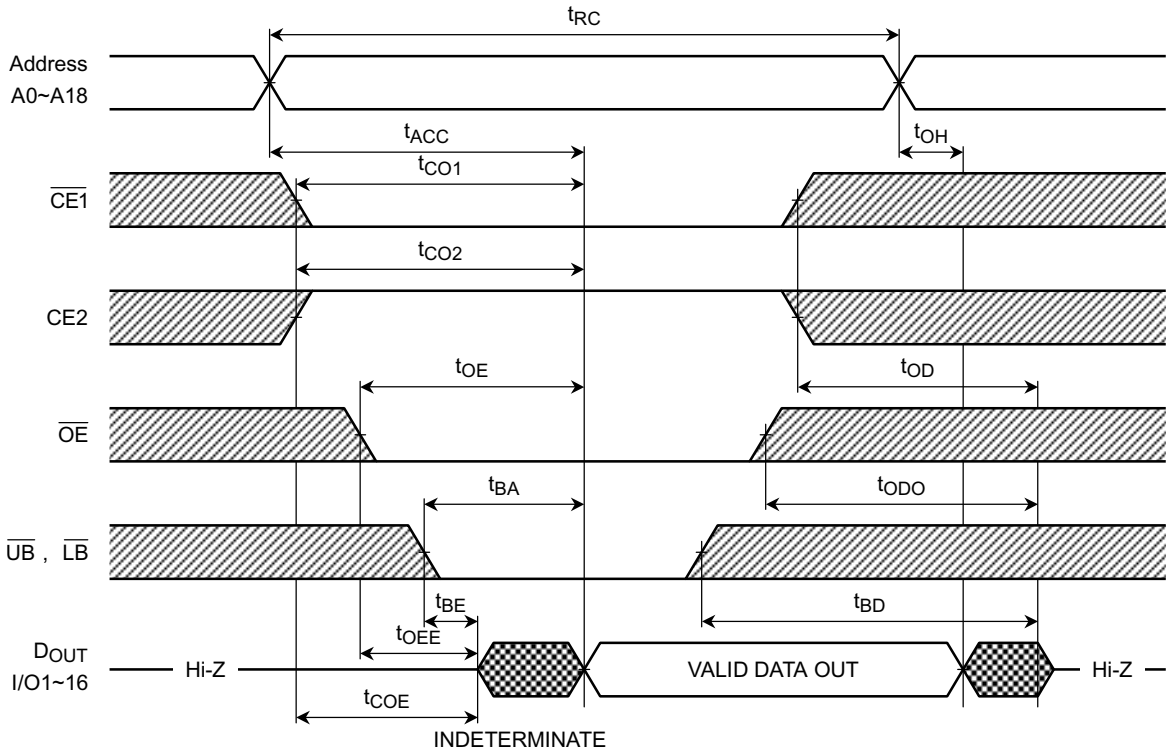
SYMBOL	PARAMETER	TC55W800XB				UNIT
		7		8		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	85	—	100	—	ns
t_{WP}	Write Pulse Width	55	—	60	—	
t_{CW}	Chip Enable to End of Write	70	—	80	—	
t_{BW}	Data Byte Control to End of Write	70	—	80	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	35	—	40	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	35	—	40	—	
t_{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

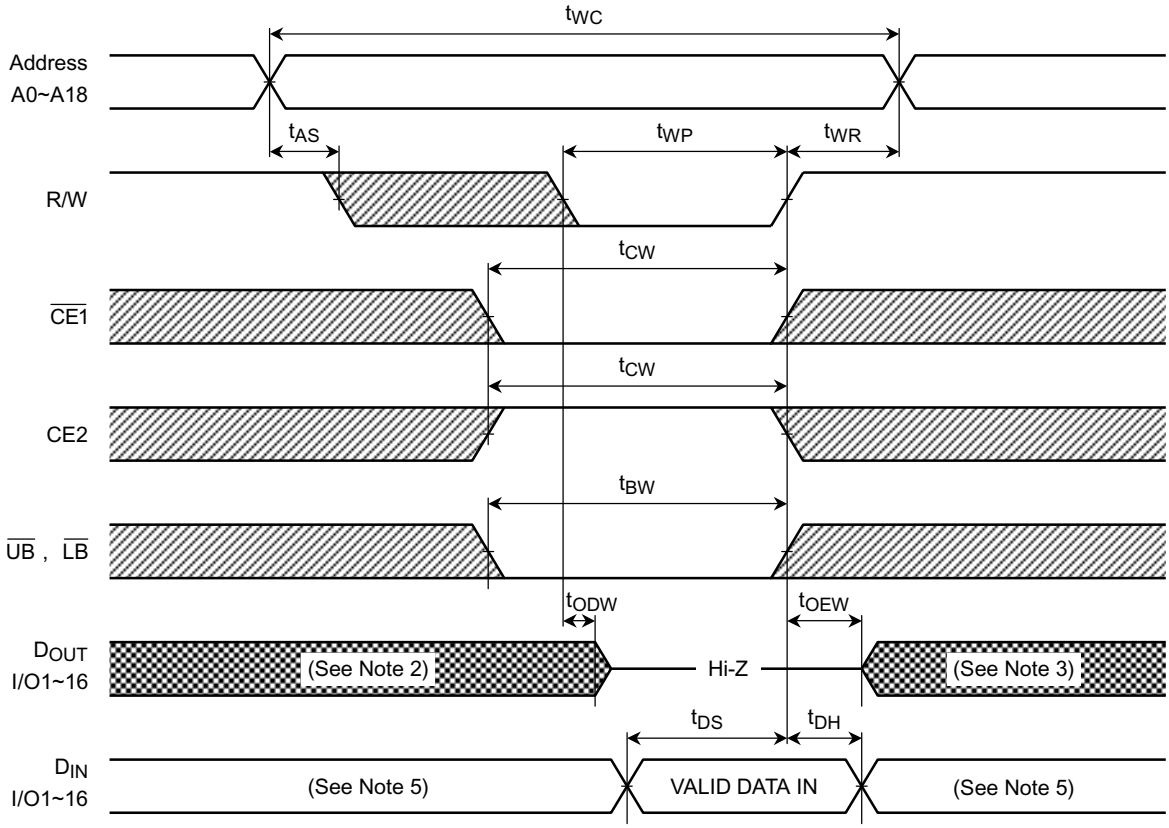
PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V_{DD} – 0.2 V, 0.2 V
Timing measurements	$V_{DD} \times 0.5$
Reference level	$V_{DD} \times 0.5$
t_R, t_F	5 ns

TIMING DIAGRAMS

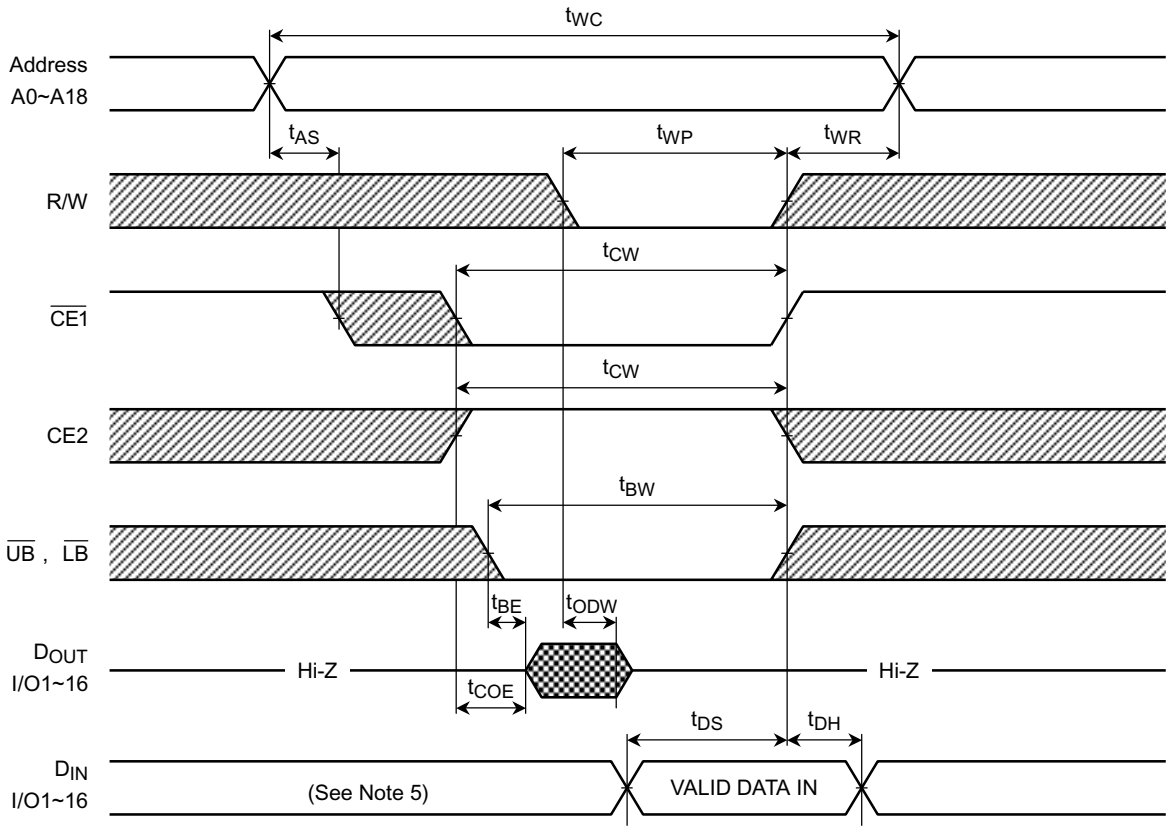
READ CYCLE (See Note 1)



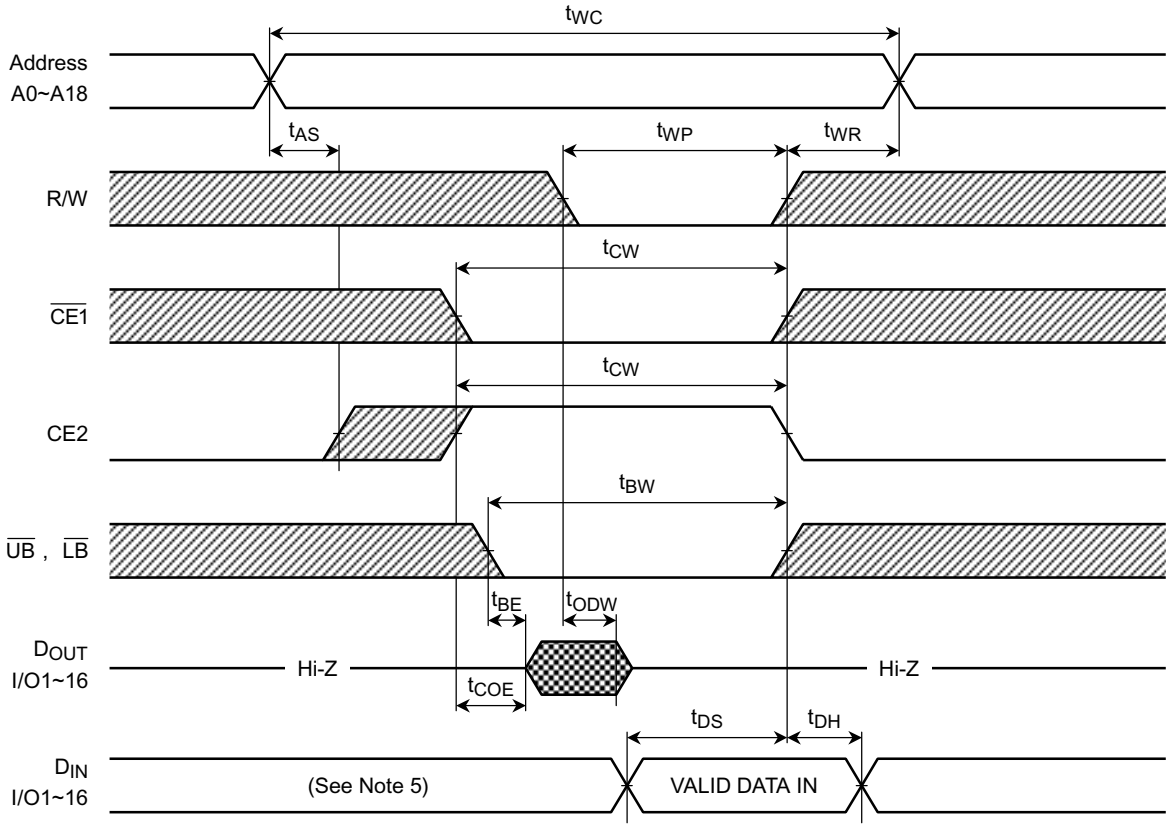
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



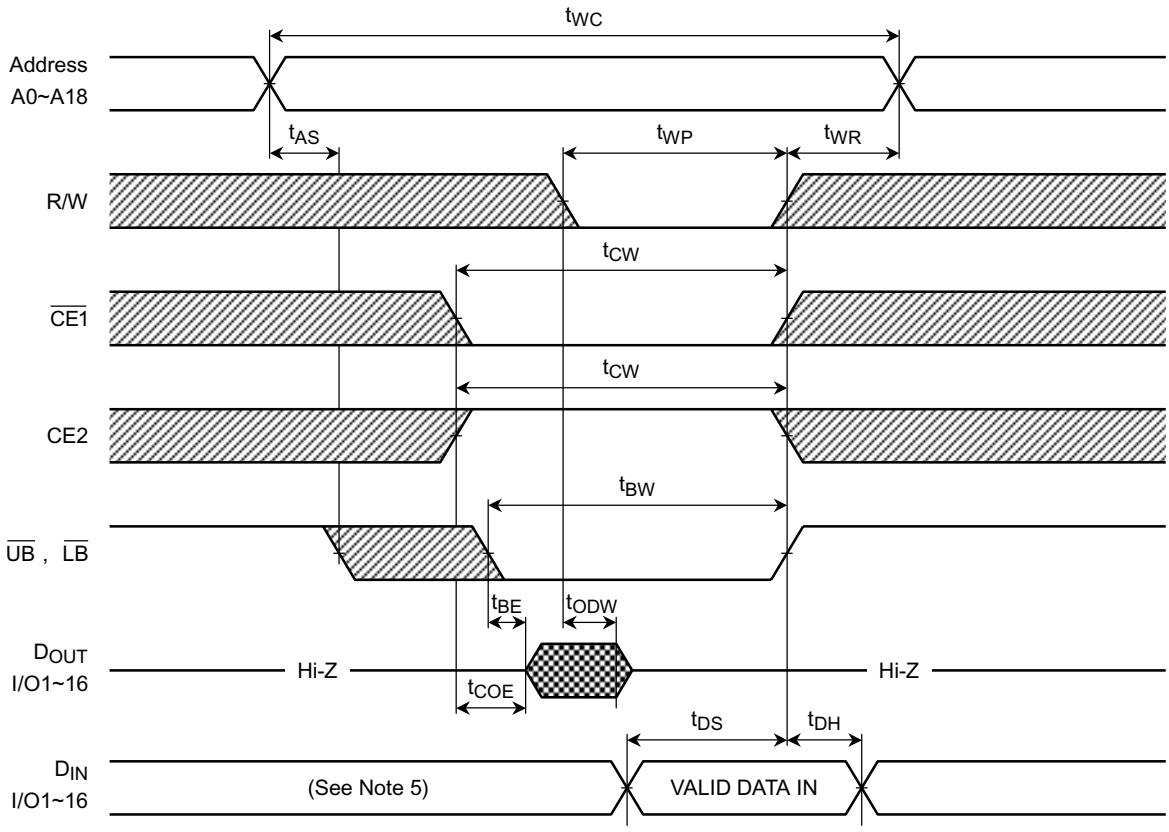
WRITE CYCLE 2 ($\overline{CE1}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



WRITE CYCLE 4 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)



Note:

(1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE1}$ goes LOW(or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE1}$ goes HIGH(or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

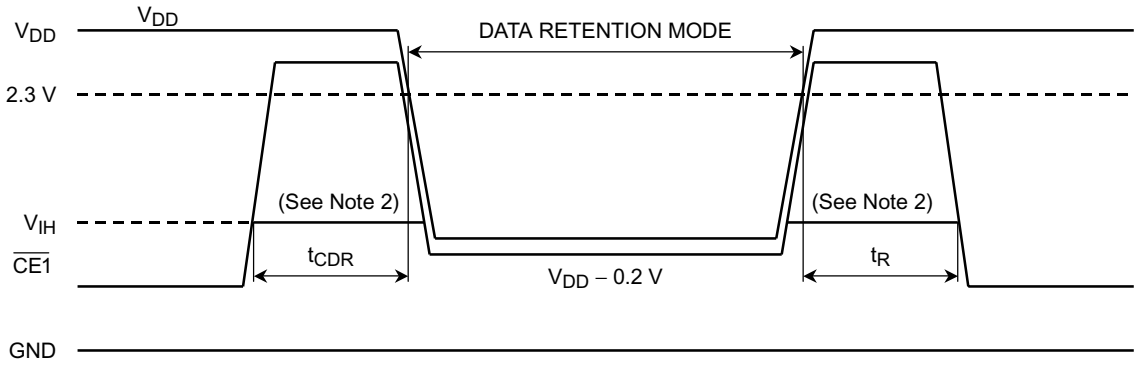
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = –40° to 85°C)

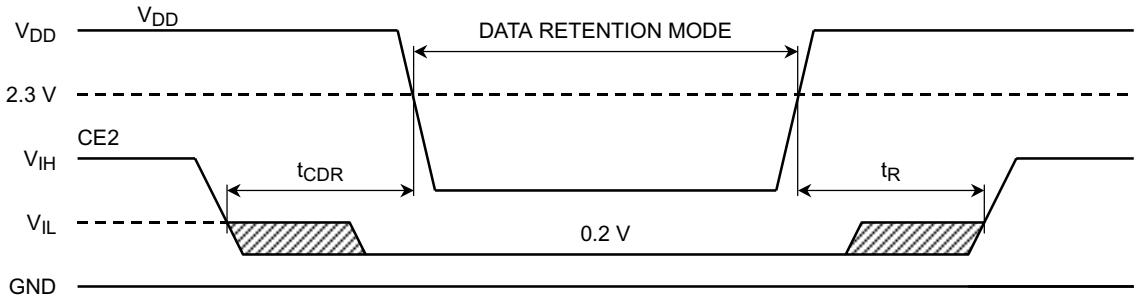
SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			1.5	—	3.3	V
I_{DDS2}	Standby Current	V_{DH} = 3.3 V	Ta = –40~85°C	—	—	10	μA
		V_{DH} = 3.0 V	Ta = –40~40°C	—	—	1	
			Ta = –40~85°C	—	—	5	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	—	—	ns
t_R	Recovery Time			t_{RC} (See Note)	—	—	ns

Note: Read cycle time

$\overline{CE1}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



Note:

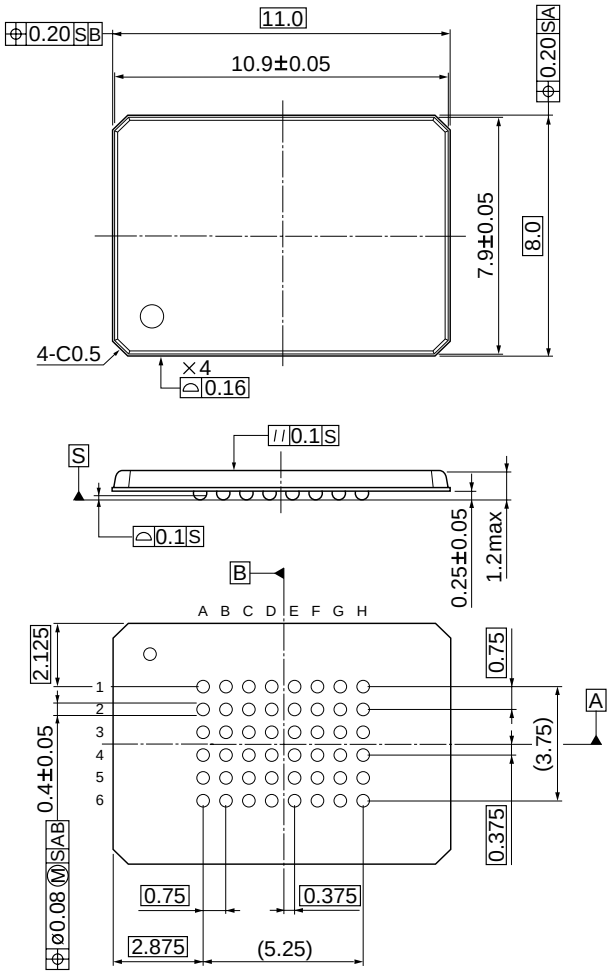
(1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V or CE2 ≥ V_{DD} – 0.2 V.

(2) When $\overline{CE1}$ is operating at the V_{IH} level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.3 to 2.2V.

(3) In CE2 controlled data retention mode, minimum standby current mode is entered when CE2 ≤ 0.2 V.

PACKAGE DIMENSIONS

P-TFBAG48-0811-0.75AZ Unit: mm



Weight: 0.21 g (typ)

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000707EBA

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