DATA SHEET

PCA2000; PCA2001
32 kHz watch circuit with programmable adaptive motor pulse

Product specification
Supersedes data of 2003 Feb 04

2003 Dec 17

Philips
Semiconductors

PHILIPS

32 kHz watch circuit with programmable adaptive motor pulse

PCA2000; PCA2001

FEATURES

- Amplitude-regulated 32 kHz quartz crystal oscillator, with excellent frequency stability and high immunity to leakage currents
- Electrically programmable time calibration with 1 ppm resolution stored in One Time Programmable (OTP) memory
- The quartz crystal is the only external component connected
- Very low power consumption, typical 90 nA
- One second output pulses for bipolar stepping motor
- Minimum power consumption for the entire watch, due to self adaptation of the motor drive according to the required torque
- Reliable step detection circuit
- Motor pulse width, pulse modulation, and pulse adaptation range programmable in a wide range, stored in OTP memory
- Stop function for accurate time setting and power saving during shelf life
- End Of Life (EOL) indication for silver oxide or lithium battery (only the PCA2000 has the EOL feature)
- Test mode for accelerated testing of the mechanical parts and the IC.

APPLICATIONS

- Driver circuits for bipolar stepping motors
- High immunity motor drive circuits.

GENERAL DESCRIPTION

The PCA2000; PCA2001 are CMOS integrated circuits for battery operated wrist watches with a 32 kHz quartz crystal as timing element and a bipolar 1 Hz stepping motor. The quartz crystal oscillator and the frequency divider are optimized for minimum power consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment.

To obtain the minimum overall power consumption for the watch, an automatic motor pulse adaptation function is provided. The circuit supplies only the minimum drive current, which is necessary to ensure a correct motor step. Changing the drive current of the motor is achieved by chopping the motor pulse with a variable duty cycle. The pulse width and the range of the variable duty cycle can be programmed to suit different types of motor. The automatic pulse adaptation scheme is based on a safe dynamic detection of successful motor steps.

A pad RESET is provided (used for stopping the motor) for accurate time setting and for accelerated testing of the watch.

The PCA2000 has a battery EOL warning function. If the battery voltage drops below the EOL threshold voltage (which can be programmed for silver oxide or lithium batteries), the motor steps change from one pulse per second to a burst of four pulses every 4 seconds.

The PCA2001 uses the same circuit as the PCA2000, but without the EOL function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA2000U/AA	–	bare die; chip in tray	–
PCA2001U/AA	–	bare die; chip in tray	–
PCA2000U/10AA	–	bare die; chip on film frame carrier	–
PCA2001U/10AA	–	bare die; chip on film frame carrier	–

BLOCK DIAGRAM

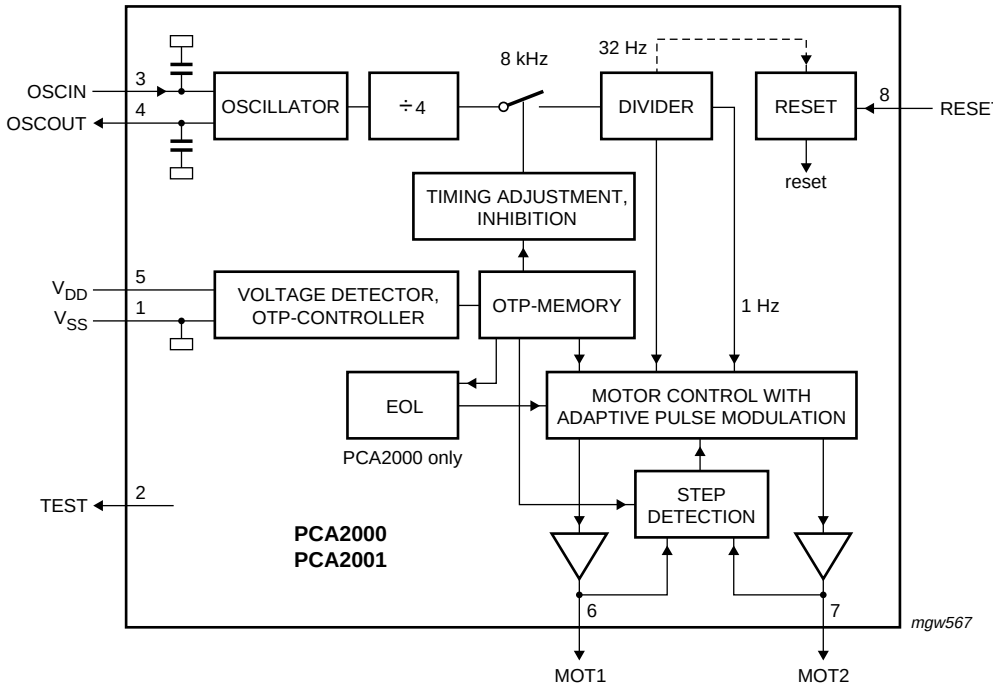


Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
V_{SS}	1	ground
TEST	2	test output
OSCIN	3	oscillator input
OSCOUT	4	oscillator output
V_{DD}	5	supply voltage
MOT1	6	motor 1 output
MOT2	7	motor 2 output
RESET	8	reset input

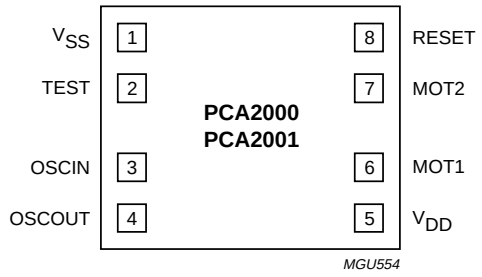


Fig.2 Pad configuration.

FUNCTIONAL DESCRIPTION

Motor pulse

The motor output supplies pulses of different driving stages, depending on the torque required to turn on the motor. The number of different stages can be selected between three and six. With the exception of the highest driving stage, each motor pulse (t_p in Figs 3 and 6) is followed by a detection phase during which the motor movement is monitored, in order to check whether the motor has turned correctly or not.

If a missing step is detected, a correction sequence is generated (see Fig.3) and the driving stage is switched to the next level. The correction sequence consists of two pulses: first a short pulse in the opposite direction (0.98 ms, modulated with the maximum duty cycle) to give the motor a defined position, followed by a motor pulse of the strongest driving level. Every 4 minutes, the driving level is lowered again by one stage.

The motor pulse has a constant pulse width. The driving level is regulated by chopping the driving pulse with a variable duty cycle. The driving level starts from the programmed minimum value and increases by 6.25% after each failed motor step. The strongest driving stage, which is not followed by a detection phase, is programmed separately.

Therefore, it is possible to program a larger energy gap between the pulses with step detection and the strongest, not monitored, pulse. This might be necessary to ensure a reliable and stable operation under adverse conditions (magnetic fields, vibrations). If the watch works in the highest driving stage, the driving level jumps after the 4-minute period directly to the lowest stage, and not just one stage lower.

To optimize the performance for different motors, the following parameters can be programmed:

- Pulse width: 0.98 to 7.8 ms in steps of 0.98 ms
- Duty cycle of lowest driving level: 37.5% to 56.25% in steps of 6.25%
- Number of driving levels (including the highest driving level): 3 to 6
- Duty cycle of the highest driving level: 75% or 100%
- Enlargement pulse for the highest driving level: on or off.

The enlargement pulse has a duty cycle of 25% and a pulse width which is twice the programmed motor pulse width. The repetition period for the chopping pattern is 0.98 ms. Figure 4 shows an example of a 3.9 ms pulse.

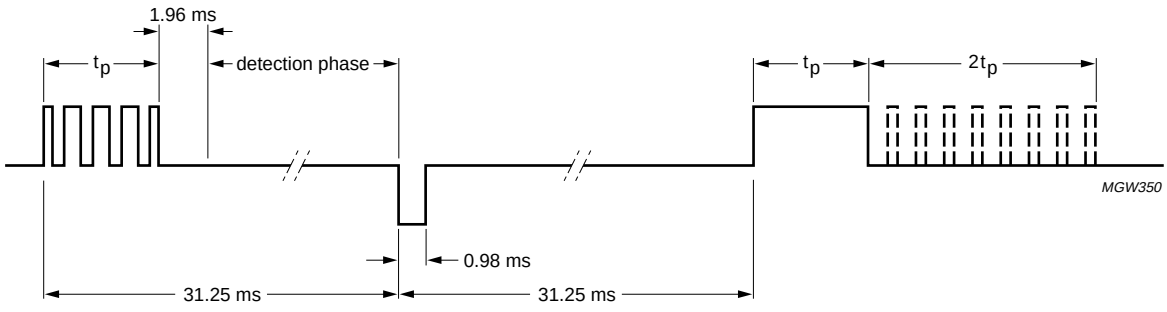


Fig.3 Correction sequence after failed motor step.

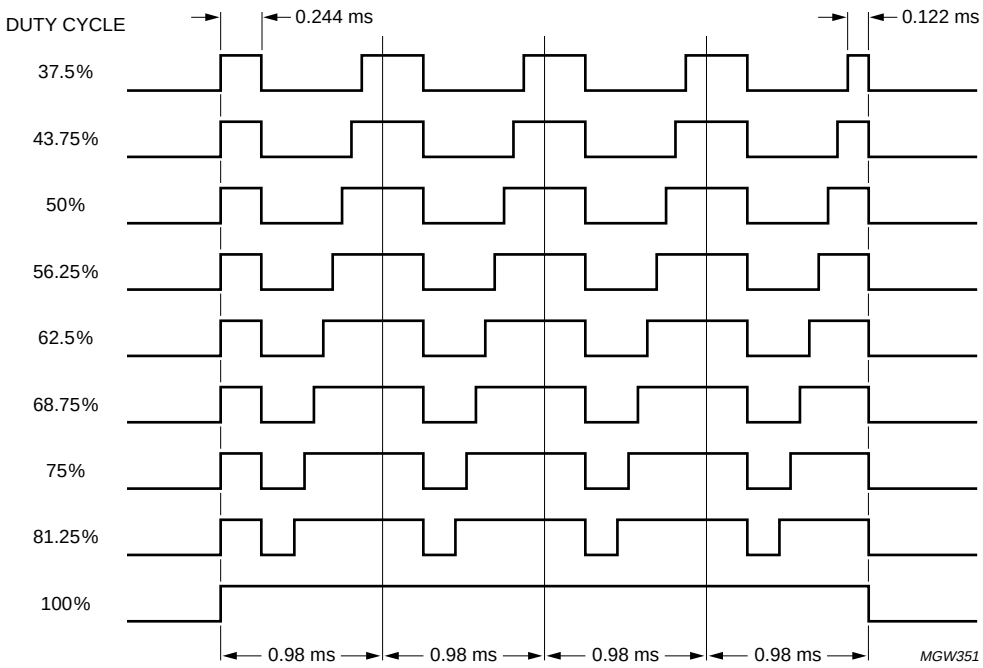


Fig.4 Possible modulations for a 3.9 ms motor pulse.

Step detection

Figure 5 shows a simplified diagram of the motor driving and step detection circuit, and Fig.6 shows the step detection sequence and corresponding sampling current. Between the motor driving pulses, the switches P1 and P2 are closed, which means the motor is short-circuited. For a pulse in one direction, P1 and N2 are open, and P2 and N1 are closed with the appropriate duty cycle; for a pulse in the opposite direction, P2 and N1 are open, and P1 and N2 closed.

The step detection phase is initiated after the motor driving pulse (see Fig.3). P1 and P2 are first closed for 0.98 ms and then all four drive switches (P1, N1, P2 and N2) are opened for 0.98 ms.

As a result, the energy stored in the motor inductance is reduced as fast as possible.

The induced current caused by the residual motor movement is then sampled in phase 3 (closing P3 and P2) and in phase 4 (closing P1 and P4). For step detection in the opposite direction P1 and P4 are closed during phase 3 and P2 and P3 during phase 4 (see Fig.6).

The condition for a successful motor step is a positive step detection pulse (current in the same direction as in the driving phase) followed by a negative detection pulse within a given time limit. This time limit can be programmed between 3.9 and 10.7 ms (in steps of 0.98 ms) in order to ensure a safe and correct step detection under all conditions (for instance magnetic fields). The step detection phase stops after the last 31.25 ms, after the start of the motor driving pulse.

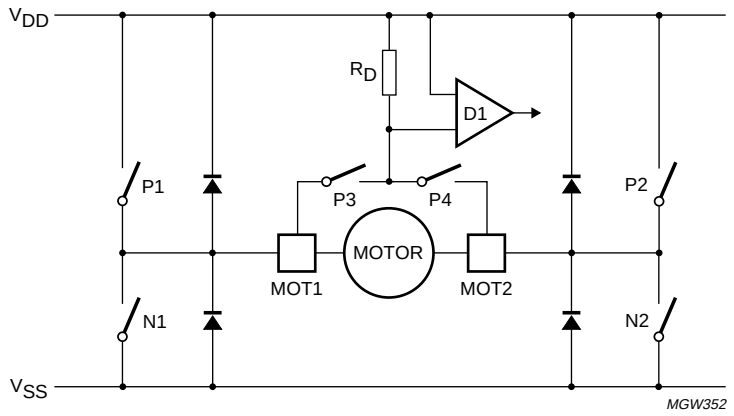


Fig.5 Simplified diagram of motor driving and step detection circuit.

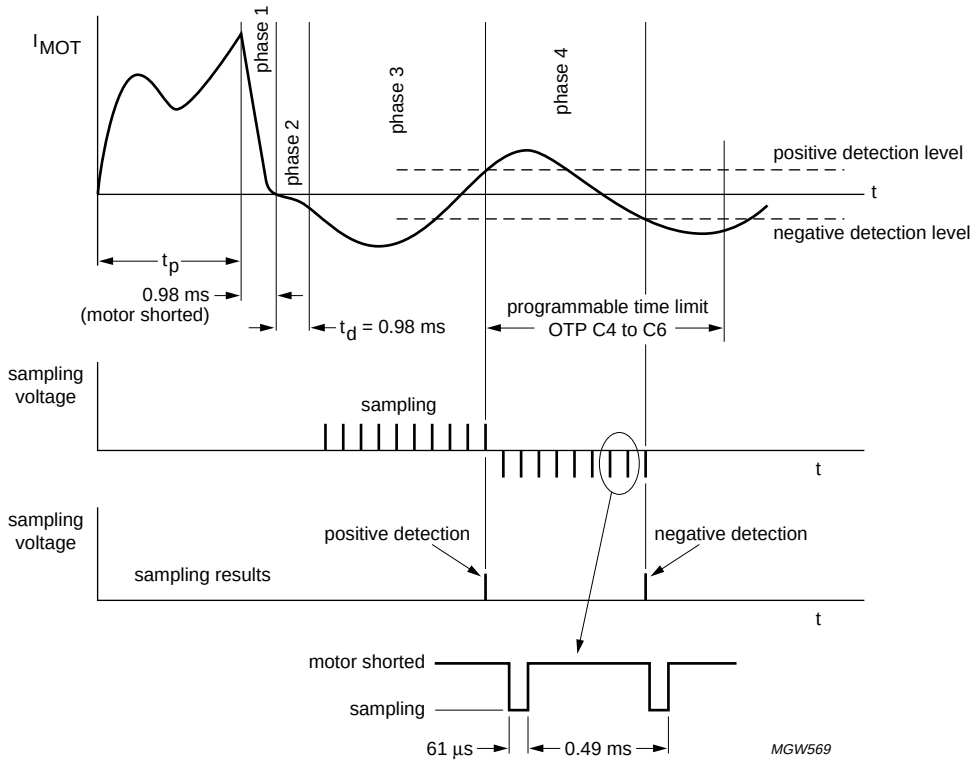


Fig.6 Step detection sequence and corresponding sampling voltage.

Time calibration

The quartz crystal oscillator has an integrated capacitance of 5.2 pF, which is lower than the specified capacitance (C_L) of 8.2 pF for the quartz crystal. Therefore, the oscillator frequency is typically 60 ppm higher than 32.768 kHz. This positive frequency offset is compensated by removing the appropriate number of 8192 Hz pulses in the divider chain (maximum 127 pulses), every 1 or 2 minutes. The time correction is given in Table 1.

After measuring the effective oscillator frequency, the number of correction pulses must be calculated and stored together with the calibration period in the OTP memory (see Section “Programming the memory cells”).

The oscillator frequency can be measured at pad RESET, where a square wave signal with the frequency of $\frac{1}{1024} \times f_{osc}$ is provided.

This frequency shows a jitter every minute or every two minutes, depending on the programmed calibration period, which originates from the time calibration.

Details on how to measure the oscillator frequency and the programmed inhibit time are given in Section “Measurement of oscillator frequency and inhibit time”.

Reset

At pin RESET an output signal with a frequency of $\frac{1}{1024} \times f_{osc}$ = 32 Hz is provided.

Connecting pad RESET to V_{DD} stops the motor drive and opens all four (P1, N1, P2 and N2) driver switches (see Fig.5). Connecting pad RESET to V_{SS} activates the test mode. In this mode the motor output frequency is 32 Hz, which can be used to test the mechanical function of the watch.

After releasing the pad RESET, the motor starts exactly one second later with the smallest duty cycle and with the opposite polarity to the last pulse before stopping.

The debounce time for the RESET function is between 31 and 62 ms.

Programming possibilities

The programming data is stored in OTP cells (EPROM cells). At delivery, all memory cells are in state 0. The cells can be programmed to the state 1, but then there is no more set back to state 0.

The programming data is organized in an array of three 8-bit words: word A contains the time calibration, and words B and C contain the setting for the monitor pulses (see Table 2).

Table 1 Time calibration

CALIBRATION PERIOD	CORRECTION PER STEP (n = 1)		CORRECTION PER STEP (n = 127)	
	ppm	seconds per day	ppm	seconds per day
1 minute	2.03	0.176	258	22.3
2 minutes	1.017	0.088	129	11.15

Table 2 Words and bits

WORD	BIT							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	lowest stage: duty cycle		number of driving stages		highest stage: duty cycle and stretching		factory test bit	
C	pulse width			maximum time delay between positive and negative detection pulses			EOL voltage	factory test bit

Table 3 Description of word A bits

BIT	VALUE	DESCRIPTION
Inhibit time		
1 to 7	–	Adjust the number of the 8192 Hz pulses to be removed. Bit 1 is the MSB and bit 7 is the LSB.
Calibration period		
8	0	1 minute
	1	2 minutes

Table 4 Description of word B bits

BIT	VALUE	DESCRIPTION
Duty cycle lowest driving stage		
1 to 2	00	37.5%
	01	43.75%
	10	50%
	11	56.25%
Number of driving stages		
3 to 4	00	3
	01	4
	10	5
	11	6; note 1
Duty cycle highest driving stage		
5	0	75%; note 2
	1	100%
Stretching pulse		
6	0	pulse is not stretched
	1	pulse of $2t_{pr}$ and duty cycle of 25% is added
Factory test bits		
7 to 8	–	

Notes

1. Including the highest driving stage, which one has no motor step detection.
2. If the maximum duty cycle of 75% is selected, not all programming combinations are possible since the second highest level must be smaller than the highest driving level.

Table 5 Description of word C bits

BIT	VALUE	DESCRIPTION
Pulse width t_{pr} (ms)		
1 to 3	000	0.98
	001	1.95
	010	2.90
	011	3.90
	100	4.90
	101	5.90
	110	6.80
	111	7.80
Time delay t_{max} (ms); note 1		
4 to 6	000	3.91
	001	4.88
	010	5.86
	011	6.84
	100	7.81
	101	8.79
	110	9.77
	111	10.74
EOL voltage of the battery		
7	0	1.38 V (silver-oxide)
	1	2.5 V (lithium)
Factory test bit		
8	–	

Note

1. Between positive and negative detection pulses.

Programming procedure

For a watch it is essential that the timing calibration can be made after the watch is fully assembled. In this situation, the supply pads are often the only terminals which are still accessible.

Writing to the OTP cells and performing the related functional checks is achieved in the PCA2000; PCA2001 by modulating the supply voltage. The necessary control circuit consists basically of a voltage level detector, an instruction counter which determines the function to be performed, and an 8-bit shift register which allows writing to the OTP cells of an 8-bit word in one step and acts as a data pointer for checking the OTP content.

There are five different instruction states (states 3 and 5 are handled as state 4):

- State 1: measurement of the quartz crystal oscillator frequency (divided by 1024)
- State 2: measurement of the inhibit time
- State 3: write/check word A
- State 4: write/check word B
- State 5: write/check word C.

Each instruction state is switched on with a pulse to V_P (6.7 V). After this large pulse, an initial waiting time of t_0 (20 ms) is required. The programming instructions are then entered by modulating the supply voltage with small pulses (amplitude $V_{P(mod)}$ = 0.35 V and pulse width t_{mod} = 30 µs). The first small pulse defines the start time, the following pulses perform three different functions, depending on the delay from the preceding pulse (see Figs 7, 8, 11, and 12):

- t_1 = 0.7 ms: increments the instruction counter
- t_2 = 1.7 ms: clocks the shift register with data = logic 0
- t_3 = 2.7 ms: clocks the shift register with data = logic 1.

The programming procedure requires a stable oscillator. This means that a waiting time, determined by the start-up time of the oscillator is necessary after power-up of the circuit.

After the $V_{P(start)}$ pulse, the instruction counter is in state 1 and the data shift register is cleared.

The instruction state ends with a second pulse to $V_{P(stop)}$ or with a pulse to V_{store}.

In any case, the instruction states are terminated automatically 2 seconds after the last $V_{DD(mod)}$ pulse.

Programming the memory cells

Applying the two-stage programming pulse (see Fig.7) transfers the stored data in the shift register to the OTP cells.

Perform the following to program a memory word:

1. Starting with a $V_{P(start)}$ pulse wait for the time period t_0 then set the instruction counter to the word you want to write ($t_d = t_1$).
2. Enter the data you want to store in the shift register ($t_d = t_2$ or t_3). Enter the LSB first (bit 8) and the MSB last (bit 1).
3. Apply the two-stage programming pulse ($V_{pre\text{-}store}$ then V_{store}) stores the word. The delay between the last data bit and the pre-store pulse ($V_{pre\text{-}store}$) is $t_d = t_4$.

The example shown in Fig.7 performs the following functions:

- Start
- Setting instruction counter to state 4 (word B)
- Entering data word 110101 into the shift register (sequence: first bit 6 and last bit 1)
- Writing to the OTP cells for word B.

General start up sequence

You must follow the sequence below to ensure the correct operation at start up:

1. Apply the supply voltage to the circuit.
2. Wait for at least 2 seconds.
3. Connect the pad RESET to V_{DD} for a minimum of 62 ms (this activates the stop mode).
4. Disconnect the pad RESET from V_{DD} (this resets the circuit to normal operating mode).

After this sequence the memory contents are read immediately and the programmed options are set. This sequence also resets all major circuit blocks and ensures that they function correctly.

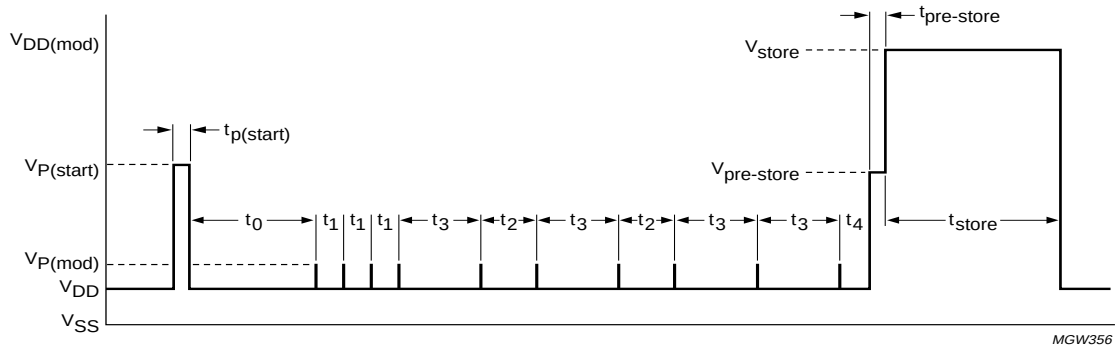


Fig.7 Supply voltage modulation for programming.

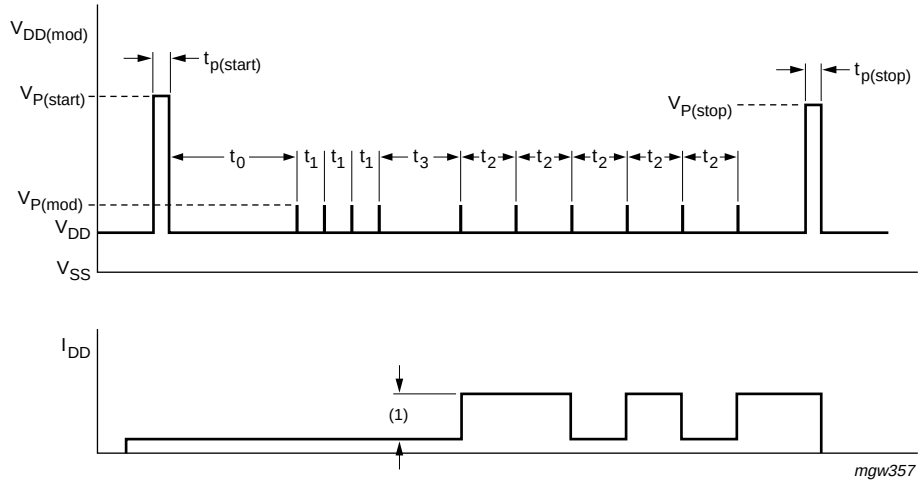
Checking memory content

The stored data of the OTP array can be checked bit wise by measuring the supply current. The array word is selected by the instruction state and the bit is addressed by the shift register.

To read a word, the word is first selected (pulse distance t_1), and a logic 1 is written into the first cell of the shift register (pulse distance t_3). This logic 1 is then shifted through the entire shift register (pulse distance t_2), so that it points with each clock pulse to the next bit.

If the addressed OTP cell contains a logic 1, a 30 kΩ resistor is connected between V_{DD} and V_{SS}, which increases the supply current accordingly.

Figure 8 shows the supply voltage modulation for reading word B, with the corresponding supply current variation for word B = 110101 (sequence: first MSB and last LSB).



(1) $\Delta I_{DD} = \frac{V_{DD}}{30\ k\Omega}$

Fig.8 Supply voltage modulation and corresponding supply current variation for reading word B.

Frequency tuning of assembled watch

Figure 9 shows the test set-up for frequency tuning the assembled watch.

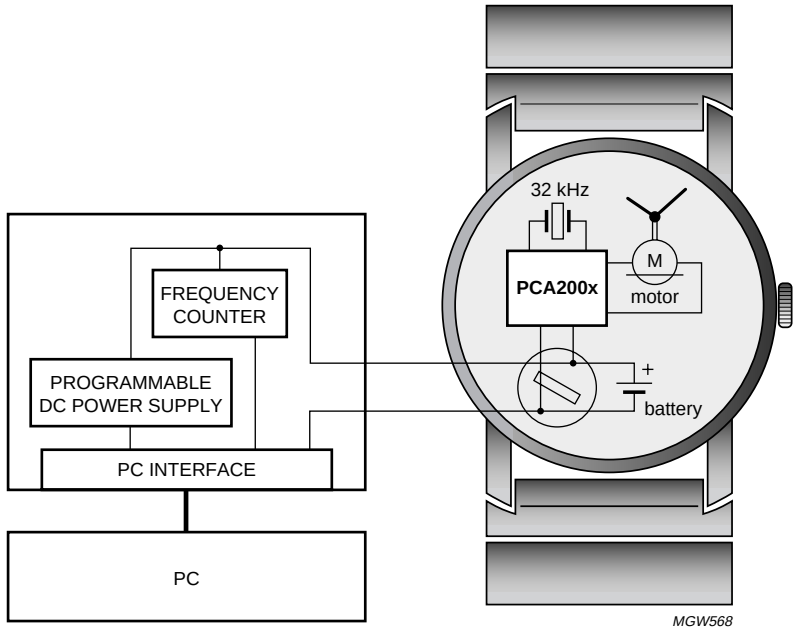


Fig.9 Frequency tuning at assembled watch.

Measurement of oscillator frequency and inhibit time

The output of the two measuring states can either be monitored directly at pad RESET or as a modulation of the supply voltage (a modulating resistor of 30 kΩ is connected between V_{DD} and V_{SS} when the signal at pad RESET is at HIGH-level).

You must follow the supply voltage modulation (see Fig.10)) in order to guarantee the correct start up of the circuit during production and testing.

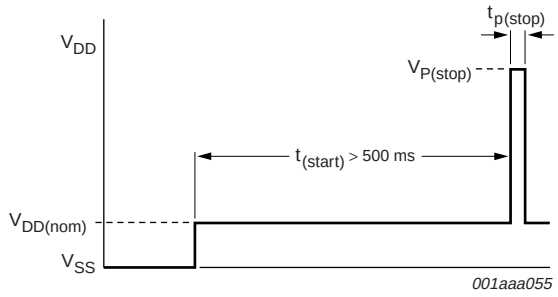


Fig.10 Supply voltage at start up during production and testing.

Measuring states:

- State 1: quartz crystal oscillator frequency divided by 1024; state 1 starts with a pulse to V_P and ends with a second pulse to V_P
- State 2: inhibit time (see Figs 11 and 12); a signal with periodicity of 31.25 + n × 0.122 ms appears at pad RESET and as current modulation at pad V_{DD}.

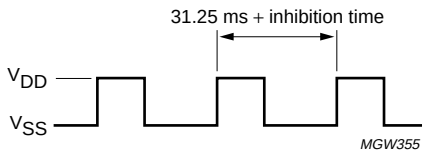


Fig.11 Output waveform at pad RESET for instruction state 2.

Customer testing

Connecting pad RESET to V_{SS} activates the test mode. In this test mode, the motor output frequency is 8 Hz; the duty cycle reduction and battery check occurs every second, instead of every 4 minutes. If the supply voltage drops below the EOL threshold voltage, the motor output frequency is 32 Hz with the highest driving level.

EOL of battery

The supply voltage is checked every 4 minutes. If it drops below the EOL reference (1.38 V for silver-oxide, 2.5 V for lithium batteries), the motor steps change from one pulse per second to a burst of four pulses every 4 seconds. The step detection is switched off, and the motor is driven with the highest pulse level.

Only the PCA2000 has an EOL function.

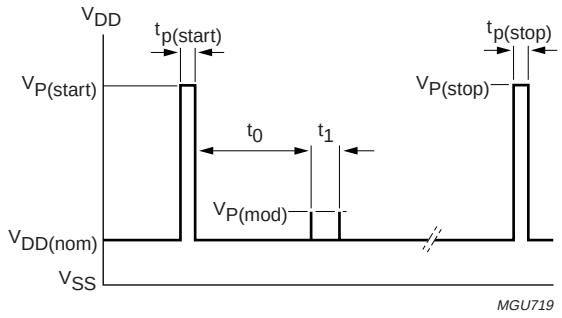


Fig.12 Supply voltage modulation for starting and stopping of instruction state 2.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; notes 1 and 2	–1.8	+7.0	V
V_i	all input voltages		V_{SS} – 0.5	V_{DD} + 0.5	V
T_{amb}	ambient temperature		–10	+60	°C
T_{stg}	storage temperature		–30	+100	°C
$t_{o(sc)}$	output short-circuit duration		indefinite		s

Notes

1. For writing to the OTP cells, the supply voltage V_{DD} can be raised to a maximum of 12 V for a period of 1 second.
2. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which rapidly discharges the battery.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However to be totally safe, it is advised to undertake handling precautions appropriate to handling MOS devices. Advice can be found in *"Data handbook IC16: General; handling MOS devices"*.

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; quartz crystal: R_S = 40 kΩ, C_1 = 2 to 3 fF, C_L = 8.2 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	normal operating mode; T_{amb} = –10 to +60 °C	1.10	1.55	3.60	V
ΔV_{DD}	supply voltage variation	$\Delta V/\Delta t$ = 1 V/µs	–	–	0.25	V
I_{DD}	supply current	between motor pulses	–	90	120	nA
		between motor pulses at V_{DD} = 3.5 V	–	120	180	nA
		T_{amb} = –10 to +60 °C	–	–	200	nA
		stop mode; pad RESET connected to V_{DD}	–	100	135	nA
Motor output						
V_{sat}	saturation voltage	R_M = 2 kΩ; T_{amb} = –10 to +60 °C; note 1	–	150	200	mV
Z_{sc}	short-circuit impedance	between motor pulses; I_{motor} < 1 mA	–	200	300	Ω
Oscillator						
V_{start}	starting voltage		1.1	–	–	V
g_m	transconductance	$V_{OSCIN} \leq$ 50 mV (p-p)	5	10	–	µS
t_{osc}	start-up time		–	0.3	0.9	s
$\Delta f/f$	frequency stability	ΔV_{DD} = 100 mV	–	0.05	0.20	ppm
C_{int}	integrated load capacitance		4.3	5.2	6.3	pF
R_{par}	parasitic resistance	allowed resistance between adjacent pads	20	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage level detector						
$V_{th(EOL)}$	EOL threshold voltage	silver-oxide battery	1.30	1.38	1.46	V
		lithium battery	2.35	2.50	2.65	V
TC_{EOL}	temperature coefficient		–	–0.07	–	%/°C
Pad RESET						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R_L = 1 MΩ; C_L = 10 pF; note 2	1.4	–	–	V
t_r, t_f	rise and fall time	R_L = 1 MΩ; C_L = 10 pF; note 2	–	1	–	µs
$I_{i(AV)}$	average input current	pad RESET connected to V_{DD} or V_{SS}	–	10	20	nA

Notes

1. Σ (P + N).
2. R_L and C_L are a load resistor and load capacitor, externally connected to pad RESET.

Table 6 Specifications for OTP programming (see Figs 7, 8 and 12).

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage during programming procedure	1.5	–	3.0	V
$V_{P(start)}$	supply voltage for starting programming procedure	6.6	–	6.8	V
$V_{P(stop)}$	supply voltage for stopping programming procedure	6.2	–	6.4	V
$V_{P(mod)}$	supply voltage modulation for entering instructions	320	350	380	mV
$V_{pre\text{-}store}$	supply voltage for pre-store pulse	6.2	–	6.4	V
V_{store}	supply voltage for writing to the OTP cells	9.9	10.0	10.1	V
I_{store}	supply current for writing to the OTP cells	–	–	10	mA
$t_{p(start)}$	pulse width of start pulse	8	10	12	ms
$t_{p(stop)}$	pulse width of stop pulse	0.05	–	0.5	ms
t_{mod}	modulation pulse width	25	30	40	µs
$t_{pre\text{-}store}$	pulse width of pre-store pulse	0.05	–	0.5	ms
t_{store}	pulse width for writing to the OTP cells	95	100	110	ms
t_0	waiting time after start pulse	20	–	30	ms
t_1	pulse distance for incrementing the state counter	0.6	0.7	0.8	ms
t_2	pulse distance for clocking the data register with data = logic 0	1.6	1.7	1.8	ms
t_3	pulse distance for clocking the data register with data = logic 1	2.6	2.7	2.8	ms
t_4	waiting time for writing to OTP cells	0.1	0.2	0.3	ms
SR	slew rate for modulation of the supply voltage	0.5	–	5.0	V/µs
R_{read}	supply current modulation read-out resistor	18	30	45	kΩ

Note

1. Program each word once only.

BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
V_{SS}(3)	1	–480	+330
TEST(2)	2	–480	+160
OSCIN	3	–480	–160
OSCOUT	4	–480	–330
V_{DD}	5	+480	–330
MOT1	6	+480	–160
MOT2	7	+480	+160
RESET	8	+480	+330

Notes

1. All coordinates are referenced, in μm, to the centre of the die (see Fig.13).
2. Pad TEST is used for factory tests; in normal operation it should be left open-circuit, and it has an internal pull-down resistance to V_{SS}.
3. The substrate (rear side of the chip) is connected to V_{SS}. Therefore the die pad must be either floating or connected to V_{SS}.

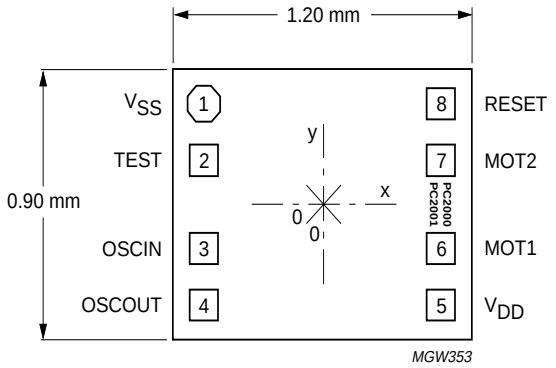


Fig.13 Bonding pad locations.

Table 7 Mechanical chip data; note 1

PARAMETER	VALUE
Bonding pad:	
metal	96 × 96 μm
opening	86 × 86 μm
Thickness:	
chip for bonding	200 ±25 μm
chip for golden bumps	270 ±25 μm
Bumps:	
height	25 ±5 μm

Note

1. The substrate of the chip is connected to V_{SS}.

TRAY INFORMATION

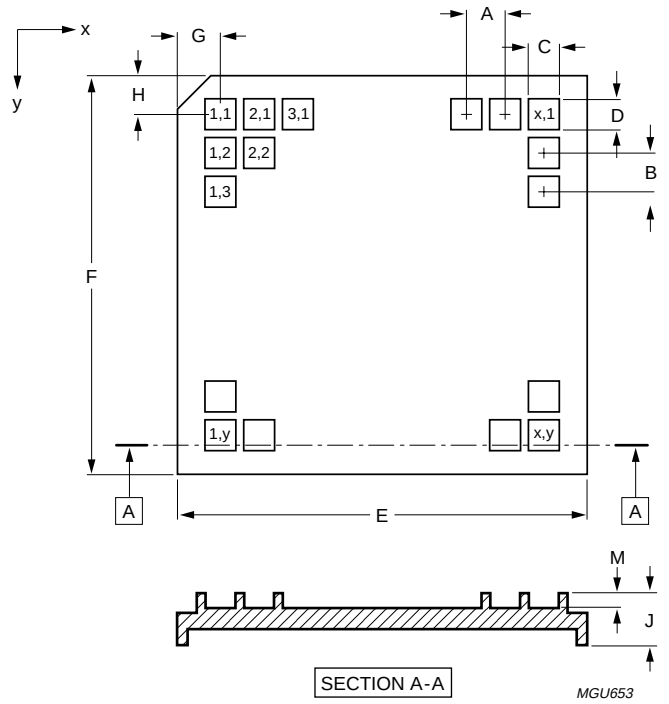
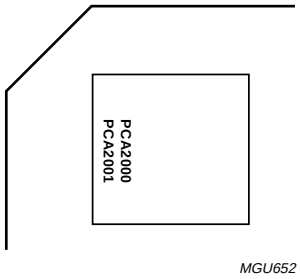


Fig.14 Tray details.

Table 8 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch; x direction	2.15 mm
B	pocket pitch; y direction	2.43 mm
C	pocket width; x direction	1.01 mm
D	pocket width; y direction	1.39 mm
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	distance from cut corner to pocket (1, 1) centre	4.86 mm
H	distance from cut corner to pocket (1, 1) centre	4.66 mm
J	tray thickness	3.94 mm
M	pocket depth	0.61 mm
x	number of pockets in x direction	20
y	number of pockets in y direction	18



The orientation of the IC in a pocket is indicated by the position of the IC type name on the surface of the die, with respect to the cut corner on the upper left of the tray.

Fig.15 Tray alignment.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Bare die — All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of Philips' delivery. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post packing tests performed on individual die or wafer. Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands R15/03/pp19 Date of release: 2003 Dec 17 Document order number: 9397 750 11757

Let's make things better.

Philips
Semiconductors

PHILIPS