

## FDM3622

# N-Channel PowerTrench® MOSFET

100V, 4.4A, 60mΩ

### Features

- $r_{DS(ON)} = 44m\Omega$  (Typ.),  $V_{GS} = 10V$ ,  $I_D = 4.4A$
- $Q_g(tot) = 13nC$  (Typ.),  $V_{GS} = 10V$
- Low Miller Charge
- Low  $Q_{RR}$  Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

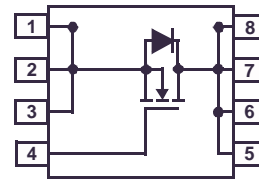
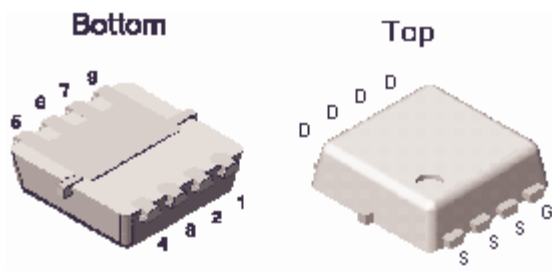
### Applications

- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier

Formerly developmental type 82744

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.



**MicroFET 3.3 x 3.3**

## MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , $R_{\theta JA} = 52^\circ\text{C/W}$ )	4.4	A
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 6\text{V}$ , $R_{\theta JA} = 52^\circ\text{C/W}$ )	3.8	
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , $R_{\theta JA} = 52^\circ\text{C/W}$ )	2.8	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	190	mJ
$P_D$	Power dissipation	2.4	W
	Derate above $25^\circ\text{C}$	19	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1a)	52	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1b)	108	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case (Note 1)	1.8	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDM3622	FDM3622	MicroFET3.3x3.3	7"	12mm	3000 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$T_C = 100^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 4.4\text{A}$ , $V_{GS} = 10\text{V}$	-	0.044	0.060	$\Omega$
		$I_D = 3.8\text{A}$ , $V_{GS} = 6\text{V}$	-	0.056	0.080	
		$I_D = 4.4\text{A}$ , $V_{GS} = 10\text{V}$ , $T_C = 150^\circ\text{C}$	-	0.092	0.120	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	820	-	pF
$C_{OSS}$	Output Capacitance		-	125	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	35	-	pF
$R_G$	Gate Resistance	$V_{GS} = 0.5\text{V}$ , $f = 1\text{MHz}$	-	3.1	-	$\Omega$
$Q_g(TOT)$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	13	17	nC
$Q_g(TH)$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V	-	1.6	2.1	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 50\text{V}$ $I_D = 4.4\text{A}$ $I_g = 1.0\text{mA}$	-	3.6	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	2.0	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	3.4	-	nC

**Resistive Switching Characteristics** ( $V_{GS} = 10V$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 50V, I_D = 4.4A$ $V_{GS} = 10V, R_{GS} = 24\Omega$	-	-	54	ns
$t_{d(ON)}$	Turn-On Delay Time		-	11	-	ns
$t_r$	Rise Time		-	25	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	35	-	ns
$t_f$	Fall Time		-	26	-	ns
$t_{OFF}$	Turn-Off Time		-	-	92	ns

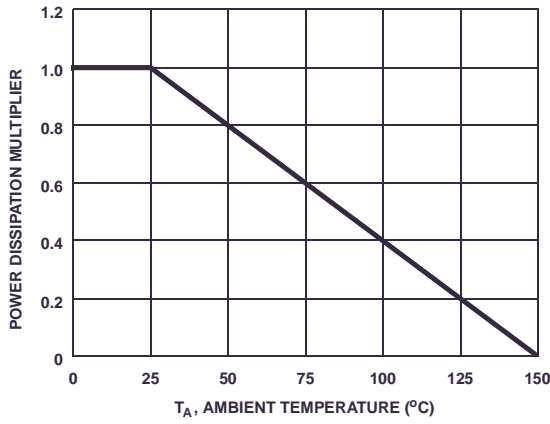
**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 4.4A$	-	-	1.25	V
		$I_{SD} = 2.2A$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 4.4A, dI_{SD}/dt = 100A/\mu s$	-	-	56	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 4.4A, dI_{SD}/dt = 100A/\mu s$	-	-	108	nC

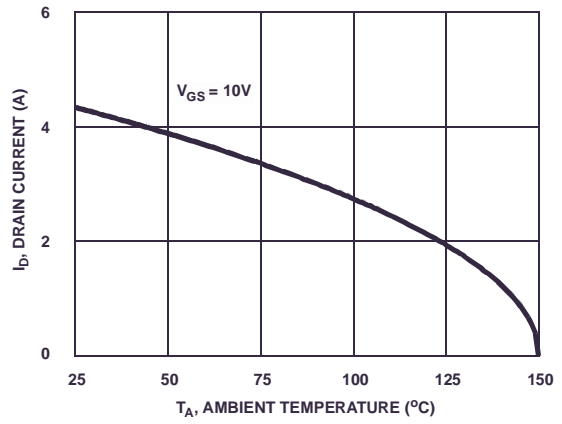
**Notes:**

- $R_{\theta JA}$  is determined with the device mounted on a 1in<sup>2</sup> 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
  - $R_{\theta JA} = 52^{\circ}C/W$  when mounted on a 1in<sup>2</sup> pad of 2 oz. copper.
  - $R_{\theta JA} = 108^{\circ}C/W$  when mounted on a minimum pad of 2 oz. copper.
- Starting  $T_J = 25^{\circ}C, L = 31mH, I_{AS} = 3.5A, V_{DD} = 100V$

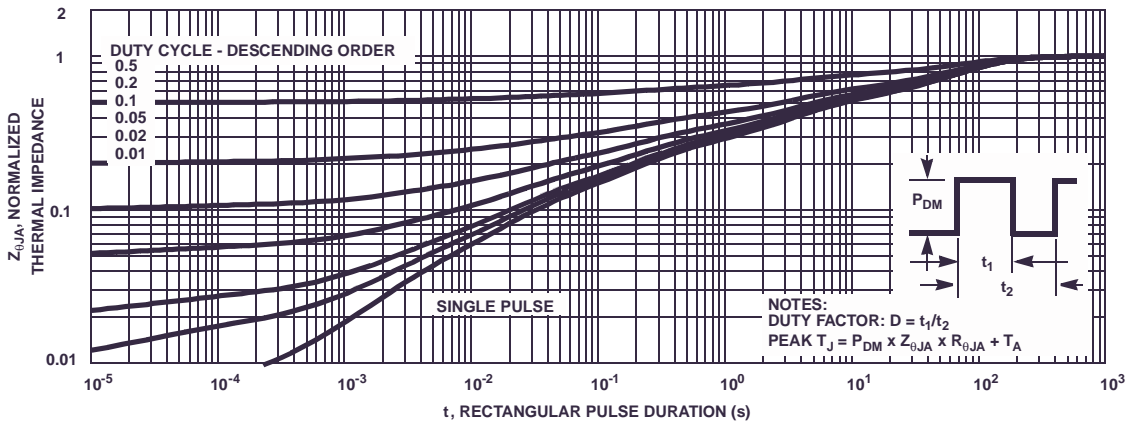
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



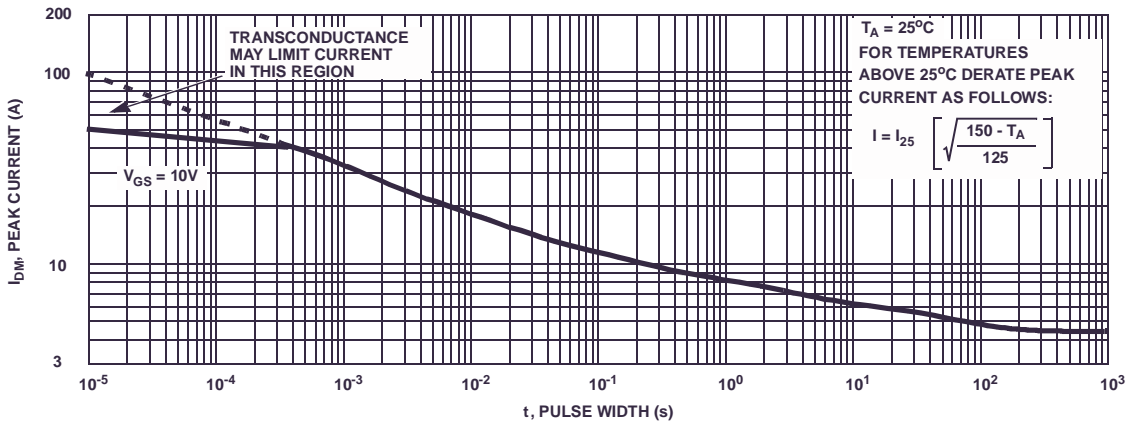
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Ambient Temperature**

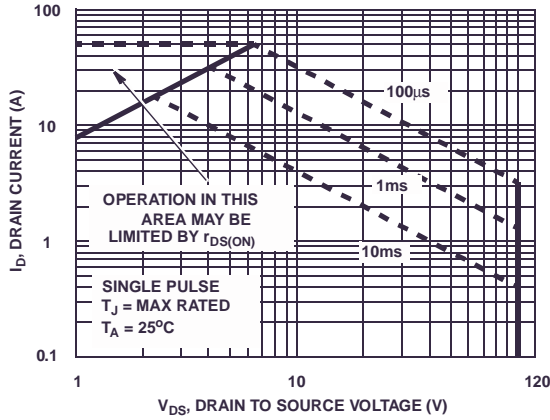


**Figure 3. Normalized Maximum Transient Thermal Impedance**

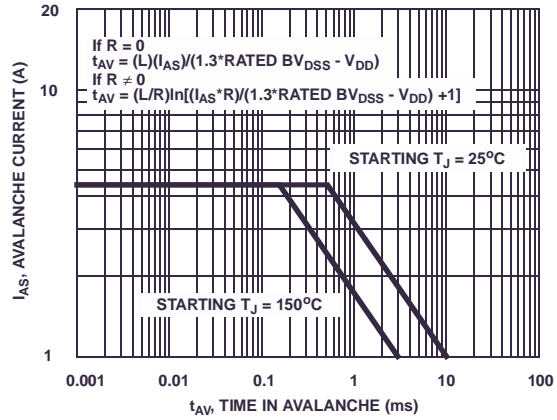


**Figure 4. Peak Current Capability**

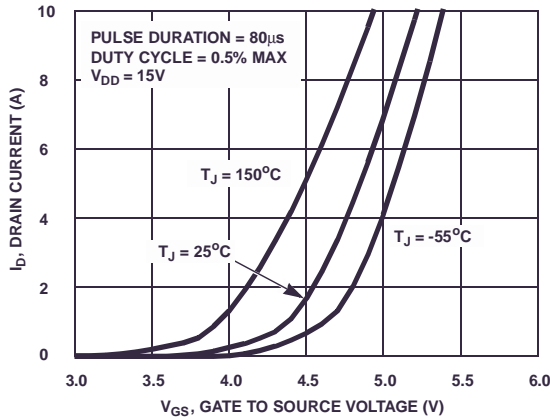
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



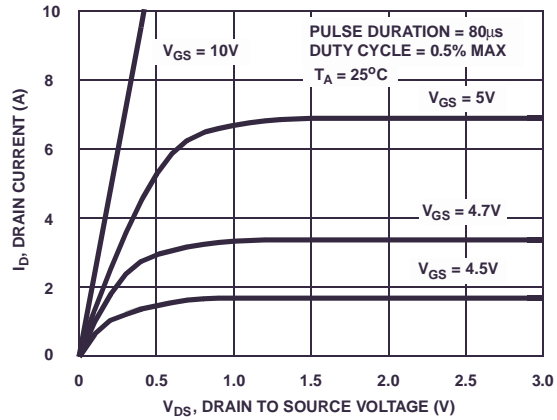
**Figure 5. Forward Bias Safe Operating Area**



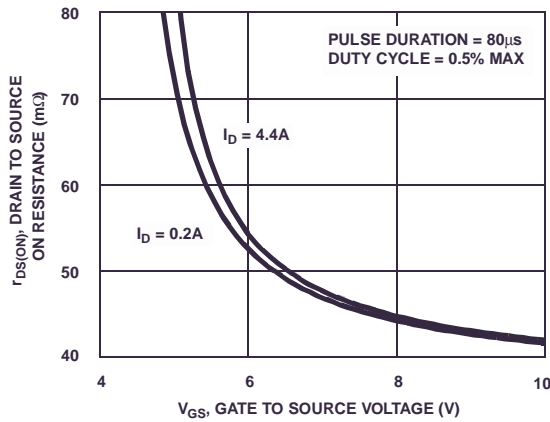
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
**Figure 6. Unclamped Inductive Switching Capability**



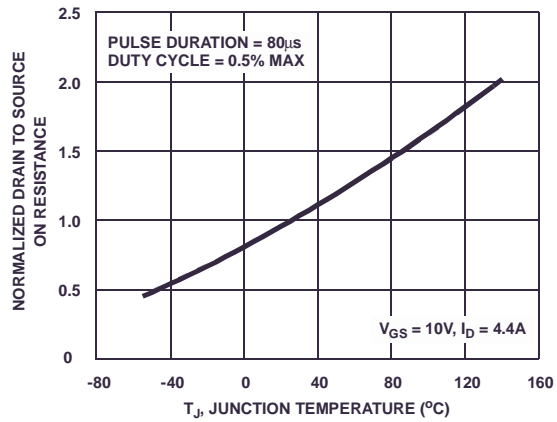
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

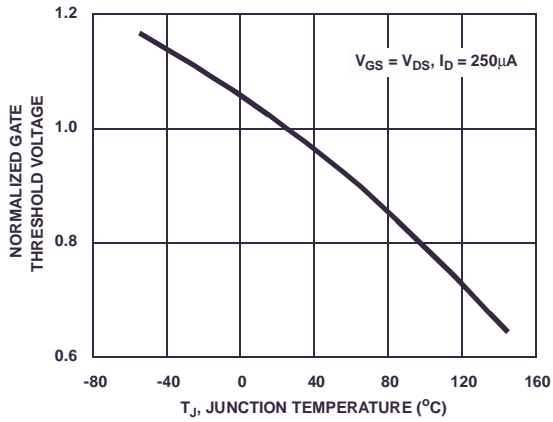


**Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current**

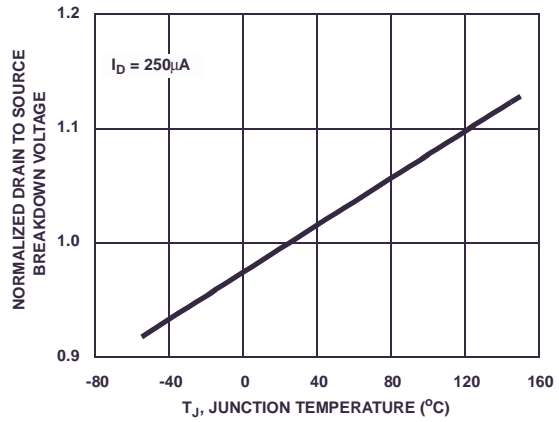


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

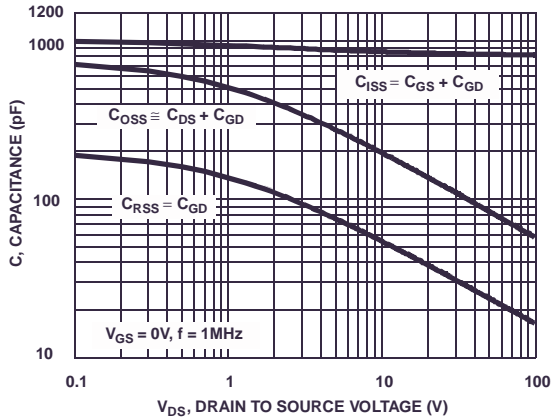
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



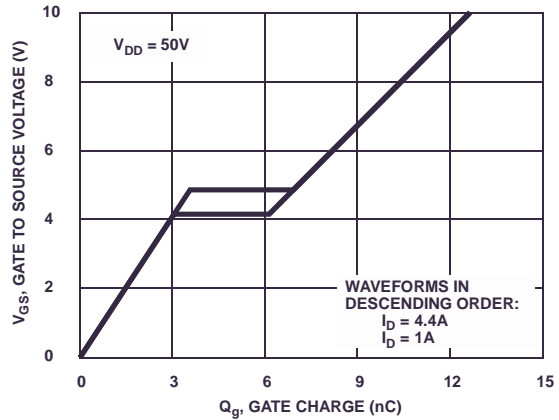
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Currents**

### Test Circuits and Waveforms

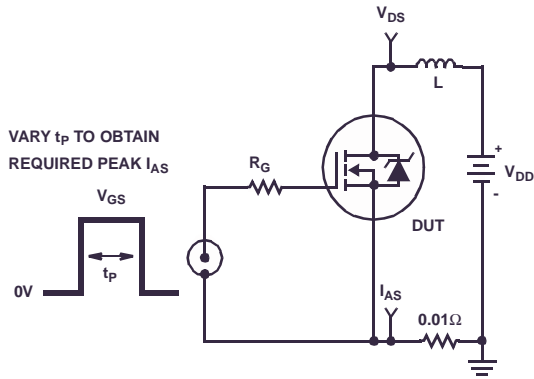


Figure 15. Unclamped Energy Test Circuit

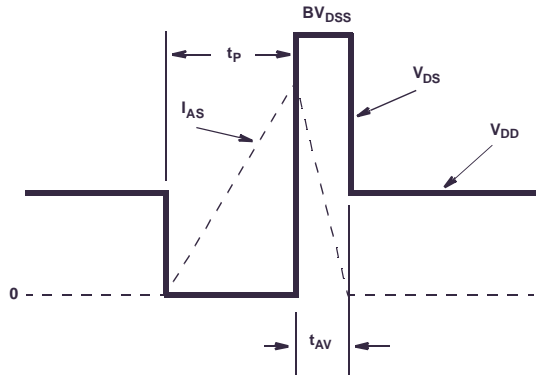


Figure 16. Unclamped Energy Waveforms

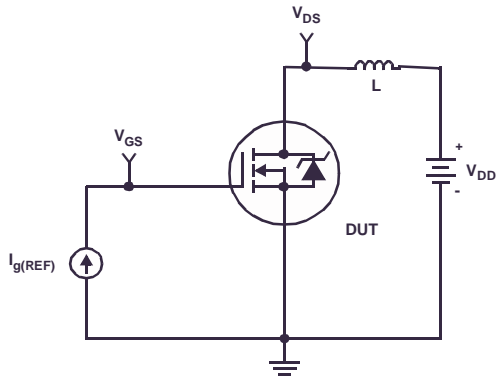


Figure 17. Gate Charge Test Circuit

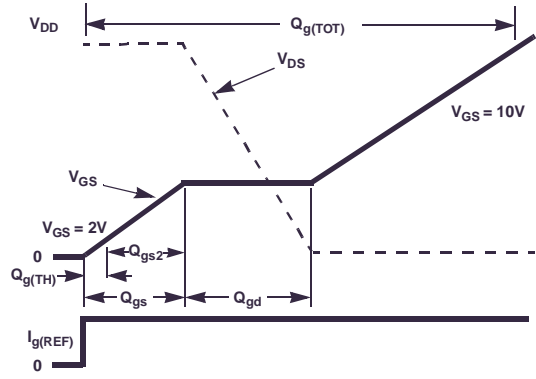


Figure 18. Gate Charge Waveforms

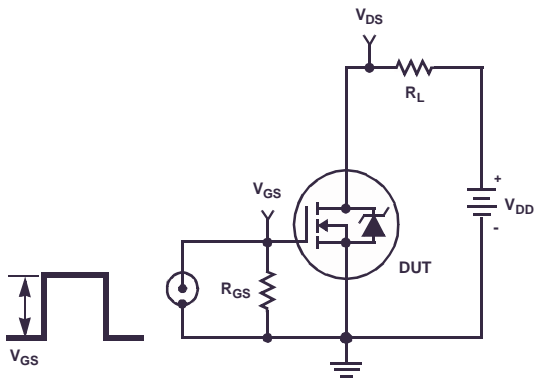


Figure 19. Switching Time Test Circuit

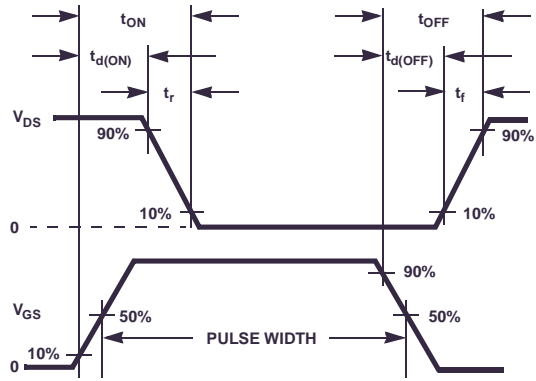


Figure 20. Switching Time Waveforms

**PSPICE Electrical Model**

.SUBCKT FDM3622 2 1 3 ; rev October 2004  
 Ca 12 8 2.5e-10  
 Cb 15 14 2.5e-10  
 Cin 6 8 8e-10

Dbody 7 5 DbodyMOD  
 Dbreak 5 11 DbreakMOD  
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 109  
 Eds 14 8 5 8 1  
 Egs 13 8 6 8 1  
 Esg 6 10 6 8 1  
 Evthres 6 21 19 8 1  
 Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 1.06e-9  
 Ldrain 2 5 1.0e-9  
 Lsource 3 7 0.19e-9

RLgate 1 9 10.6  
 RLdrain 2 5 10  
 RLsource 3 7 1.9

Mmed 16 6 8 8 MmedMOD  
 Mstro 16 6 8 8 MstroMOD  
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
 Rdrain 50 16 RdrainMOD 9e-3  
 Rgate 9 20 3.16  
 RSLC1 5 51 RSLCMOD 1.0e-6  
 RSLC2 5 50 1.0e3  
 Rsource 8 7 RsourceMOD 27.7e-3  
 Rvthres 22 8 RvthresMOD 1  
 Rvtemp 18 19 RvtempMOD 1  
 S1a 6 12 13 8 S1AMOD  
 S1b 13 12 13 8 S1BMOD  
 S2a 6 15 14 13 S2AMOD  
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*70),2.5))}}

.MODEL DbodyMOD D (IS=1.2E-12 RS=9.4e-3 TRS1=2.0e-3 TRS2=4.5e-7  
 + CJO=5.5e-10 M=0.56 TT=4.4e-8 XT1=4.0)

.MODEL DbreakMOD D (RS=0.6 TRS1=1.4e-3 TRS2=-5e-5)

.MODEL DplcapMOD D (CJO=2.0e-10 IS=1.0e-30 N=10 M=0.54)

.MODEL MmedMOD NMOS (VTO=3.58 KP=2.8 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.16)

.MODEL MstroMOD NMOS (VTO=4.26 KP=32 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=3.12 KP=0.04 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=31.6 RS=0.1)

.MODEL RbreakMOD RES (TC1=1.05e-3 TC2=-1.1e-8)

.MODEL RdrainMOD RES (TC1=3.0e-2 TC2=5e-5)

.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=2.9e-6)

.MODEL RsourceMOD RES (TC1=1.0e-3 TC2=1.0e-6)

.MODEL RvthresMOD RES (TC1=-3.9e-3 TC2=-1.4e-5)

.MODEL RvtempMOD RES (TC1=-3.4e-3 TC2=1.8e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.0 VOFF=-2.0)

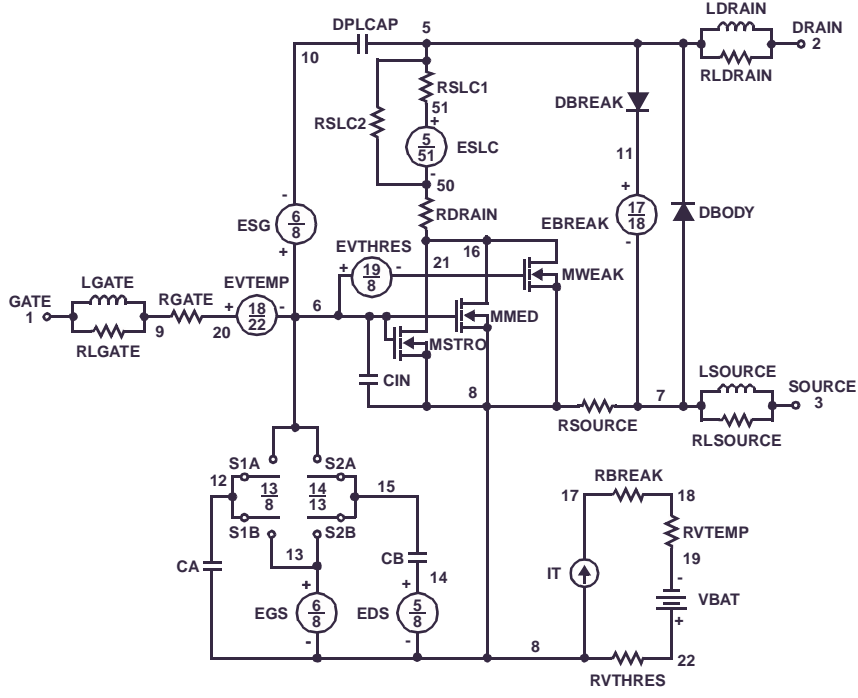
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-6.0)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





## SABER Electrical Model

REV October 2004

ttemplate FDM3622 n2,n1,n3

electrical n2,n1,n3

```

{
var i iscl
dp..model dbodymod = (isl=1.2e-12,rs=9.4e-3,trs1=2.0e-3,trs2=4.5e-7,cjo=5.5e-10,m=0.56,tt=4.4e-8,xti=4.0)
dp..model dbreakmod = (rs=0.6,trs1=1.4e-3,trs2=-5.0e-5)
dp..model dplcapmod = (cjo=2.0e-10,isl=10.0e-30,nl=10,m=0.54)
m..model mmedmod = (type=_n,vto=3.58,kp=2.8,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.26,kp=32,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.12,kp=0.04,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-6.0,voff=-2.0)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2.0,voff=-6.0)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.5,voff=0.3)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.3,voff=-0.5)
c.ca n12 n8 = 2.5e-10
c.cb n15 n14 = 2.5e-10
c.cin n6 n8 = 8e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 109
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 1.06e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 0.19e-9

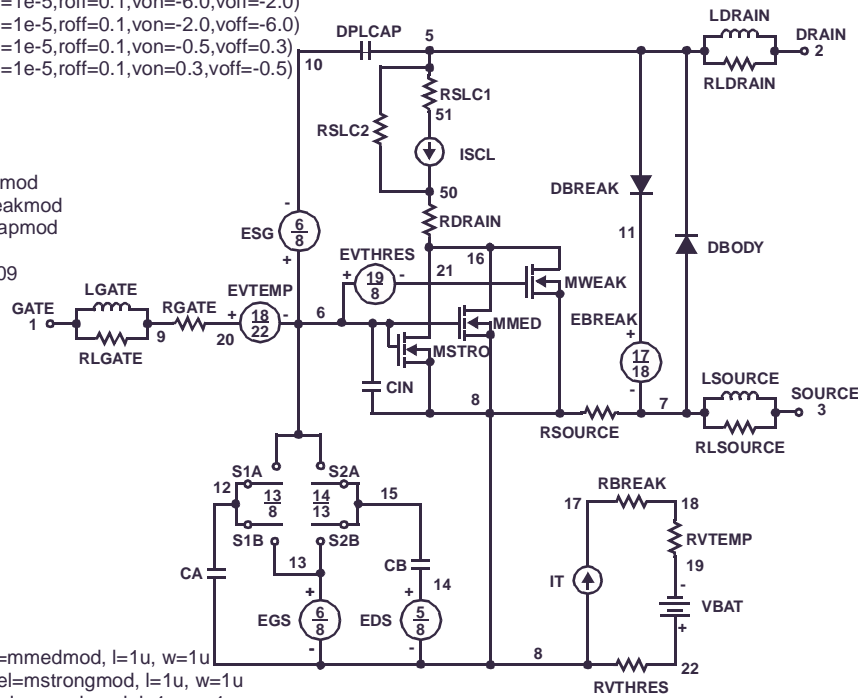
res.rlgate n1 n9 = 10.6
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 1.9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1.05e-3,tc2=-1.1e-8
res.rdrain n50 n16 = 9e-3, tc1=3.0e-2,tc2=5e-5
res.rgate n9 n20 = 3.16
res.rslc1 n5 n51 = 1.0e-6, tc1=3.0e-3,tc2=2.9e-6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7 = 27.7e-3, tc1=1.0e-3,tc2=1.0e-6
res.rvthres n22 n8 = 1, tc1=-3.9e-3,tc2=-1.4e-5
res.rvtemp n18 n19 = 1, tc1=-3.4e-3,tc2=1.8e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = (((n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/70)** 2.5))
}
}

```



**SPICE Thermal Model**

REV October 2004

FDM3622\_JA Junction Ambient  
Copper Area = 1sq.in

CTHERM1 TH c2 1.1e-4  
CTHERM2 c2 c3 1.2e-4  
CTHERM3 c3 c4 3.0e-4  
CTHERM4 c4 c5 2.0e-3  
CTHERM5 c5 c6 6.4e-3  
CTHERM6 c6 c7 3.2e-2  
CTHERM7 c7 c8 2.9e-1  
CTHERM8 c8 Ambient 3

RTHERM1 TH c2 2.0e-2  
RTHERM2 c2 c3 1.3e-1  
RTHERM3 c3 c4 2.0e-1  
RTHERM4 c4 c5 1.1  
RTHERM5 c5 c6 3.3  
RTHERM6 c6 c7 6.8  
RTHERM7 c7 c8 12.2  
RTHERM8 c8 Ambient 27

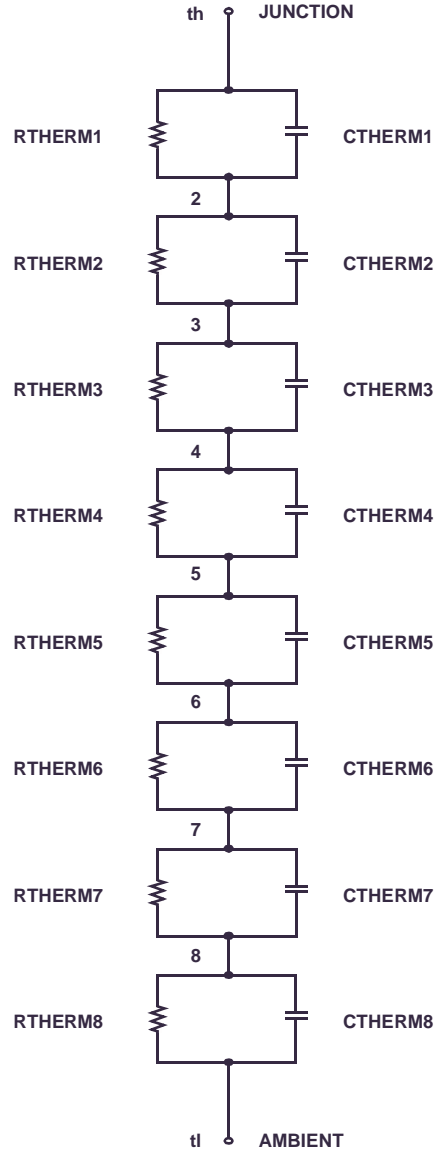
**SABER Thermal Model**

SABER thermal model FDM3622

Copper Area = 1sq.in  
template thermal\_model th tl  
thermal\_c th, tl

```
{
ctherm.ctherm1 th c2 =1.1e-4
ctherm.ctherm2 c2 c3 =1.2e-4
ctherm.ctherm3 c3 c4 =3.0e-4
ctherm.ctherm4 c4 c5 =2.0e-3
ctherm.ctherm5 c5 c6 =6.4e-3
ctherm.ctherm6 c6 c7 =3.2e-2
ctherm.ctherm7 c7 c8 =2.9e-1
ctherm.ctherm8 c8 tl =3

rrtherm.rtherm1 th c2 =2.0e-2
rtherm.rtherm2 c2 c3 =1.3e-1
rtherm.rtherm3 c3 c4 =2.0e-1
rtherm.rtherm4 c4 c5 =1.1
rtherm.rtherm5 c5 c6 =3.3
rtherm.rtherm6 c6 c7 =6.8
rtherm.rtherm7 c7 c8 =12.2
rtherm.rtherm8 c8 tl =27
}
```



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Bottomless™	FASTr™	ISOPLANAR™	PowerEdge™	SuperSOT™-3
CoolFET™	FPST™	LittleFET™	PowerSaver™	SuperSOT™-6
CROSSVOLT™	FRFET™	MICROCOUPLER™	PowerTrench®	SuperSOT™-8
DOME™	GlobalOptoisolator™	MicroFET™	QFET®	SyncFET™
EcoSPARK™	GTO™	MicroPak™	QS™	TinyLogic®
E <sup>2</sup> CMOS™	HiSeC™	MICROWIRE™	QT Optoelectronics™	TINYOPTO™
EnSigna™	I <sup>2</sup> C™	MSX™	Quiet Series™	TruTranslation™
FACT™	<i>i-Lo</i> ™	MSXPro™	RapidConfigure™	UHC™
		OCX™	RapidConnect™	UltraFET®
Across the board. Around the world.™		OCXPro™	µSerDes™	UniFET™
The Power Franchise®		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	
		PACMAN™	SPM™	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.