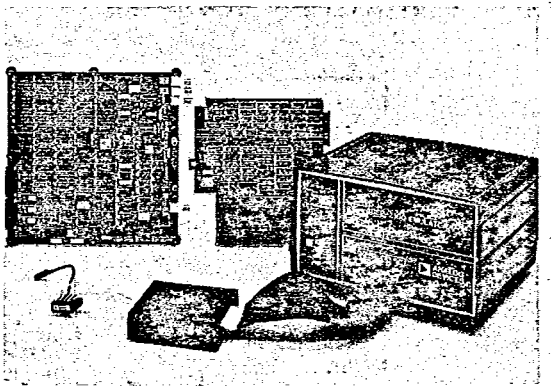
T-49-05

# DSP Hardware Development Tools

## ADDS-21XX





### FEATURES

**ADSP-2100A EVALUATION BOARD**

- Can Be Used to Benchmark Real-Time Performance
- Interfaces to an IBM-PC or VAX Host via RS-232 Connectors
- Operates at 8MHz
- Same Interactive, Symbolic User Interface as the Emulator and Simulator
- Three Execution Modes: Single-Step, Extend, Emulator
- Displays Contents of ADSP-2100A Registers, Program Memory, Data Memory and Stack
- Multiple Program Memory Breakpoints Supported
- 4K Program and 2K Data Memory Installed with Sockets for Expanding to Full 32K Program and 16K Data Memory
- Fully Documented Prototyping Expansion Connector to Customize Evaluation Board to Your Application
- Bidirectional Codec Channel to Process Real-World Signals
- 12-Bit Linear DAC Provides an Oscilloscope Interface
- Input Preamp with Microphone Jack and Output Amplifier with Speaker Jack Directly Supports Audio and Speech Applications

**ADSP-2100A IN-CIRCUIT EMULATOR**

- Performs In-Circuit Emulation
- Interfaces to an IBM-PC or VAX Host via Two RS-232 Connectors
- Operates at 8MHz
- Same Interactive, Symbolic User Interface as the ADSP-2100 Simulator and Evaluation Board
- Three Execution Modes: Single-Step, Extend, Emulator
- Displays Contents of ADSP-2100A Registers, Program Memory, Data Memory and Stack
- Supports Multiple Program Memory Breakpoints
- User-Selectable Program Memory Source: Emulator or Target System
- User-Selectable System Clock Source: Emulator, Target System or External

**OPTIONAL TRACE BOARD FOR IN-CIRCUIT EMULATOR**

- Buffers Up To 8K of Bus Activity for Display and Analysis
- Break Triggering on an Extensive Set of Possible Bus Conditions
- Buffer Can Be Uploaded to Host for Further Analysis
- Installs Inside Emulator Case

### GENERAL DESCRIPTION

The ADSP-2100A Hardware Development Tools support the prototyping, development and debugging of applications in hardware.

The Evaluation Board allows the user to benchmark real-time performance by executing Analog Devices-supplied or user-developed DSP routines.

The In-Circuit Emulator allows the user to debug code in the actual target system.

The Trace Board enhances the In-Circuit Emulator by capturing activity on the four external buses of the processor.

The Hardware Development Tools have the same interactive, symbolic user interface as the Simulator. Single-step, extend and emulator execution modes run the processor as required for your debugging activity. Four major display modes enable users to examine contents of ADSP-2100A registers, program memory, data memory and stack. Multiple program memory breakpoints are supported.

## ADSP-2100A EVALUATION BOARD

The Evaluation Board is an easy-to-use development tool for evaluating the ADSP-2100A DSP Microprocessor in real-time applications. It has three roles in the design process. As a demonstration system, you can observe the ADSP-2100A's real-time performance in executing standard DSP benchmarks. As an evaluation system, it can be used prior to designing hardware for the real-time execution of your application routines. As a simulation accelerator, application code can be executed in real time for increased productivity of software developers.

The Evaluation Board is a stand alone system consisting of an ADSP-2100A DSP Microprocessor, 4K words of (24-bit) program memory, and 2K words of (16-bit) data memory. Additional program and data memory sockets are provided and can be populated as desired up to the full 32K program and 16K data memory address space.

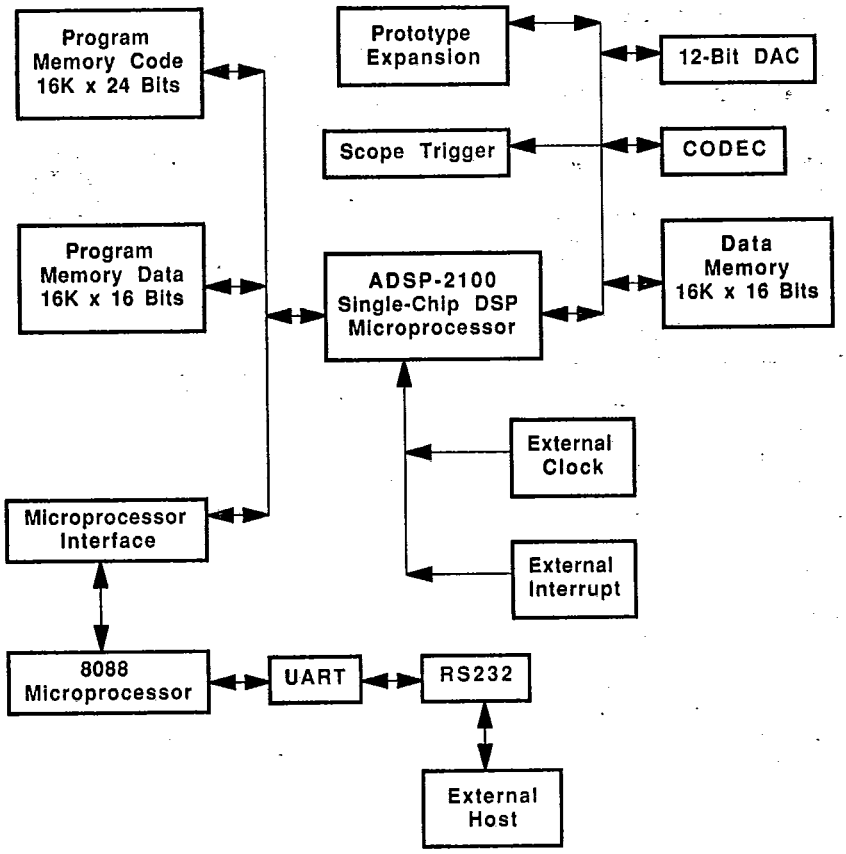



*Figure 1. Evaluation Board Block Diagram*

The Evaluation Board's ADSP-2100A runs under the control of an on-board host processor enabling the user to access a variety of powerful debugging tools. When interfaced to an external host computer system running the Cross-Software, the Evaluation Board serves as a real-time development tool.

The emulator mode runs the processor at full speed. Extend mode updates the screen every cycle during program execution. Single-step mode executes a single instruction per carriage return. In addition, multiple program memory breakpoints are supported.

The Evaluation Board has four major display modes: register, program memory, data memory and stack. Register mode displays the contents of the ADSP-2100A's primary and alternate registers. Program memory mode displays the contents of program memory. Data memory mode displays the contents of data memory. Stack display shows the contents of the ADSP-2100A's program counter stack and count stack.

The Evaluation Board connects to a terminal and host computer via two RS-232C serial connectors.

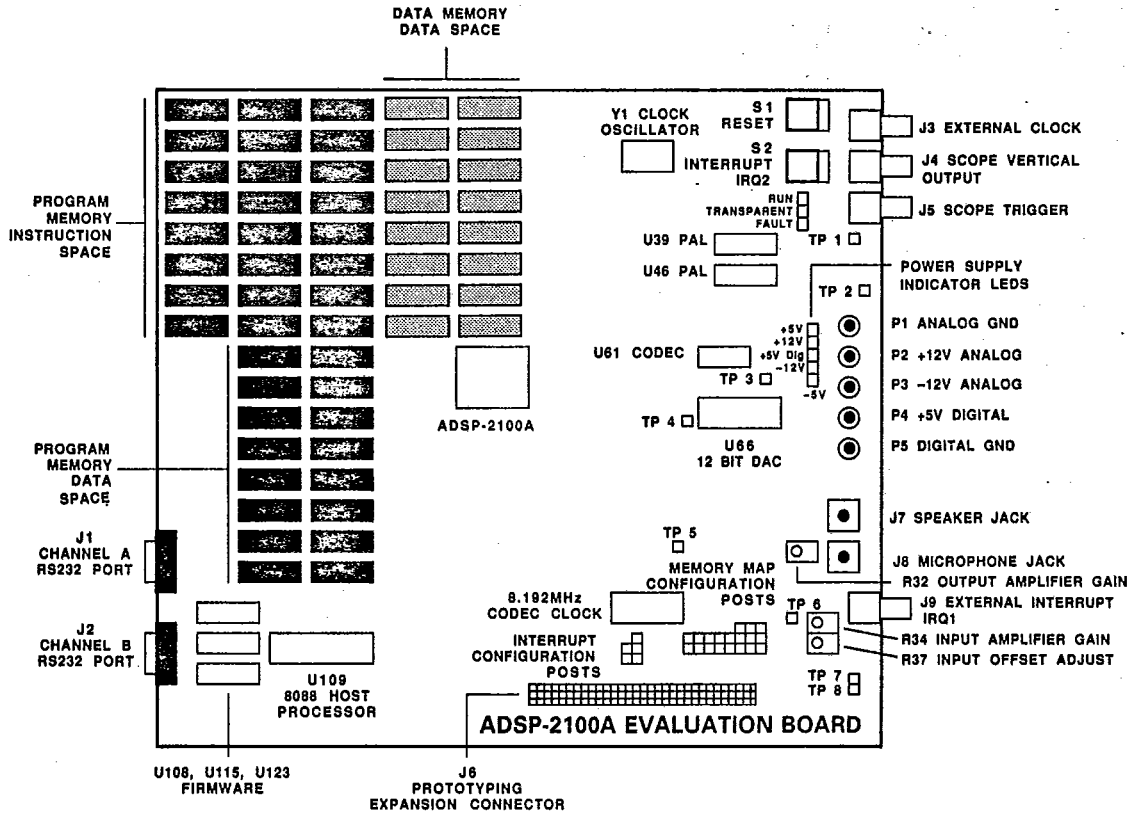



*Figure 2. Evaluation Board*

Built-in analog interfaces provide access to real signals for easy implementation of audio, speech and telecommunications applications. A bidirectional codec channel and an undedicated 12-bit linear D/A converter process real-world signals. The prototyping expansion bus allows you to construct custom hardware to reflect or test the eventual hardware environment. In addition, three BNC connectors interface to external instrumentation. An integral microphone jack and input pre-amplifier, along with a speaker jack and output amplifier, support speech and telecommunication applications.

With a microphone, speaker and oscilloscope you can easily implement audio and speech applications. The microphone and speaker are connected to the bidirectional codec channel via jacks on the input preamp and output amplifier. The codec is a National Semiconductor TP3051. It is a memory-mapped peripheral of the ADSP-2100A that can be written to or read from using the Data Memory Read and Data Memory Write commands. The codec represents the input/output sample in an 8-bit binary form. By using the standard μ-law nonlinear transformation, the codec's effective dynamic range can be extended to 13 bits. The codec samples data at a frequency of 8.192kHz using a dedicated clock generator. Communication between the codec and the ADSP-2100A is synchronized with the DMACK signal. The codec rejects signals that do not fall in the range of 200Hz to 3400Hz and should be used only in speech or audio applications in which telephone-quality signals are adequate. An input pre-amplifier (Analog Devices AD741 operational amplifier) and output audio amplifier (National Semiconductor LM338 Audio Power Amplifier) are connected to the input and output of the codec.

To display processed data, the oscilloscope is connected to the 12-bit linear DAC via a BNC connector. The DAC is an Analog Devices AD667 12-bit D/A converter. It is a memory-mapped peripheral of the ADSP-2100A that can be written using the Data Memory Write commands. The DAC is intended for use as an analog output for the display of processed data on an oscilloscope. It is not intended as a means of reconstructing sampled data processed by the ADSP-2100A; it lacks the deglitching circuitry and anti-imaging filtering required of such a system. The user can construct a linear analog interface consisting of an A/D converter, D/A converter, antialiasing filter and anti-imaging filter using the prototyping expansion connector.

The prototyping expansion connector provides the data, address and interface signals for customizing the Evaluation Board. For example, analog circuitry composed of linear A/D and D/A converters and antialiasing filters may be connected to the Evaluation Board for implementing filtering applications. The 96-contact prototyping expansion connector brings out the following signals:

**Input Signals**

| | |
|---|---|
| EIRQ3 | External Interrupt Request 3 (Highest Priority) |
| EIRQ2 | External Interrupt Request 2 |
| EIRQ1 | External Interrupt Request 1 |
| EIRQ0 | External Interrupt Request 0 |
| EBR | External Bus Request . Allows your target board to request control of the data memory interface. |
| EDMACK | Data Memory Acknowledge. Used for asynchronous transfers across the data memory interface. |
| THALT | Processor Halt by Target System. Assertion of THALT halts the ADSP-2100A. |
| RESETOUT | System Reset Output. The ADSP-2100A's RESET line is available at this contact as an output only. |

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**Output Signals**

| | |
|---|---|
| +12V | +12V Analog |
| AGND | Analog Ground |
| −12V | −12V Analog |
| GND | Digital Ground |
| $\overline{BG}$ | Bus Grant. Acknowledges an external bus request ($\overline{BR}$). |
| DMA13–0 | Data Memory Address bits |
| $\overline{DMRD}$ | Data Memory Read. Indicates a read operation on the data memory interface. |
| $\overline{DMWR}$ | Data Memory Write. Indicates a write operation on the data memory interface. |
| $\overline{DMS}$ | Data Memory Select. Signals a data memory access on the data memory interface. |
| TRAP | Indicates the execution of a TRAP instruction. The ADSP-2100A halts execution and the TRAP signal remains asserted until THALT is asserted. |
| ECE8–1 | External Chip Enables 8 through 1. These outputs are memory-mapped locations. |

**Bidirectional Signals**

| | |
|---|---|
| DMD15–0 | Data Memory Data Bus |

The Evaluation Board must be interfaced to an IBM-PC (with VT100 emulation) or VAX/VMS system via the RS-232 connectors. This host computer must also run the ADSP-2100 Cross-Software. The board requires ±12V and +5V power supplies.

## ADSP-2100A IN-CIRCUIT EMULATOR

The In-Circuit Emulator allows you to debug code (developed with the Software Development tools) in the actual target system. The Emulator uses an ADSP-2100A to emulate the processor. It plugs into the target system's ADSP-2100A socket and operates at the ADSP-2100A's cycle rate. The Emulator provides a software interface similar to the Cross-Software Simulator and to the Evaluation Board.

Once your program has been debugged in the software environment you can further prove and debug in the hardware area using the Emulator. It provides a variety of ways to download your program into the actual hardware, executing out of emulator program memory or target system program memory, for example, or using any of three sources for the system clock.

The Emulator supports three execution modes. In emulator mode the Emulator runs at the full processor speed and halts only when a break condition is encountered. Break conditions include breakpoints, traps, halt on keyboard interrupt and target system voltage below 4.5V. While the Emulator is running in emulator mode, only the program counter and elapsed time information is updated. When the Emulator halts, the full screen is updated.

Extend mode runs the processor in a continuous single-step manner, updating the display after each processor cycle. Instructions are disassembled on the screen as they are executed. In emulator and extend modes, emulation can be halted by setting a breakpoint at a specified location in program memory.

In single-step mode, the Emulator executes one instruction and halts. All display contents are updated and instructions are disassembled as they are executed. The next instruction is executed if you type a carriage return or enter the RUN command.

The Emulator has four major display modes (five with the Trace Board installed). Register display shows the contents of the ADSP-2100A's primary and secondary registers. The program memory and data memory displays show the contents of program and data memories. Stack display shows the contents of the ADSP-2100A's program counter stack and count stack.

Using the same interactive, symbolic user interface as the Simulator, the Emulator allows the user to modify the contents of registers, program memory, data memory and the program counter. Breakpoints can be set in the emulator-based program memory. User-defined addresses and values can be displayed symbolically. Numbers can be specified and displayed in either decimal or hexadecimal format.

The Emulator has other features. The baud rate and parity settings for communications between the Emulator and the host computer can be specified by the user's terminal. The Emulator Pod can be activated and deactivated under software control. The program memory source can be either the Emulator's internal program memory RAM or the target system's program memory. Also, files can be downloaded from the host system. The system clock can be selected from either the Emulator's internal clock, the target system's clock or an external clock generator.

### Propagation Delays

Although the Emulator matches the ADSP-2100A closely in performance for a few signals, its timing is degraded somewhat from that of the processor. Propagation delays and, in some cases, software overhead account for the delays. The signals with degraded timing are:

- CLKIN
- $\overline{\text{IRQ}}$
- $\overline{\text{BR}}$
- $\overline{\text{RESET}}$
- $\overline{\text{HALT}}$
- TRAP
- $\overline{\text{PMWR}}$ and $\overline{\text{PMRD}}$

All other signals operate at essentially the same timing as the processor in a non-emulator system. Complete information and timing diagrams are given in Appendix B of the *ADSP-2100 Emulator Manual*.

## TRACE BOARD FOR ADSP-2100A IN-CIRCUIT EMULATOR

The Emulator supports an optional, factory-installed Trace Board. The Trace Board keeps a running history of past external bus states PMA, DMA and DMD in an 8K buffer. The Trace Buffer Display shows the past external bus states of the ADSP-2100A.

The Trace Board allows you to trigger on bus conditions. Emulation can be halted after detecting a specified combination of bus states. The IGNORE option turns off the trace during certain PMA ranges in order to skip over sections of code. The Trace Board can trigger on the following eleven different bus combinations:

PMA AND DMA
PMA AND DMD
DMA AND DMD
PMA AND DMA AND DMD
PMA OR (DMA AND DMD)
DMA OR (PMA AND DMD)
DMD OR (PMA AND DMA)
PMA OR DMA OR DMD
(PMA AND DMA) OR (PMA AND DMD)
(PMA AND DMA) OR (DMA AND DMD)
(PMA AND DMA) OR (DMA AND DMD)

In addition, the trace buffer can be uploaded from trace board to host computer.

## ADDITIONAL INFORMATION

Request the *ADSP-2100 Emulator Manual* or the *ADSP-2100 Evaluation Board Manual* from your Analog Devices Sales Engineer for further information.

**ORDERING INFORMATION**

| Part Number | Description |
|---|---|
| ADDS-2150A* | 8MHz ADSP-2100A In-Circuit Emulator (110V) |
| ADDS-2150AE* | 8MHz ADSP-2100A In-Circuit Emulator (220V) |
| ADDS-2151A* | 8MHz ADSP-2100A In-Circuit Emulator with Trace Board (110V) |
| ADDS-2151AE* | 8MHz ADSP-2100A In-Circuit Emulator with Trace Board (220V) |
| ADDS-2160* | 8MHz ADSP-2100A Evaluation Board |
| *Upgrade Kits* | |
| ADDS-2161 | Trace Board Upgrade for ADDS-2150 |
| ADDS-2162 | Trace Board Upgrade for ADDS-2150A |

*A 12.5MHz version of this product is planned. Please contact factory for further information.