NEC

MOS INTEGRATED CIRCUIT

μPD780053,780054,780055,780056,780058

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780053,780054,780055,780056 and 780058 are members of the μPD780058 subseries in the 78K/0 series. These microcontrollers suppress the EMI (Electro Magnetic Interference) noise internally generated to the lower level than the existing μPD78054 subseries. In addition, they have many peripheral hardware units such as an 8-bit resolution A/D converter, 8-bit resolution D/A converter, timers, serial interface, real-time output ports, and interrupt functions.

A flash memory model that can operate on the same voltage as the mask ROM models, μPD78F0058, and various development tools are now under development.

The funcitons are explaned in detail in the following User's Manuals. Be sure to read these manuals when designing your system.

μPD780058, 780058Y Subseries User's Manual : U12013E
78K/0 Series User's Manual - Instruction : U12326E

FEATURES

- Internal high-capacity ROM & RAM

Item / Part Number	Program Memory (ROM)	Data Memory		
		Internal high-speed RAM	Internal buffer RAM	Internal expanded RAM
μPD780053	24K bytes	1024 bytes	32 bytes	None
μPD780054	32K bytes			
μPD780055	40K bytes			
μPD780056	48K bytes			
μPD780058	60K bytes			1024 bytes

- External memory expansion space: 64K bytes
- Minimum instruction execution time changeable from high speed (0.4 μs) to ultra low-speed (122 μs)
- I/O ports: 68 pins (N-ch open-drain : 4 pins)
- 8-bit resolution A/D converter : 8 channels (V_{DD} = 2.7 to 5.5 V)
- 8-bit resolution D/A converter : 2 channels (V_{DD} = 2.7 to 5.5 V)
- Serial interface : 3 channels
- Timer : 5 channels
- Operating voltage range : V_{DD} = 1.8 to 5.5 V

APPLICATION FIELDS

Car audio systems, cellular phones, pagers, printers, AV systems, cameras, PPCs, and vending machines

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

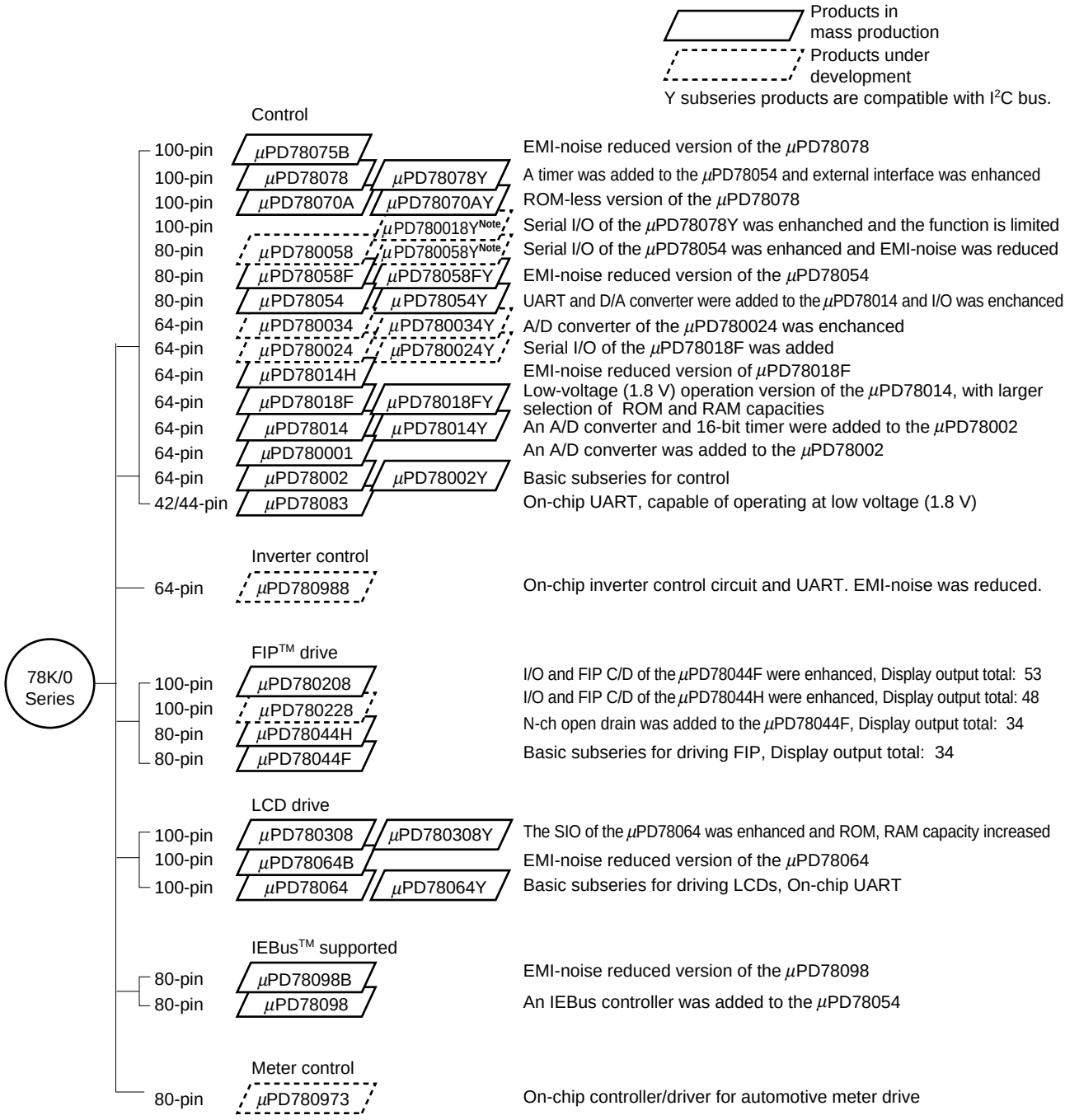
★ ORDERING INFORMATION

Part Number	Package
μPD780053GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD780053GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD780054GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD780054GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD780055GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD780055GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD780056GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD780056GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD780058GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD780058GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Remark ××× indicates ROM code suffix.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The following shows the 78K/0 Series products development. Subseries name are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K - 40K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART : 1ch)	88	1.8 V	○
	μPD78078	48 K - 60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K - 60 K	2ch							3ch (time division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K - 60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K - 60 K										2.0 V	
	μPD780034	8 K - 32 K					–	8ch	–	3ch (UART: 1ch, time division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53		
	μPD78018F	8 K - 60 K											
	μPD78014	8 K - 32 K										2.7 V	
	μPD780001	8 K		–	–					1ch	39		–
	μPD78002	8 K - 16 K			1ch		–				53		○
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
★ Inverter control	μPD780988	32 K - 60 K	3ch	**Note**	–	1ch	–	8ch	–	3ch (UART: 2ch)	47	4.0 V	○
FIP drive	μPD780208	32 K - 60 K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48 K - 60 K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32 K - 48 K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16 K - 40 K								2ch			
LCD drive	μPD780308	48 K - 60 K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time division UART: 1ch)	57	2.0 V	–
	μPD78064B	32 K								2ch (UART : 1 ch)			
	μPD78064	16 K - 32 K											
IEBus supported	μPD78098B	40 K - 60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART : 1 ch)	69	2.7 V	○
	μPD78098	32 K - 60 K											
LV	μPD78P0914	32 K	6ch	–	–	1ch	8ch	–	–	2ch	54	4.5 V	○

Note 16-bit timer : 2 channels
10-bit timer : 1 channel

OVERVIEW OF FUNCTION

Item \ Product Name		μPD780053	μPD780054	μPD780055	μPD780056	μPD780058
Internal memory	ROM	24K bytes	32K bytes	40K bytes	48K bytes	60K bytes
	High-speed RAM	1024 bytes				
	Buffer RAM	32 bytes				
	Expanded RAM	None				1024 bytes
Memory space		64 K bytes				
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function				
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz operation)				
	When subsystem clock selected	122 μs (at 32.768 kHz operation)				
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.				
I/O ports		Total : 68 • CMOS input : 2 • CMOS I/O : 62 • N-ch open-drain I/O : 4				
A/D converter		• 8-bit resolution × 8 channels (V_{DD} = 2.7 to 5.5 V)				
D/A converter		• 8-bit resolution × 2 channels (V_{DD} = 2.7 to 5.5 V)				
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel • 3-wire serial I/O mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel • 3-wire/serial I/O/UART mode (on-chip time division transfer function) selectable: 1 channel				
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel				
Timer output		3 (14-bit PWM output × 1)				
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock: 5.0 MHz operation) 32.768 kHz (at subsystem clock: 32.768 kHz operation)				
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock: 5.0 MHz operation)				
★ Vectored interrupt sources	Maskable	Internal interrupt : 13, external interrupt : 6				
	Non-maskable	Internal interrupt : 1				
	Software	1				
Test input		Internal : 1, external : 1				
Supply voltage		V_{DD} = 1.8 to 5.5 V				
Operating ambient temperature		T_A = –40 to +85°C				
★ Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)				

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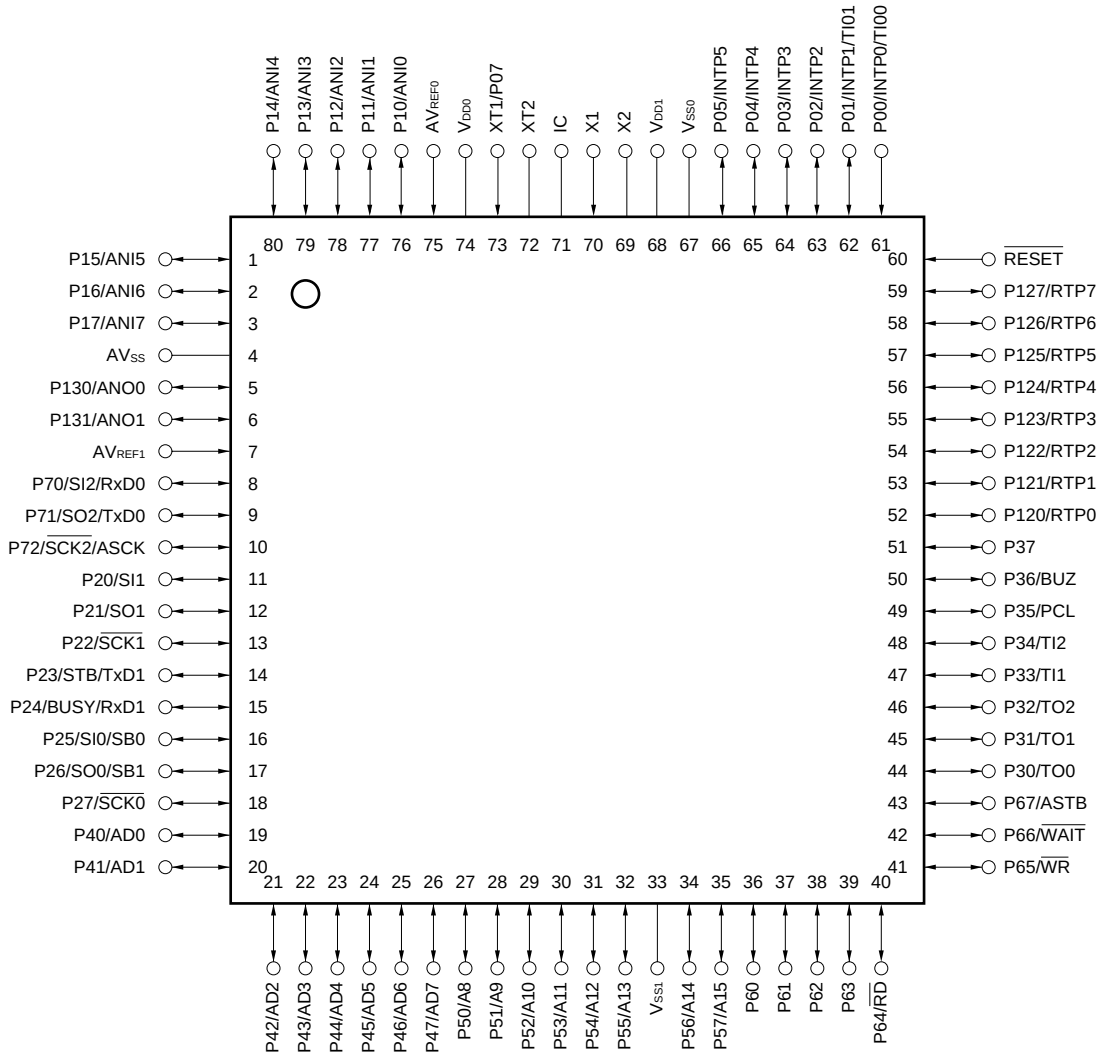
1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD780053GC-×××-8BT, 780054GC-×××-8BT, 780055GC-×××-8BT, 780056GC-×××-8BT, 780058GC-×××-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD780053GK-×××-BE9, 780054GK-×××-BE9, 780055GK-×××-BE9, 780056GK-×××-BE9, 780058GK-×××-BE9



Cautions 1. Directly connect the IC (Internally Connected) pins to V_{SS0} or V_{SS1}.

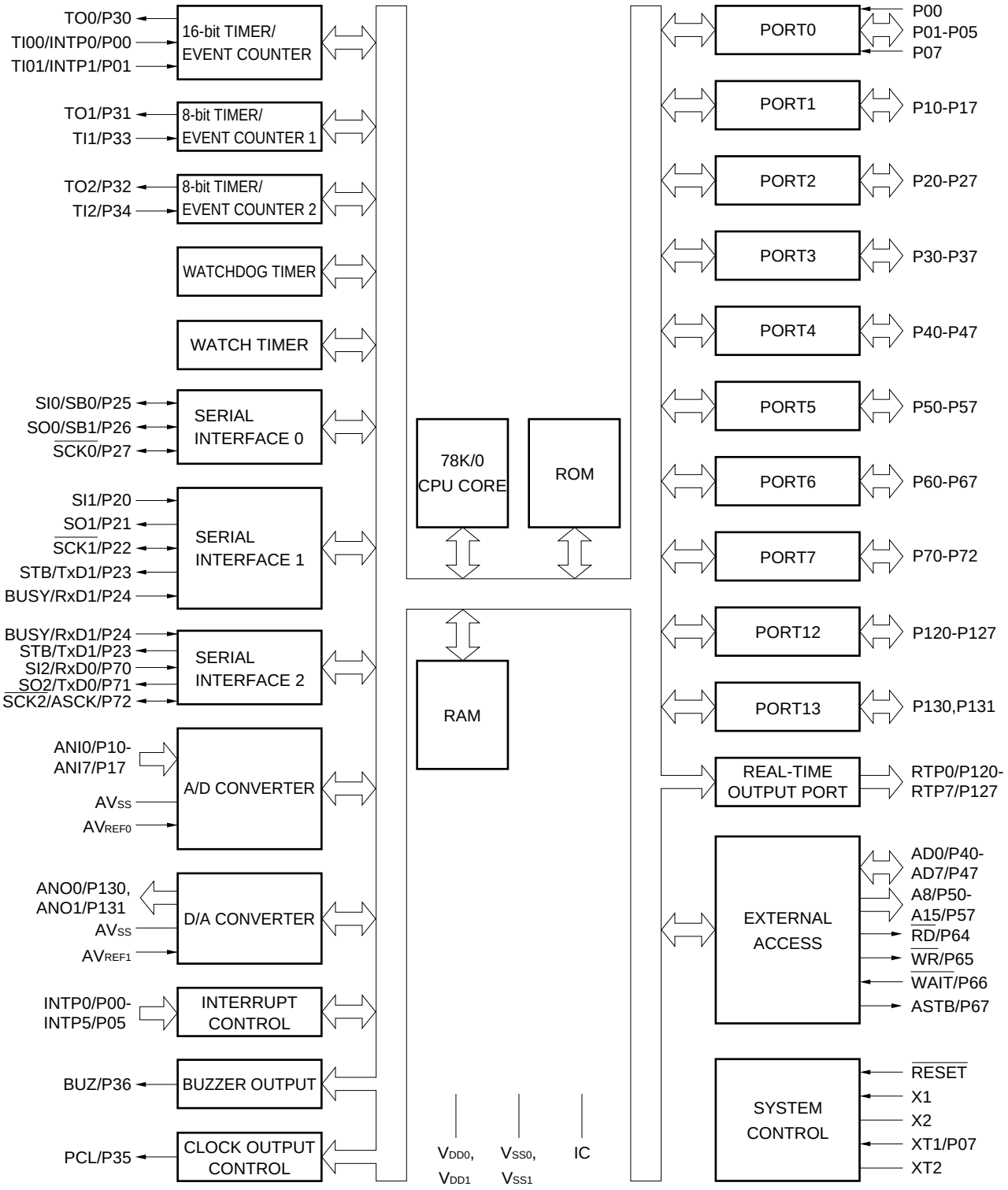
2. Connect the AV_{SS} pin to V_{SS0}.

Remarks 1. ××× indicates ROM code suffix.

2. If the microcontroller is used in an application where the noise generated from the microcontroller must be suppressed, it is recommended that power be supplied to V_{DD0} and V_{DD1} from separate sources, and that V_{SS0} and V_{SS1} be connected to separate group lines, to improve noise immunity.

A8-A15	:	Address Bus
AD0-AD7	:	Address/Data Bus
ANI0-ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
ASCK	:	Asychronous Serial Clock
ASTB	:	Address Strobe
$AV_{REF0, 1}$	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
BUSY	:	Busy
BUZ	:	Buzzer Clock
IC	:	Internally Connected
INTP0-INTP5	:	Interrupt from Peripherals
P00-P05, P07	:	Port0
P10-P17	:	Port1
P20-P27	:	Port2
P30-P37	:	Port3
P40-P47	:	Port4
P50-P57	:	Port5
P60-P67	:	Port6
P70-P72	:	Port7
P120-P127	:	Port12
P130, P131	:	Port13
PCL	:	Programmable Clock
$\overline{RD}$	:	Read Strobe
$\overline{RESET}$	:	Reset
RTP0-RTP7	:	Real-Time Output Port
RxD0, RxD1	:	Receive Data
SB0, SB1	:	Serial Bus
$\overline{SCK0}$-$\overline{SCK2}$	:	Serial Clock
SI0-SI2	:	Serial Input
SO0-SO2	:	Serial Output
STB	:	Strobe
TI00, TI01	:	Timer Input
TI1, TI2	:	Timer Input
TO0-TO2	:	Timer Output
TxD0, TxD1	:	Transmit Data
V_{DD0}, V_{DD1}	:	Power Supply
V_{SS0}, V_{SS1}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities differ depending on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 7-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07[Note 1]	Input		Input only	Input	XT1
P10-P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software[Note 2].		Input	ANI0-ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB/TxD1
P24					BUSY/RxD1
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40-P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0-AD7

Notes 1. When using the P07/XT1 pins as an input port, set 1 in the bit 6 (FRC) of the processor clock control register (PCC). On-chip feedback resistor of the subsystem clock oscillator should not be used.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, set port 1 to input mode. Use of the on-chip pull-up resistor is cancelled automatically.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50-P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	A8-A15
P60	Input/output	Port 6 8-bit input/outport port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be used by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, on-chip pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI2/RxD0
P71					SO2/TxD0
P72					$\overline{SCK2}$/ASCK
P120-P127	Input/output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	RTP0-RTP7
P130, P131	Input/output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	ANO0, ANO1

3.2 OTHER PINS (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt request input for which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/ output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/ output	Serial interface serial clock input/ output	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23/TxD1
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24/RxD1
RxD0	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
RxD1				P24/BUSY
TxD0	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
TxD1				P23/STB
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0-RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120-P127
AD0-AD7	Input/ output	Low-order address/data bus at external memory expansion.	Input	P40-P47
A8-A15	Output	High-order address bus at external memory expansion.	Input	P50-P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65

3.2 OTHER PINS (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 to access external memory.	Input	P67
ANI-ANI7	Input	A/D converter analog input.	Input	P10-P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input (dual-function as analog power supply).	—	—
AV_{REF1}	Input	D/A converter reference voltage input.	—	—
AV_{SS}	—	A/D converter, D/A converter ground potential. Use at the same potential as V_{SS0}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD0}	—	Port block positive power supply.	—	—
V_{SS0}	—	Port block ground potential.	—	—
V_{DD1}	—	Positive power supply (except for port and analog blocks).	—	—
V_{SS1}	—	Ground potiential (except for port and analog blocks).	—	—
IC	—	Internally connected. Connect to V_{SS0} or V_{SS1} directly.	—	—

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0/TI00	2	Input	Connect to V_{SS0}.
P01/INTP1/TI01	8-C	Input/output	Independently connect to V_{SS0} through resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{DD0}.
P10/ANI0-P17/ANI7	11-D	Input/output	Independently connect to V_{DD0} or V_{SS0} through resistor.
P20/SI1	8-C		
P21/SO1	5-H		
P22/$\overline{SCK1}$	8-C		
P23/STB/TxD1	5-H		
P24/BUSY/RxD1	8-C		
P25/SI0/SB0	10-B		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-H		
P31/TO1			
P32/TO2			
P33/TI1	8-C		
P34/TI2			
P35/PCL	5-H		
P36/BUZ			
P37			
P40/AD0-P47/AD7	5-N		Independently connect to V_{DD0} through resistor.
P50/A8-P57/A15	5-H		Independently connect to V_{DD0} or V_{SS0} through resistor.
P60-P63	13-J		Independently connect to V_{DD0} through resistor.
P64/$\overline{RD}$	5-H		Independently connect to V_{DD0} or V_{SS0} through resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when Not Used
P70/SI2/RxD0	8-C	Input/ output	Independently connect to V_{DD0} or V_{SS0} through resistor.
P71/SO2/TxD0	5-H		
P72/$\overline{SCK2}$/ASCK	8-C		
P120/RTP0- P127/RTP7	5-H		
P130/ANO0 , P131/ANO1	12-C		Independently connect to V_{SS0} through resistor.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS0}.
AV_{REF1}			Connect to V_{DD0}.
AV_{SS}			Connect to V_{SS0}.
IC			Connect to V_{SS0} or V_{SS1} directly.

Figure 3-1. Pin Input/Output Circuits (1/2)

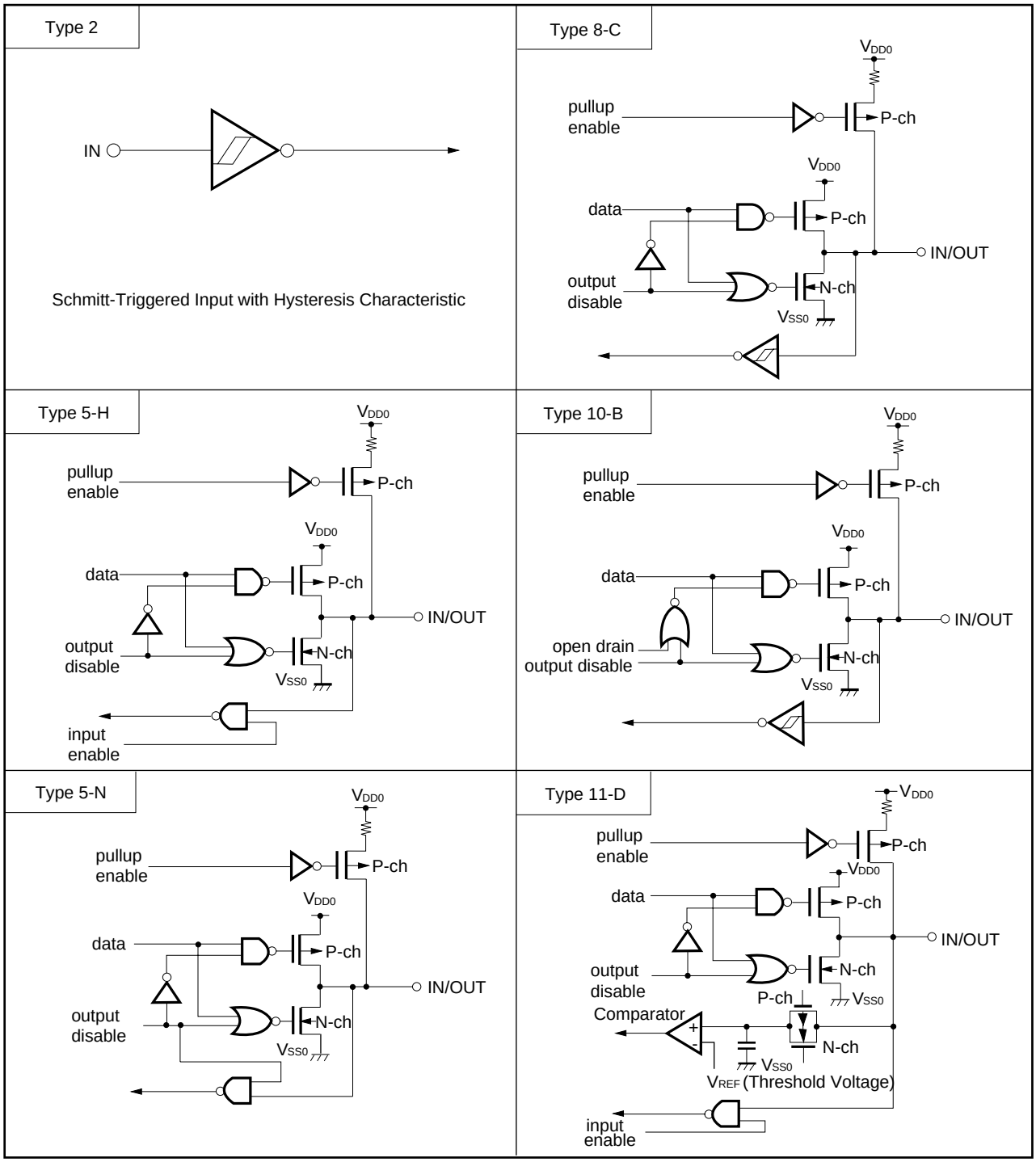
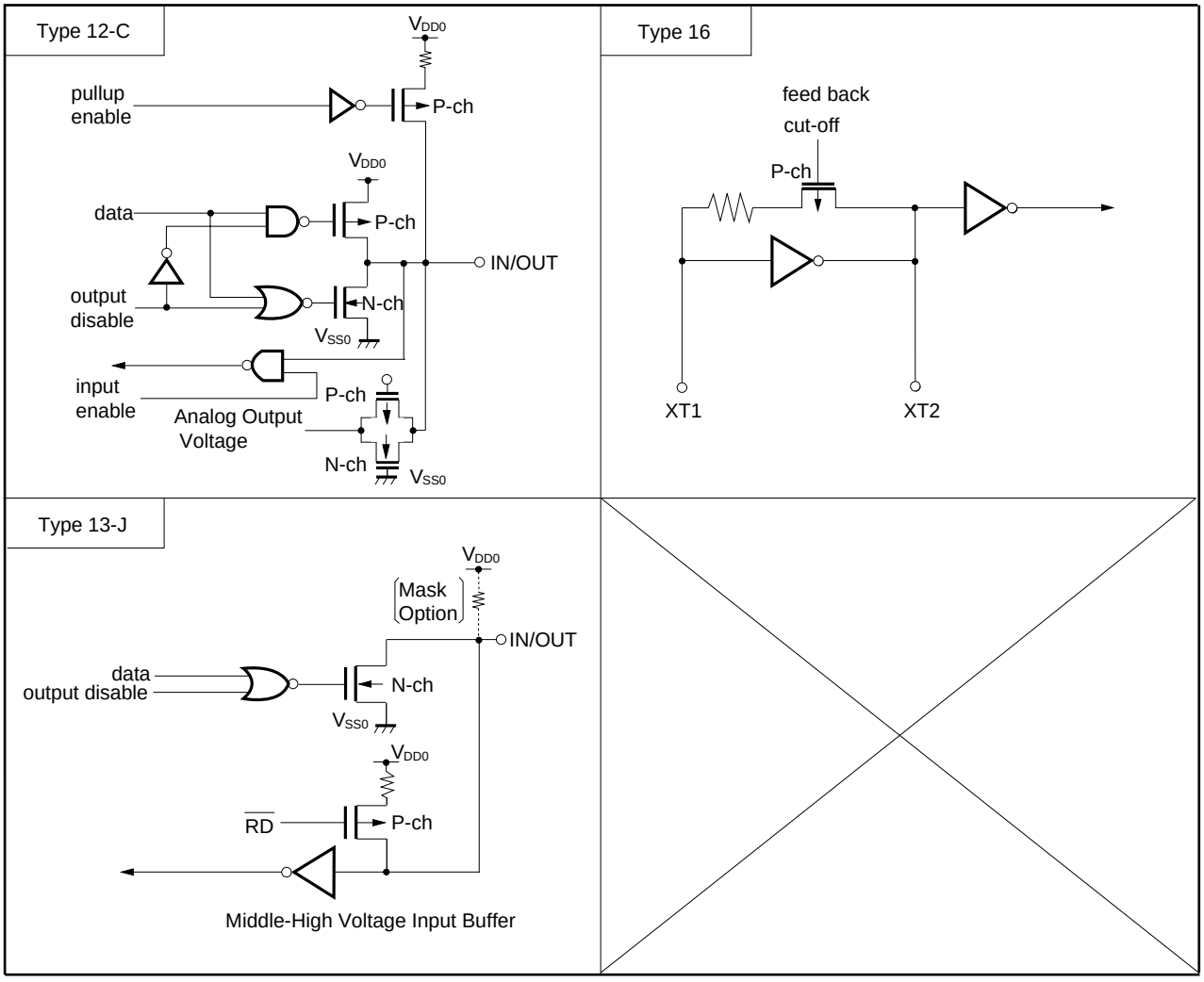


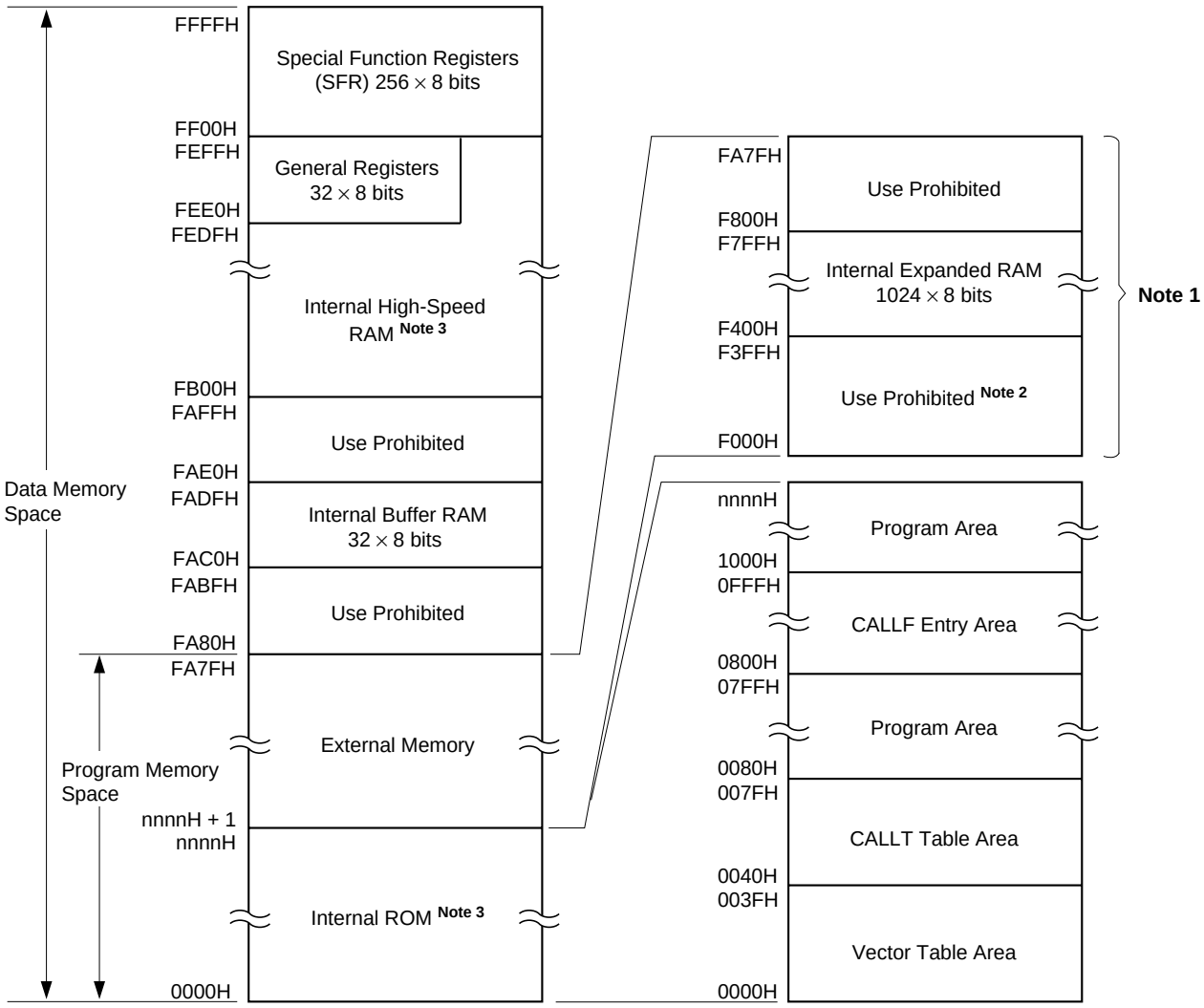
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the μPD780053/780054/780055/780056/780058 memory map.

Figure 4-1. Memory Map



Notes 1. μPD780058 only

2. When the external device expansion function is used with the μPD780058, set the internal ROM capacity to 56K bytes or less using the memory size switching register (IMS).

3. The internal ROM capacity depends on the products (see the next table).

Relevant Product Name	Internal ROM Last Address nnnnH
μPD780053	5FFFH
μPD780054	7FFFH
μPD780055	9FFFH
μPD780056	BFFFH
μPD780058	EFFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The following three types of I/O ports are available.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01-P05, port 1-port 5, P64-P67, port 7, port 12, port 13) : 62
- N-channel open-drain input/output (P60-P63) : 4

Total : 68

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port pins
	P01-P05	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 1	P10-P17	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 2	P20-P27	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 3	P30-P37	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 4	P40-P47	Input/output port pins. Input/output specifiable in 8-bit units. When used as input port pins, on-chip pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50-P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. LED direct drive capability.
Port 6	P60-P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be used by mask option. LED direct drive capability.
	P64-P67	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 7	P70-P72	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 12	P120-P127	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.
Port 13	P130, P131	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software.

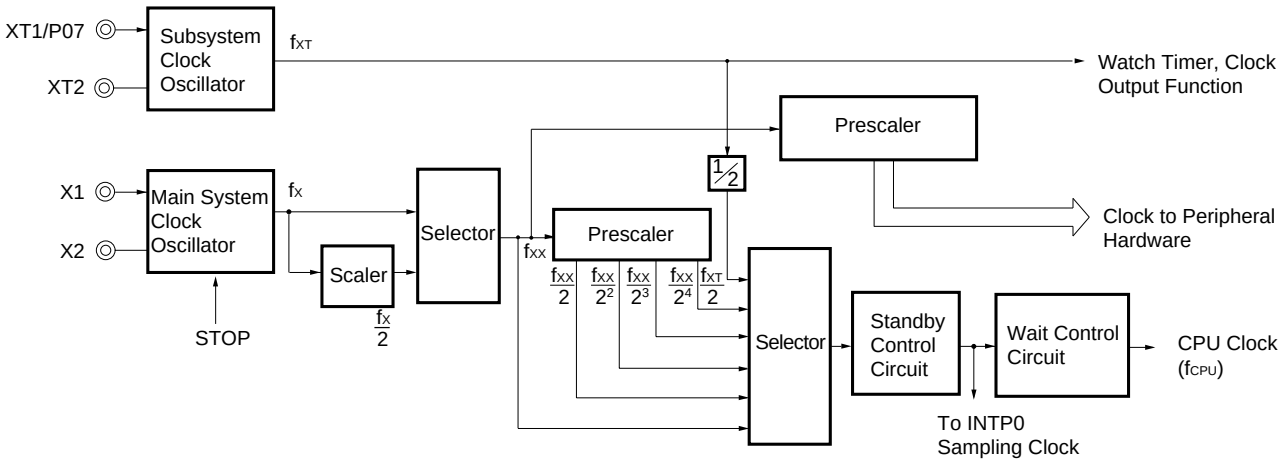
5.2 CLOCK GENERATOR

Two types of generators, a main system clock generator and a subsystem clock generator, are avaibable.

The minimum instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: at 5.0 MHz operation)
- 122 μs (subsystem clock: at 32.768 kHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

The following five channels of the timer/event counter are available.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Operations of Timer/Event Counter

		16-Bit Timer/ Event Counter	8-Bit Timer/ Event Counter	Watch Timer	Watchdog Timer
Operation mode	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	—	—
Function	Timer output	1 output	2 outputs	—	—
	PWM output	1 output	—	—	—
	Pulse width measurement	1 input	—	—	—
	Square wave output	1 output	2 outputs	—	—
	Ono-shot pulse output	1 output	—	—	—
	Interrupt request	2	2	2	1

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

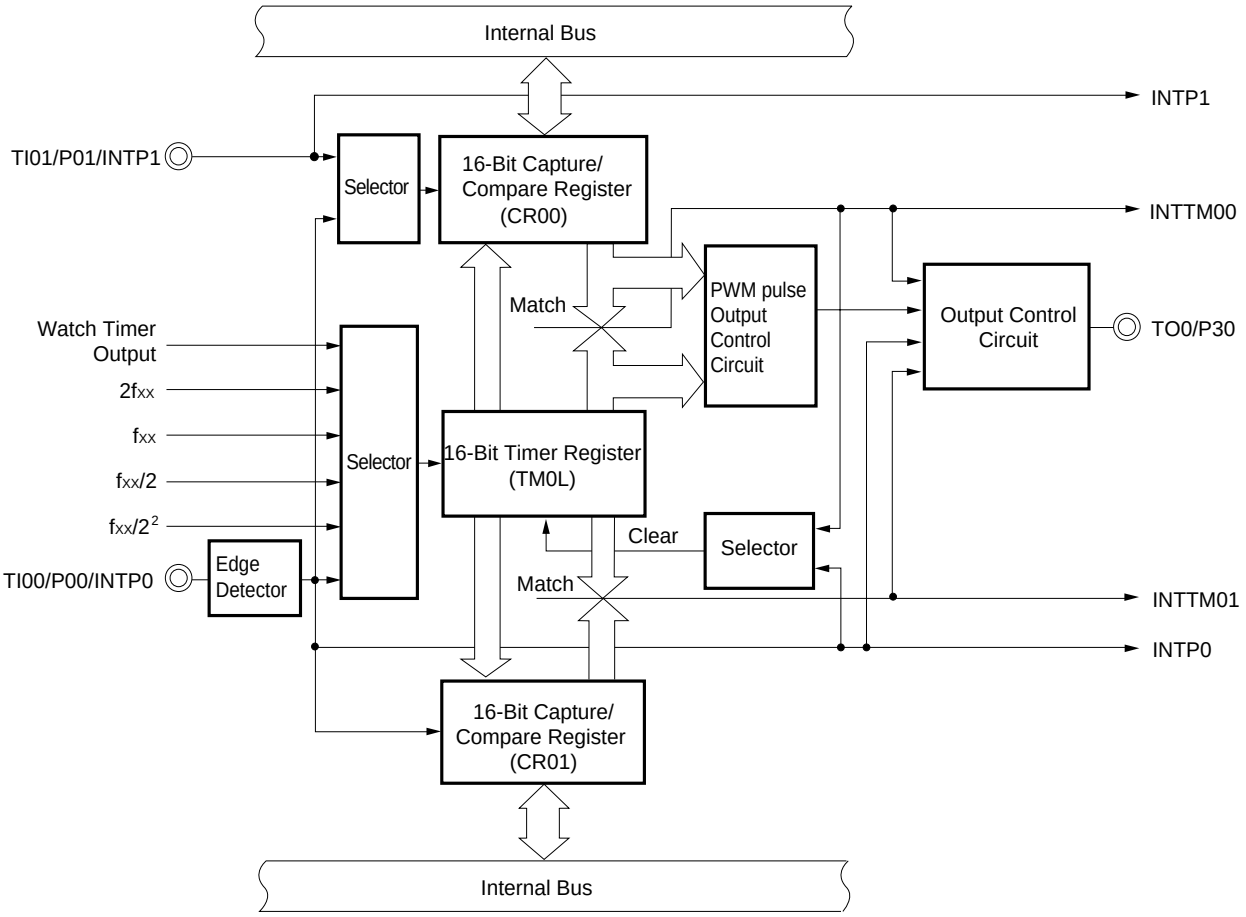


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

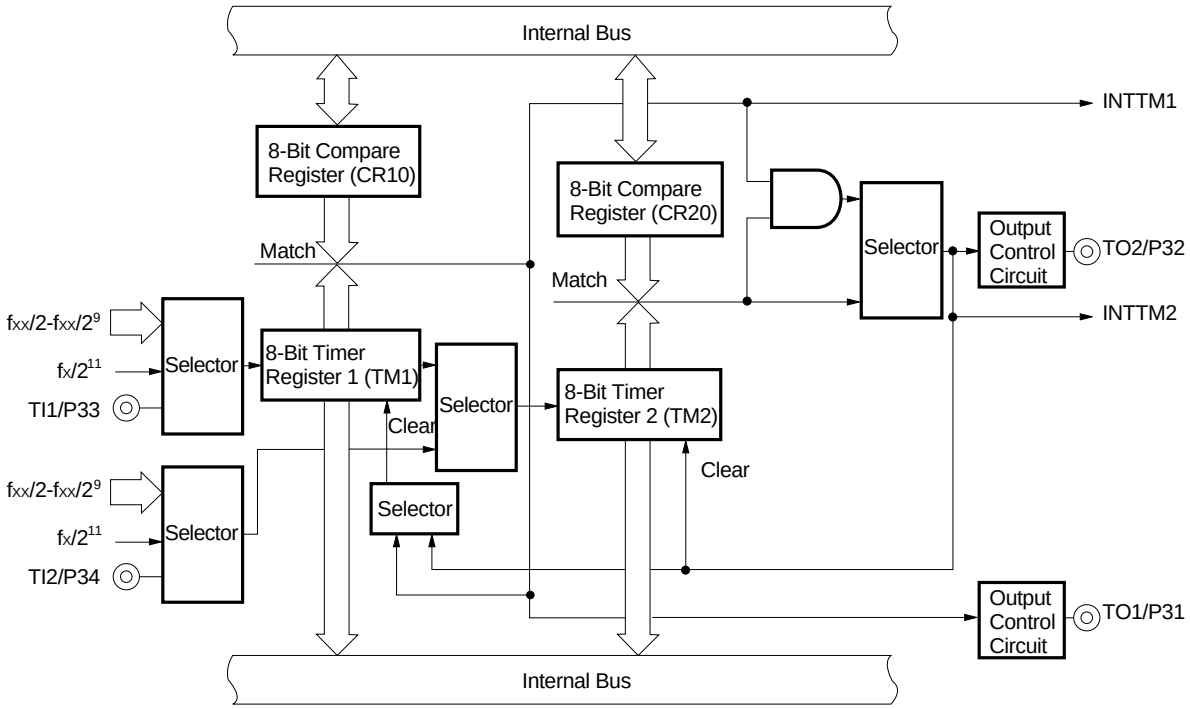


Figure 5-4. Watch Timer Block Diagram

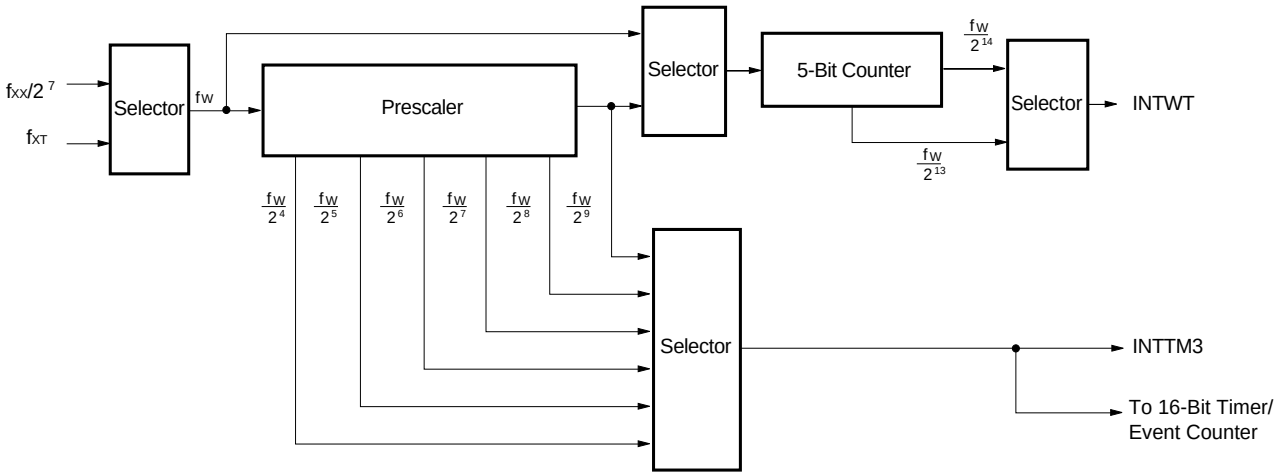
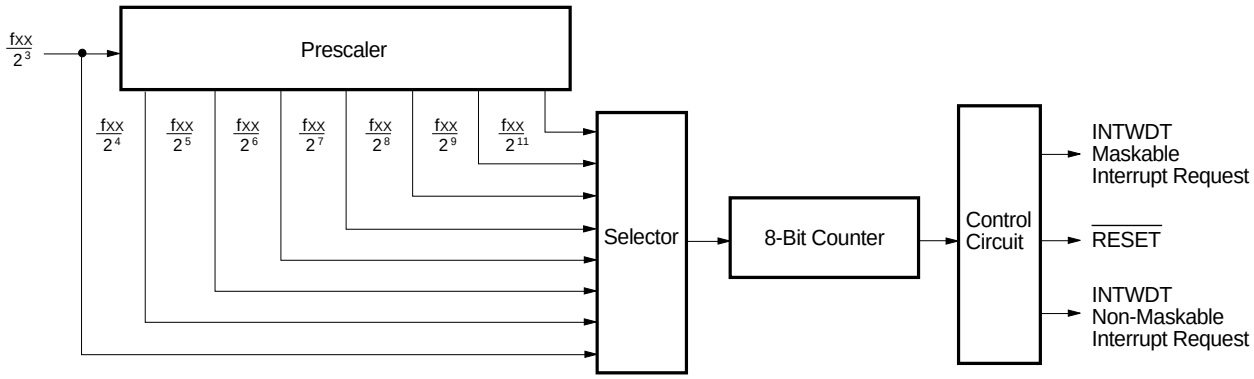


Figure 5-5. Watchdog Timer Block Diagram

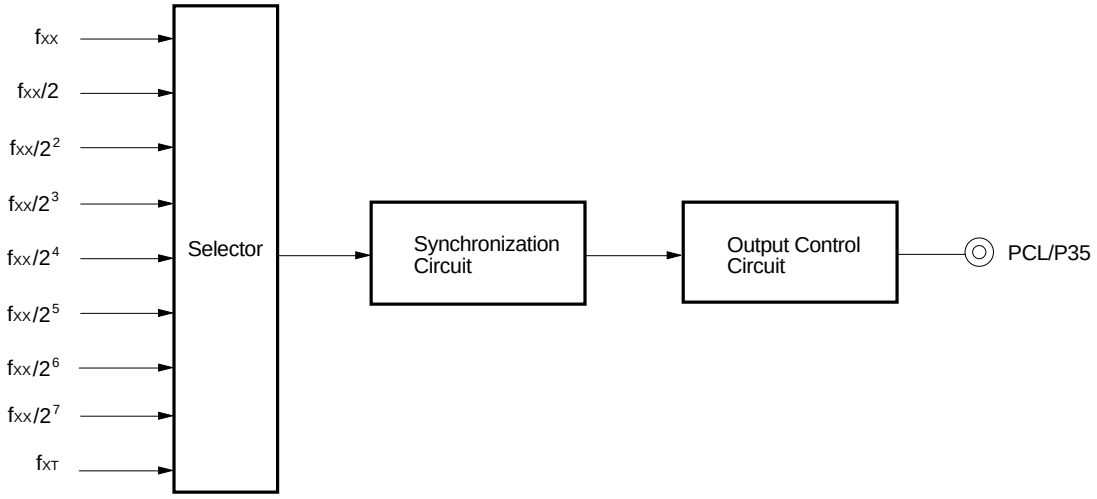


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: at 5.0 MHz operation)
- 32.768 kHz (subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Circuit Configuration

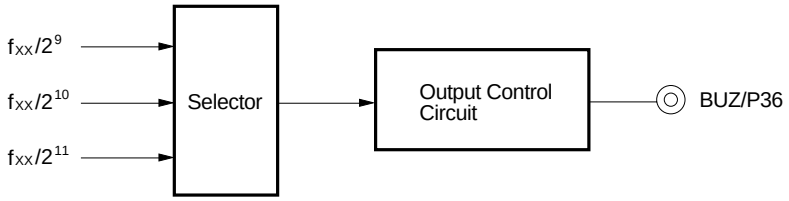


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock: at 5.0 MHz operation)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



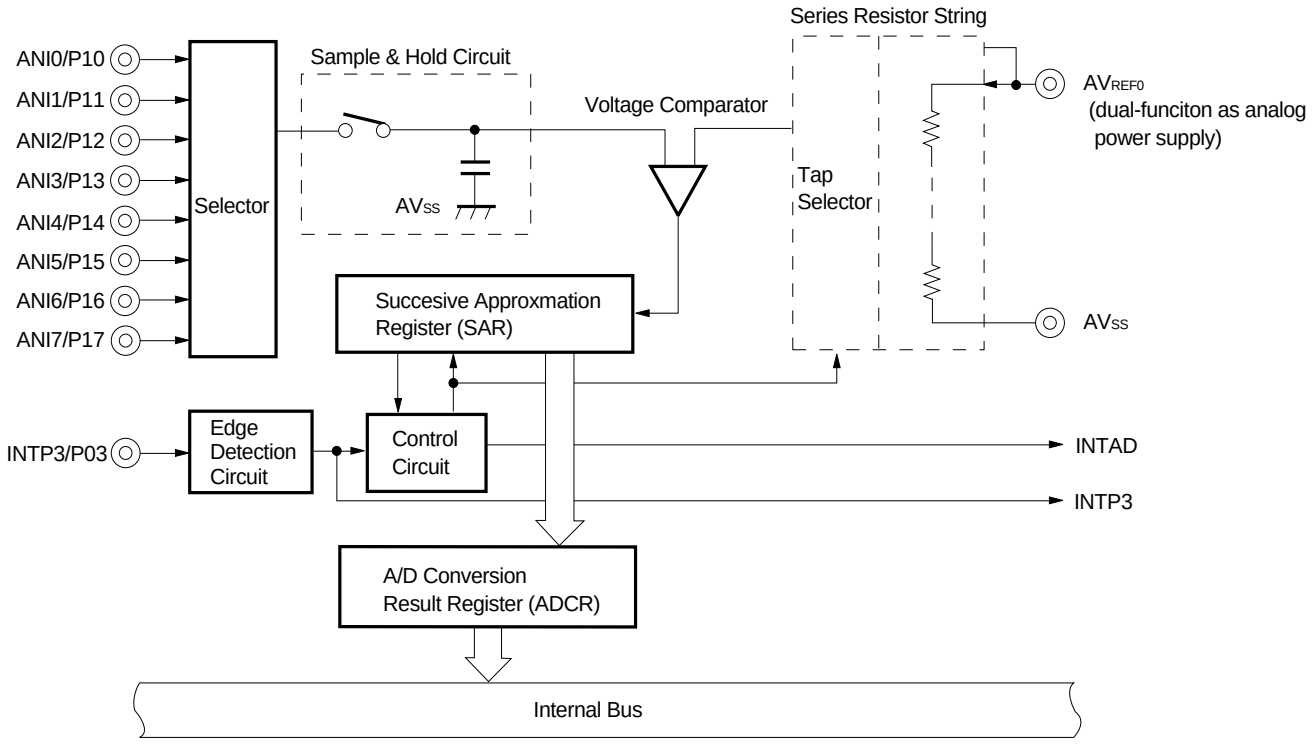
5.6 A/D CONVERTER

An A/D converter of 8-bit resolution × 8 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram

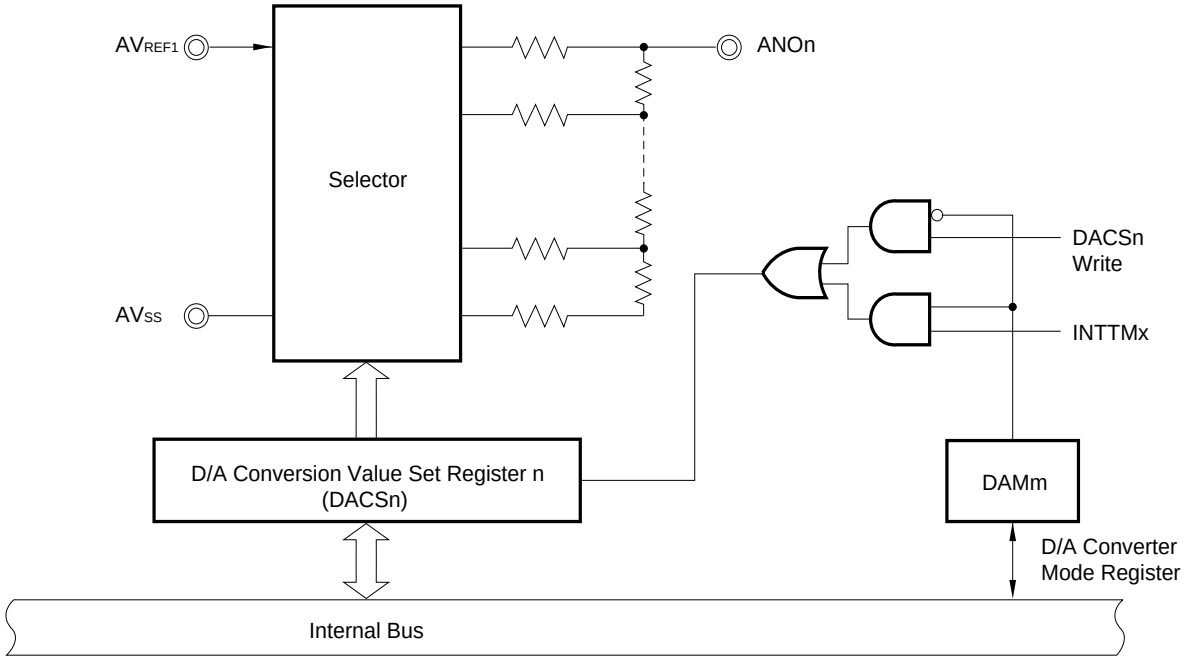


5.7 D/A CONVERTER

A D/A converter of 8-bit resolution × 2 channels is available.

Conversion method is R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1

m = 4, 5

x = 1, 2

5.8 SERIAL INTERFACES

Three channels of the clocked serial interface are incorporated.

- Serifal interface channel 0
- Serifal interface channel 1
- Serifal interface channel 2

Table 5-3. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	○ (MSB/LSB first switchable)	○ (MSB/LSB first switchable)	○ (MSB/LSB first switchable)
3-wire serial I/O mode with automatic transmit/receive function	—	○ (MSB/LSB first switchable)	—
SBI (serial bus interface) mode	○ (MSB first)	—	—
2-wire serial I/O mode	○ (MSB first)	—	—
Asynchronous serial interface (UART) mode (on-chip time division transfer function)	—	—	○ (Dedicated baud rate generator incorporated)

Figure 5-10. Serial Interface Channel 0 Block Diagram

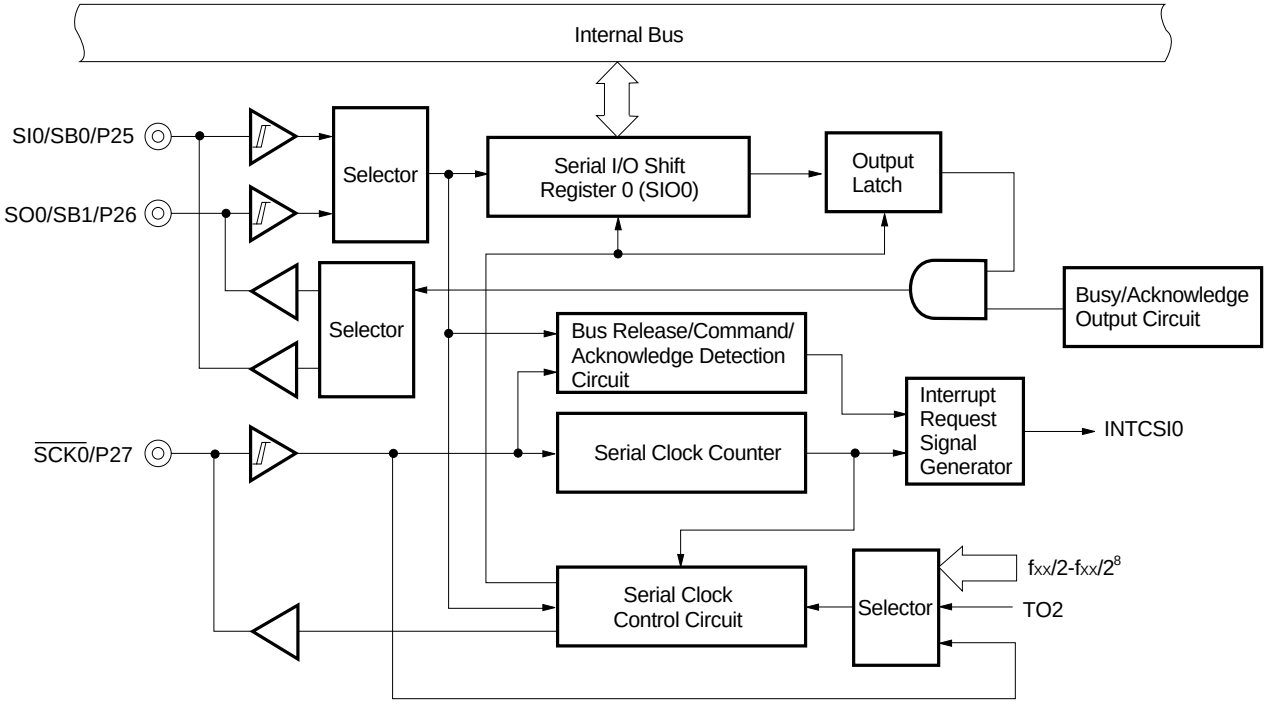


Figure 5-11. Serial Interface Channel 1 Block Diagram

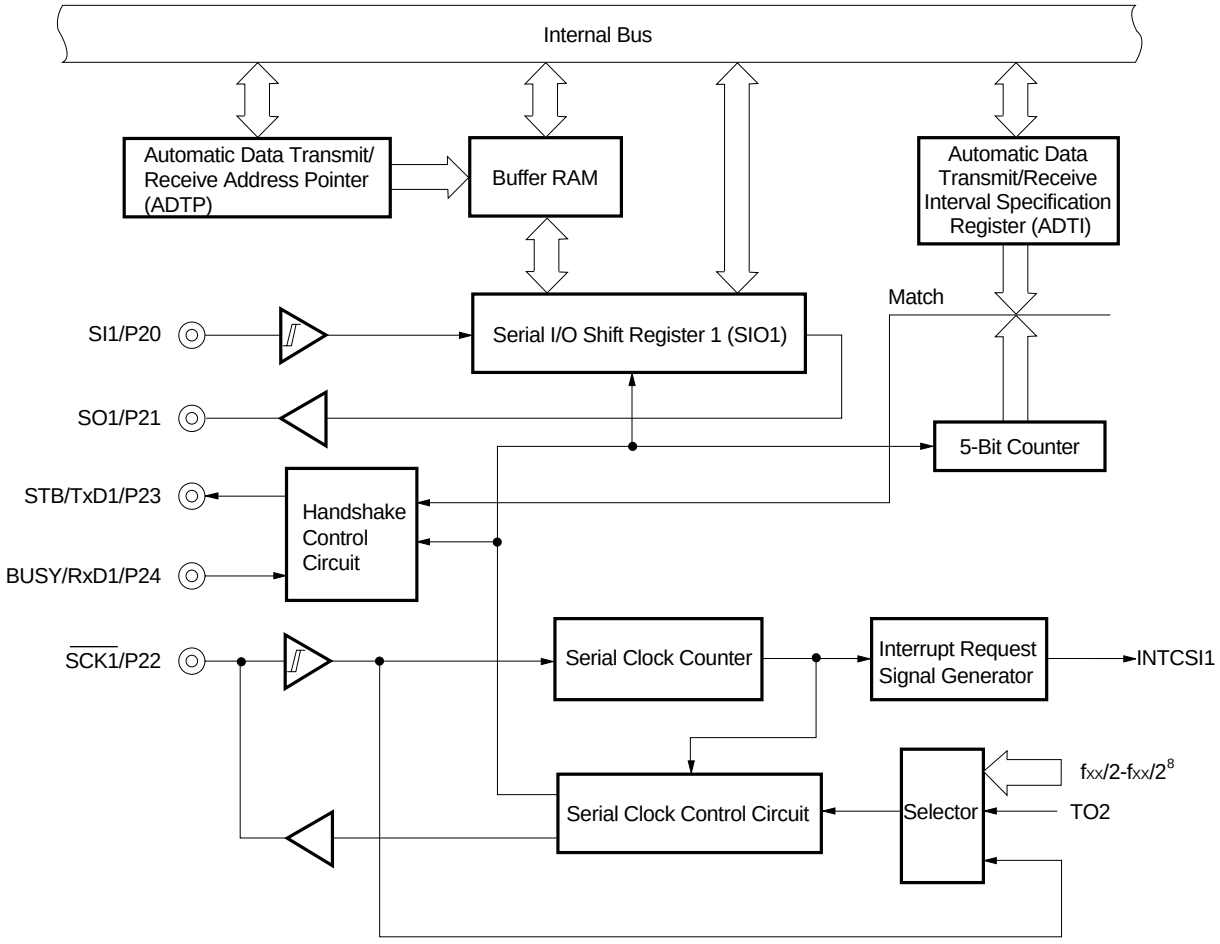
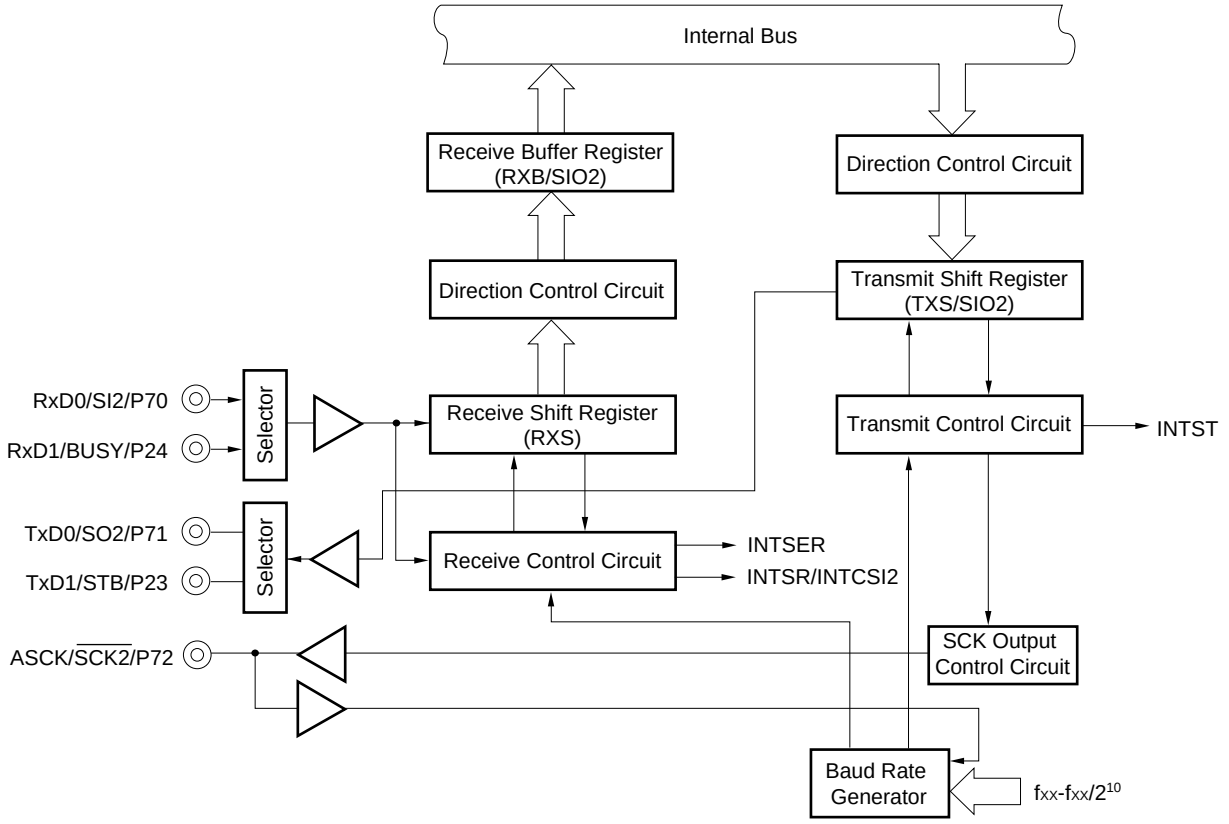


Figure 5-12. Serial Interface Channel 2 Block Diagram

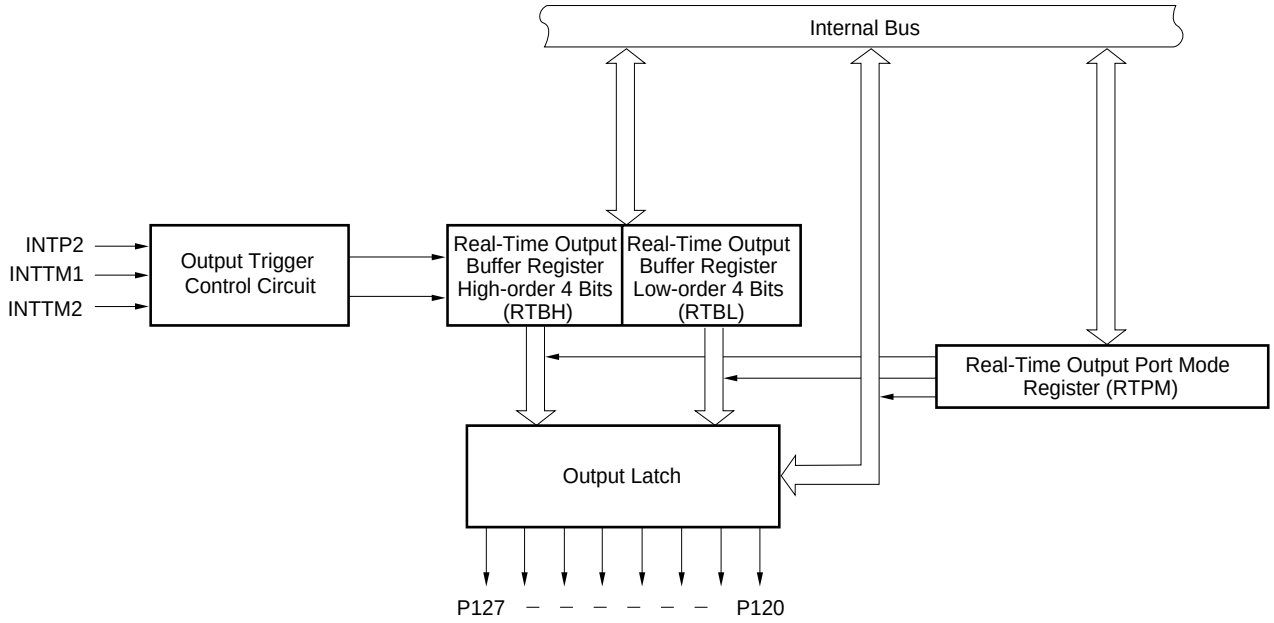


5.9 REAL-TIME OUTPUT PORT FUNCTIONS

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt request and external interrupt request generation in order to output to off-chip. This is real-time output function. And pins to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motor, etc.

Figure 5-13. Real-Time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are interrupt functions, 21 sources of three different kinds, as shown below.

- Non-maskable : 1
- Maskable : 19
- Software : 1

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	——	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	(B)
	8	INTCSI1	End of serial interface channel 1 transfer		0016H	
	9	INTSER	Generation of serial interface channel 2 UART receive error		0018H	
	10	INTSR	End of serial interface channel 2 UART reception		001AH	
		INTCSI2	End of serial interface channel 2 3-wire transfer			
	11	INTS	End of serial interface channel 2 UART transmission		001CH	

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 17, the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Table 6-1. Interrupt Source List (2/2)

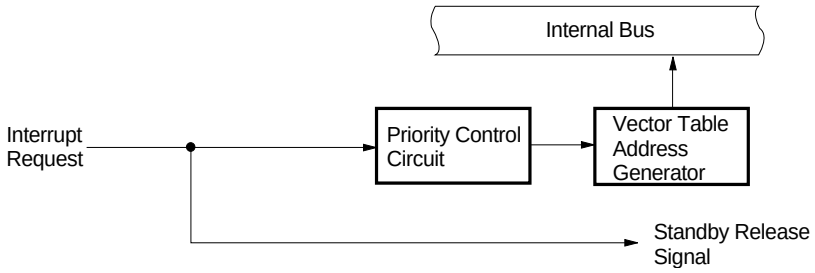
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
	12	INTTM3	Reference time interval signal from watch timer	Internal	001EH	(B)
	13	INTTM00	Generation of match signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	14	INTTM01	Generation of match signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	15	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	16	INTTM2	Generation of match signal of 8-bit timer/ event counter 2		0026H	
	17	INTAD	End of conversion by A/D converter		0028H	
Software	—	BRK	BRK instruction execution	–	003EH	(E)

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 17, the lowest.

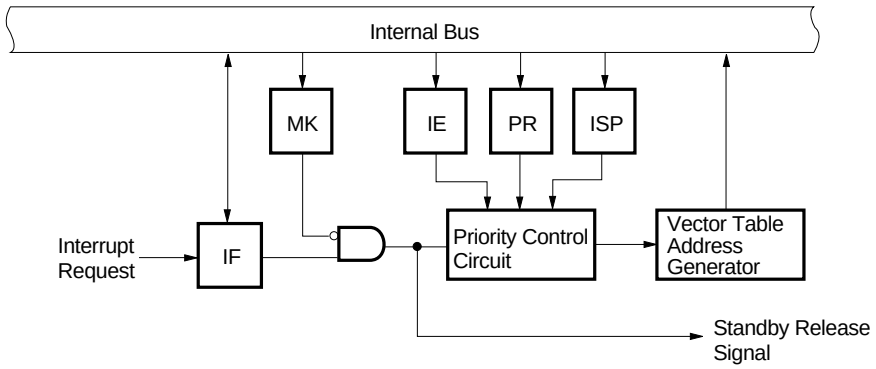
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration(1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

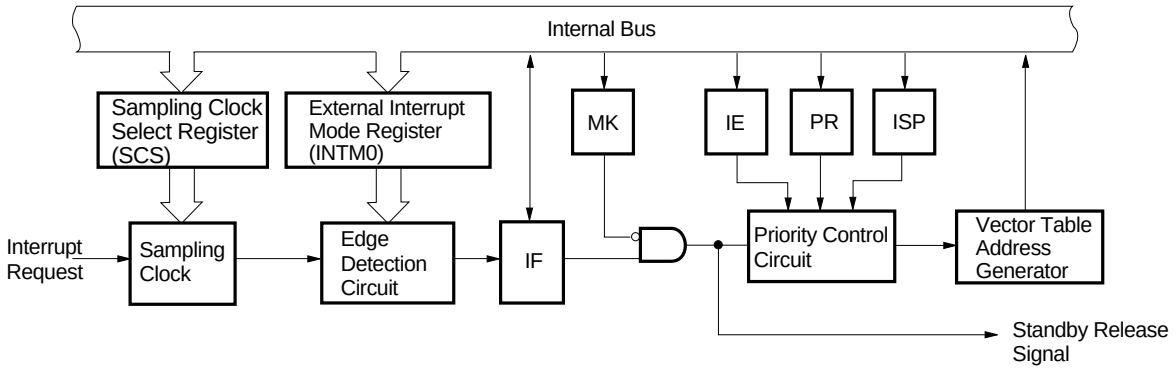
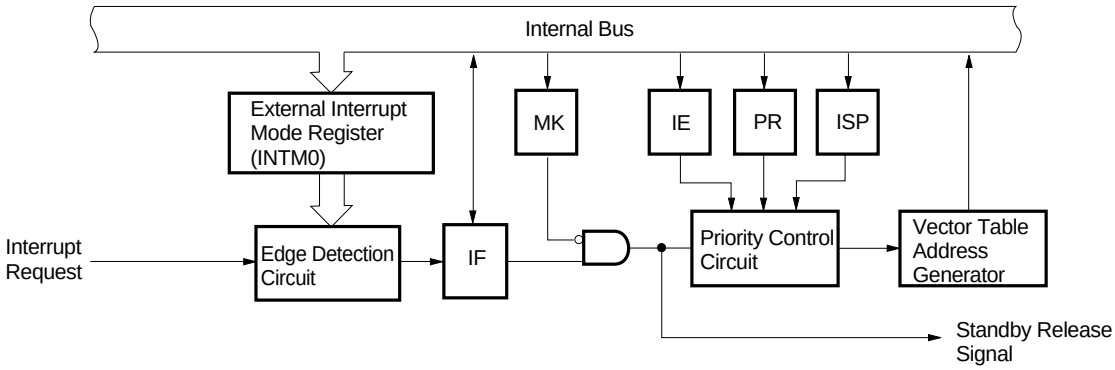
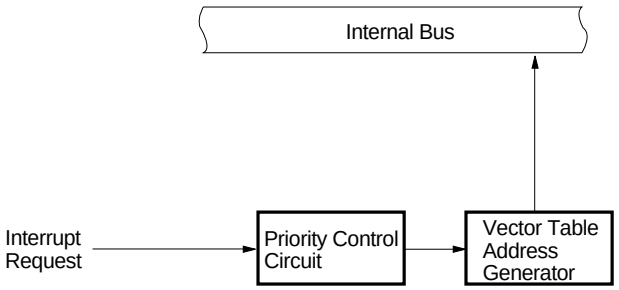


Figure 6-1. Interrupt Function Basic Configuration(2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

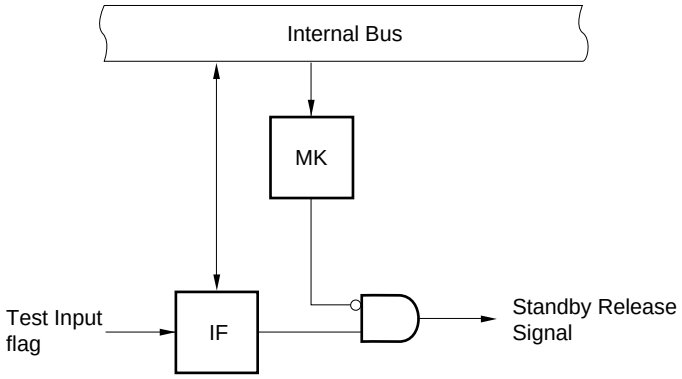
6.2 TEST FUNCTIONS

There are two sources of test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

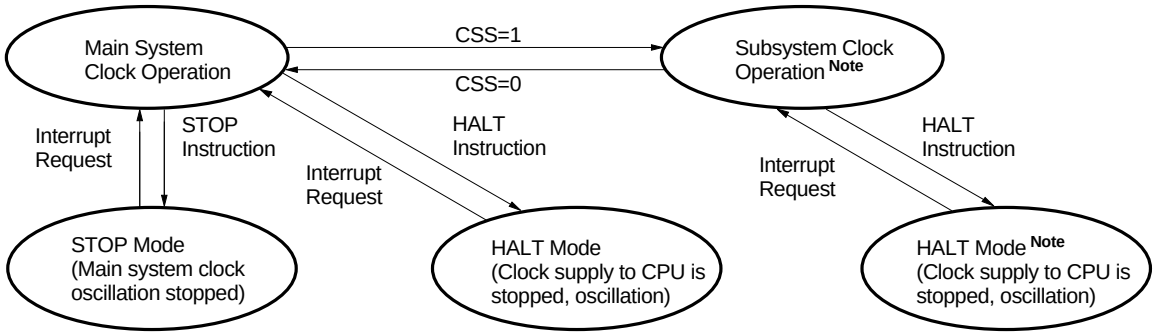
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.
  The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Function



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC (bit 7 of the processor clock control register (PCC)) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Remark CSS: Bit 4 of processor clock control regisrer (PCC).

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog time runaway time detection

10. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + Byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + Byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instruction

MOV, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp [Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW [Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 11. ELECTRICAL SPECIFICATIONS

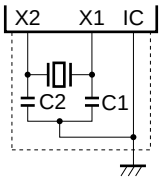
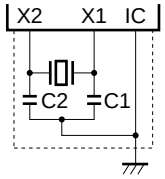
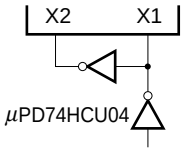
Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P05, P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	N-ch Open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	1 pin		–10	mA
		P01-P05, P30-P37, P56, P57, P60-P67, P120-P127 total		–15	mA
		P10-P17, P20-P27, P40-P47, P50-P55, P70-P72, P130, P131 total		–15	mA
Output current, low	I_{OL} **Note**	1 pin	Peak value	30	mA
			rms value	15	mA
		P50-P55 total	Peak value	100	mA
			rms value	70	mA
		P56, P57, P60-P63 total	Peak value	100	mA
			rms value	70	mA
		P10-P17, P20-P27, P40-P47, P70-P72, P130, P131 total	Peak value	50	mA
			rms value	20	mA
		P01-P05, P30-P37, P64-P67, P120-P127 total	Peak value	50	mA
			rms value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) Note 1	V_{DD} = Oscillator voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx) Note 1		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

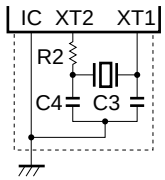
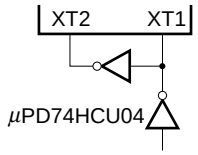
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wirinin the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS1}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured in software.

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) **Note 1**		32	32.768	35	kHz
		Oscillation stabilization time **Note 2**	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) **Note 1**		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS1}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. Therefore, when using the subsystem clock, take care with the wiring.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Measured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Measured pins returned to 0 V.	P01-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131			15	pF
			P60-P63			20	pF

Remark The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P05, P20, P22, P24-P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		15	V
				0.8 V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
			Note	0.9 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P05, P20, P22, P24-P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60-P63	4.5 V≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			Note	0		0.1 V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage, low	V_{OL1}	P50-P57, P60-P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P05, P10-P17, P20-P27, P30-P37, P40-P47, P64-P67, P70-P72, P120-P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain, pulled-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note For use as P07, use an inverter to input the reverse phase of P07 to the XT2 pin.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P72, P120-P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60-P63			–3[Note]	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60-P63		20	40	120	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131		15	30	90	kΩ

Note For P60 to P63 without on-chip pull-up resistor (specifiable by mask option), a low-level input leakage current of –200 μA (MAX.) flows only during the 1.5 clocks (no wait) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 1.5 clocks following executing a read-out instruction, the current is –3 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current Note 5	I_{DD1}	5.0 MHz Crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 3	V_{DD} = 5.0 V ±10 % Note 1		4	12	mA
			V_{DD} = 3.0 V ±10 % Note 2		0.6	1.8	mA
			V_{DD} = 2.0 V ±10 % Note 2		0.35	1.05	mA
		5.0 MHz Crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 4	V_{DD} = 5.0 V ±10 % Note 1		6.5	19.5	mA
			V_{DD} = 3.0 V ±10 % Note 2		0.8	2.4	mA
	I_{DD2}	5.0 MHz Crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 3	V_{DD} = 5.0 V ±10 %		1.4	4.2	mA
			V_{DD} = 3.0 V ±10 %		0.5	1.5	mA
			V_{DD} = 2.0 V ±10 %		280	840	μA
		5.0 MHz Crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 4	V_{DD} = 5.0 V ±10 %		1.6	4.8	mA
			V_{DD} = 3.0 V ±10 %		0.65	1.95	mA
	I_{DD3}	32.768 kHz Crystal oscillation operating mode Note 6	V_{DD} = 5.0 V ±10 %		60	120	μA
			V_{DD} = 3.0 V ±10 %		32	64	μA
			V_{DD} = 2.0 V ±10 %		24	48	μA
	I_{DD4}	32.768 kHz Crystal oscillation HALT mode Note 6	V_{DD} = 5.0 V ±10 %		25	55	μA
			V_{DD} = 3.0 V ±10 %		5	15	μA
			V_{DD} = 2.0 V ±10 %		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ±10 %		1	30	μA
			V_{DD} = 3.0 V ±10 %		0.5	10	μA
			V_{DD} = 2.0 V ±10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is unused	V_{DD} = 5.0 V ±10 %		0.1	30	μA
			V_{DD} = 3.0 V ±10 %		0.05	10	μA
			V_{DD} = 2.0 V ±10 %		0.05	10	μA

Notes 1. Operating in high-speed mode (when set the processor clock control register (PCC) to 00H).

2. Operating in low-speed mode (when set the PCC to 04H).

3. Operation with $f_{XX} = f_X/2$ (when oscillation mode selection register (OSMS) is set to 00H)

4. Operation with $f_{XX} = f_X$ (when OSMS is set to 01H)

5. This current flows in the V_{DD} and AV_{DD} pins. However, a current flowing in the A/D converter, D/A converter, and on-chip pull-up resistor are not included.

6. When the main system clock is halted

AC Characteristics

(1) Basic operation (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock (f_{XX} = 2.5 MHz)Note 1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		Operating on main system clock (f_{XX} = 5.0 MHz)Note 2	V_{DD} = 3.5 to 5.5 V	0.4		32	μs
			V_{DD} = 2.7 to 3.5 V	0.8		32	μs
		Operating on subsystem clock		40Note 3	122	125	μs
TI00 input high/ low-level width	t_{TIH00} t_{TIL00}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1Note 4			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$+0.2Note 4			μs
				$2/f_{sam}$+0.5Note 4			μs
TI01 input high/ low-level width	t_{TIH01} t_{TIL01}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs
TI1, TI2, TI5, TI6 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2, TI5, TI6 input high/ low-level width	t_{TIH1} t_{TIL1}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high/ low-level width	t_{INTH} t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$+0.1Note 4			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$+0.2Note 4			μs
				$2/f_{sam}$+0.5Note 4			μs
		INTP1-INTP5, P40-P47	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

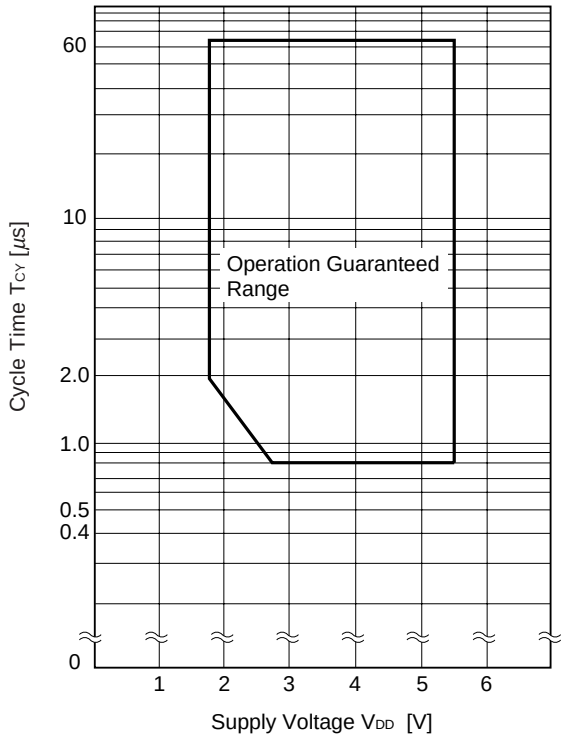
Notes 1. Operation with $f_{XX} = f_X/2$ (when oscillation mode selection register (OSMS) is set to 00H)

2. Operation with $f_{XX} = f_X$ (when OSMS is set to 01H)

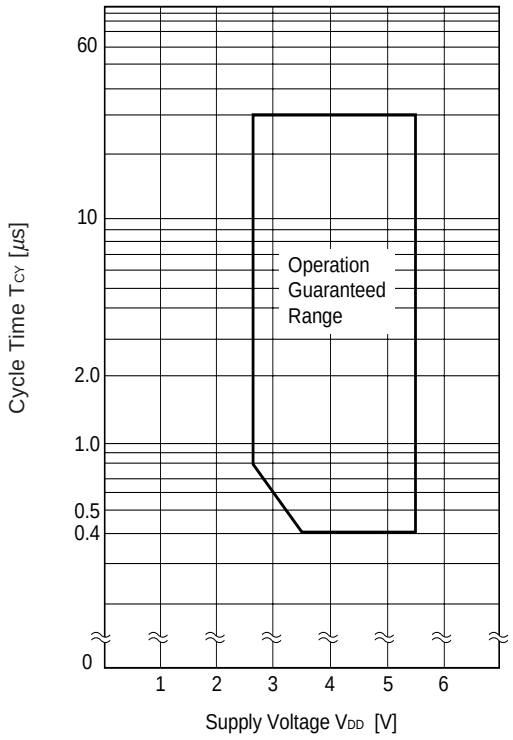
3. Value when external clock is used. When a crystal resonator is used, it is 114 μs (MIN.)

4. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$ and $f_{XX}/128$ (when N= 0 to 4).

★ **T_{CY} vs V_{DD} (At $f_{XX} = f_X/2$ main system clock operation)**



T_{CY} vs V_{DD} (At $f_{XX} = f_X$ main system clock operation)



(2) Read/write operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85 + 2n)t_{CY}$ – 80	ns
	t_{ADD2}			$(4 + 2n)t_{CY}$ – 100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 100	ns
	t_{RDD2}			$(2.85 + 2n)t_{CY}$ – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)t_{CY}$ – 60		ns
	t_{RDL2}		$(2.85 + 2n)t_{CY}$ – 60		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)t_{CY}$ – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85 + 2n)t_{CY}$ – 60		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}$ + 40	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks 1. MCS: Oscillation mode selection register (OSMS) bit 0

2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0

3. $t_{CY} = T_{CY}/4$

4. n indicates number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85 °C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 5.5 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 5.5 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 5.5 V	0.4t_{CY} – 10		ns
			0.37t_{CY} – 40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 5.5 V		(3 + 2n)t_{CY} – 160	ns
				(3 + 2n)t_{CY} – 320	ns
	t_{ADD2}	V_{DD} = 2.7 to 5.5 V		(4 + 2n)t_{CY} – 200	ns
				(4 + 2n)t_{CY} – 300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 5.5 V		(1.4 + 2n)t_{CY} – 70	ns
				(1.37 + 2n)t_{CY} – 120	ns
	t_{RDD2}	V_{DD} = 2.7 to 5.5 V		(2.4 + 2n)t_{CY} – 70	ns
				(2.37 + 2n)t_{CY} – 120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 5.5 V	(1.4 + 2n)t_{CY} – 20		ns
			(1.37 + 2n)t_{CY} – 20		ns
	t_{RDL2}	V_{DD} = 2.7 to 5.5 V	(2.4 + 2n)t_{CY} – 20		ns
			(2.37 + 2n)t_{CY} – 20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}	V_{DD} = 2.7 to 5.5 V		t_{CY} – 100	ns
				t_{CY} – 200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 5.5 V		2t_{CY} – 100	ns
				2t_{CY} – 200	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}	V_{DD} = 2.7 to 5.5 V		2t_{CY} – 100	ns
				2t_{CY} – 200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 5.5 V	(2.4 + 2n)t_{CY} – 60		ns
			(2.37 + 2n)t_{CY} – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}	V_{DD} = 2.7 to 5.5 V	(2.4 + 2n)t_{CY} – 20		ns
			(2.37 + 2n)t_{CY} – 20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}	V_{DD} = 2.7 to 5.5 V	0.4t_{CY} – 30		ns
			0.37t_{CY} – 50		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}	V_{DD} = 2.7 to 5.5 V	1.4t_{CY} – 30		ns
			1.37t_{CY} – 50		ns

Remarks 1. MCS: Oscillation mode selection register (OSMS) bit 0

2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0

3. $t_{CY} = T_{CY}/4$

4. n indicates number of waits.

(b) When except MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85 °C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 2.7 to 5.5 V	0.4t_{CY} – 20		ns
			0.37t_{CY} – 40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 5.5 V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 2.7 to 5.5 V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}	V_{DD} = 2.7 to 5.5 V	0.6t_{CY} + 180	2.6t_{CY} + 180	ns
			0.63t_{CY} + 350	2.63t_{CY} + 350	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}	V_{DD} = 2.7 to 5.5 V	0.6t_{CY} + 120	2.6t_{CY}+ 120	ns
			0.63t_{CY} + 240	2.63t_{CY}+ 240	ns

Remarks 1. MCS: Oscillation mode selection register (OSMS) bit 0

2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0

3. $t_{CY} = T_{CY}/4$

4. n indicates number of waits.

(3) Serial interface (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	2.0 V ≤ V_{DD} ≤ 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5V			300	ns
						500	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH3}, t_{KL3}	4.5 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3}/2 - 50$			ns
		2.0 V ≤ V_{DD} < 4.5 V		$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH4}, t_{KL4}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.0 V ≤ V_{DD} < 4.5 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
				3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	$t_{KCY5}/2 - 160$			ns
				$t_{KCY5}/2 - 190$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
							ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH6}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL6}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		800	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KIS8}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2–50			ns
			t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF **Note**			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} < 5.5 V	t_{KCY9}–30		t_{KCY9}+30	ns
		2.0 V < V_{DD} < 2.7 V	t_{KCY9}–60		t_{KCY9}+60	ns
			t_{KCY9}–90		t_{KCY9}+90	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				2t_{KCY9}	ns

Note C is the load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	t_{KCY11}/2–50			ns
			t_{KCY11}/2–100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of the SO2 output line.

★ **(ii) 3-wire serial I/O mode ($\overline{SCK2}$...External clock input)**

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}			400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	Other than below				160	ns
		V_{DD} = 4.5 to 5.5 V When not using external device expansion function				1	μs

Note C is the load capacitance of the SO2 output line.

(iii) UART mode (Dedicated baud rate generator output)

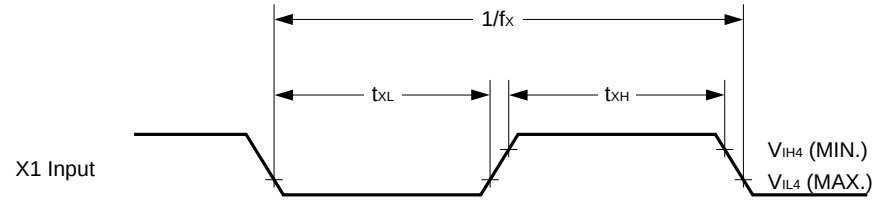
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
		2.0 V ≤ V_{DD} < 2.7 V			19531	bps
					9766	bps

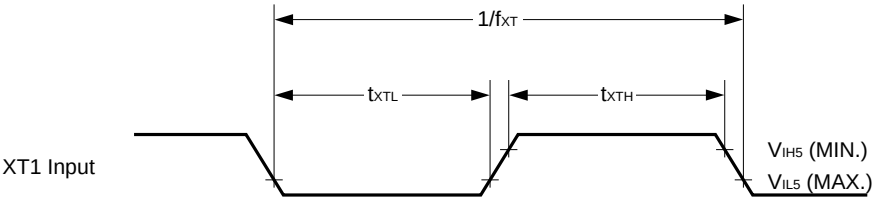
★ **(iv) UART mode (External clock input)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
		2.0 V ≤ V_{DD} < 2.7 V			9766	bps
					6510	bps
ASCK rise, fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 5.5 V, when not using external device expansion function.			1000	ns
					160	ns

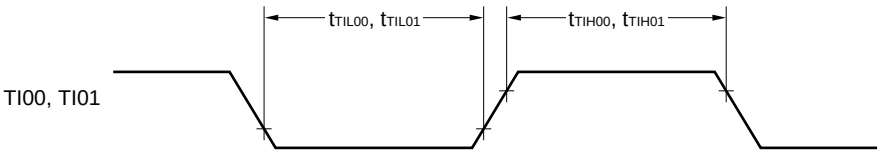
AC Timing Test Point (Excluding X1, XT1 Input)

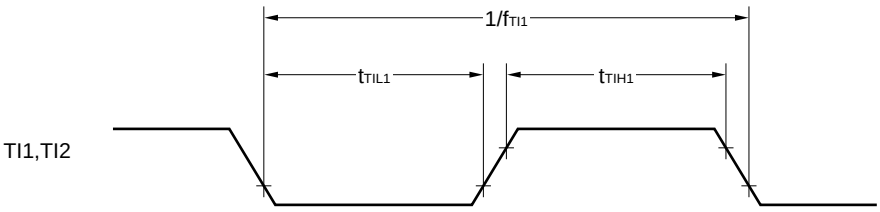
Clock Timing





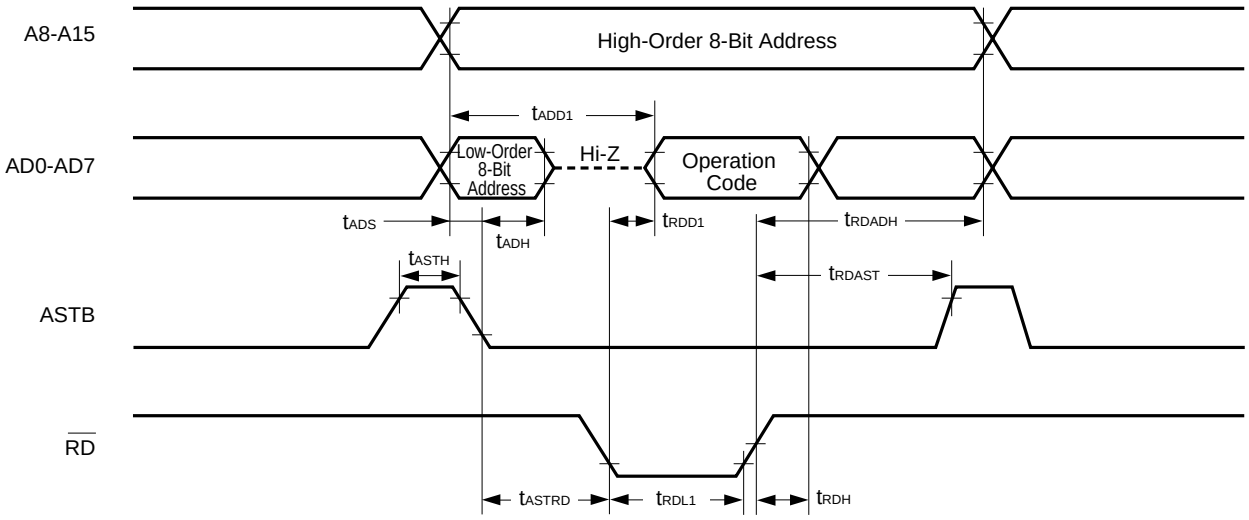
TI Timing



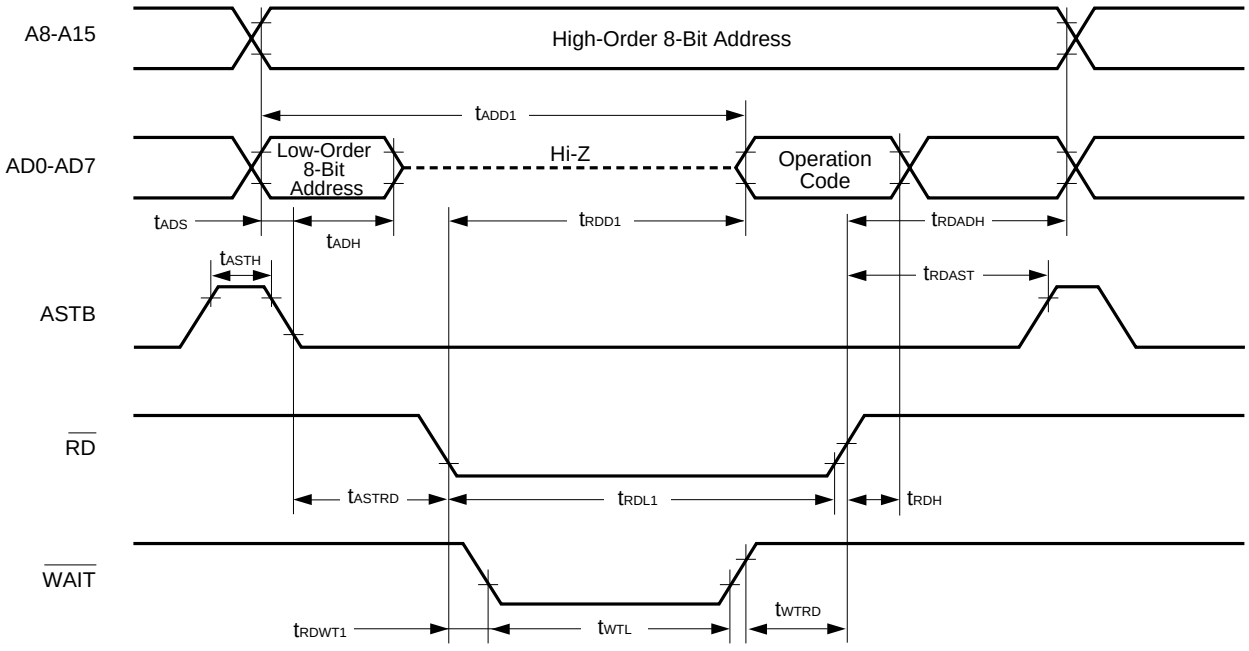


Read/Write Operation

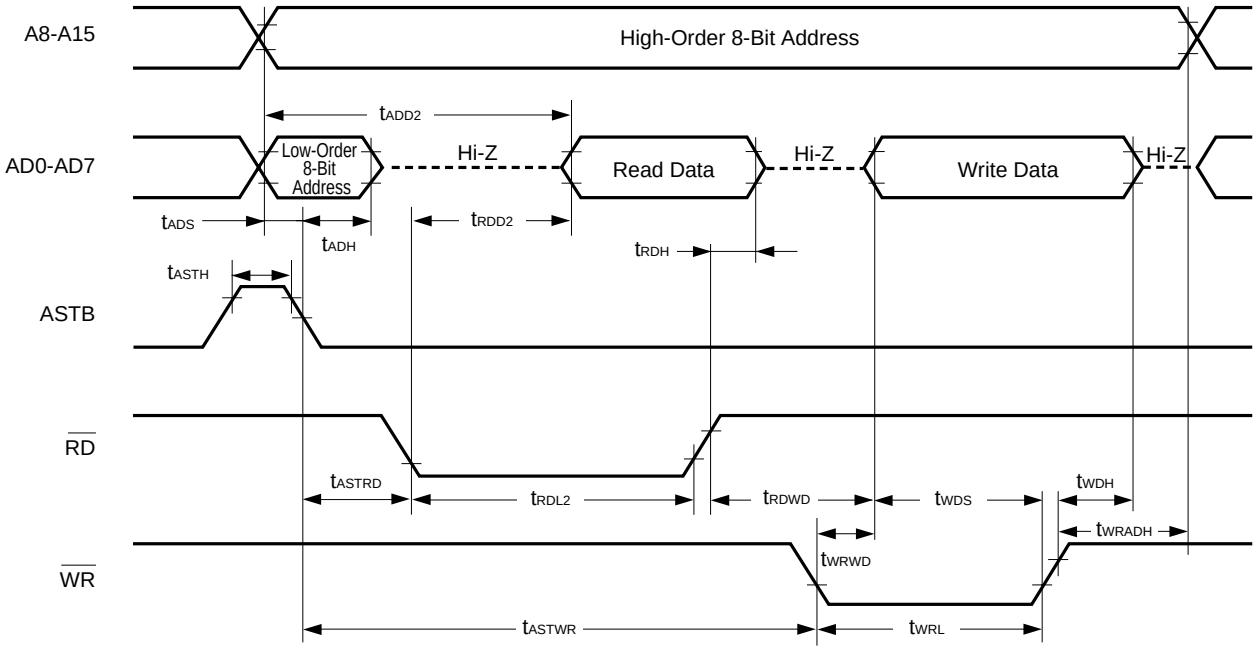
External fetch (no wait) :



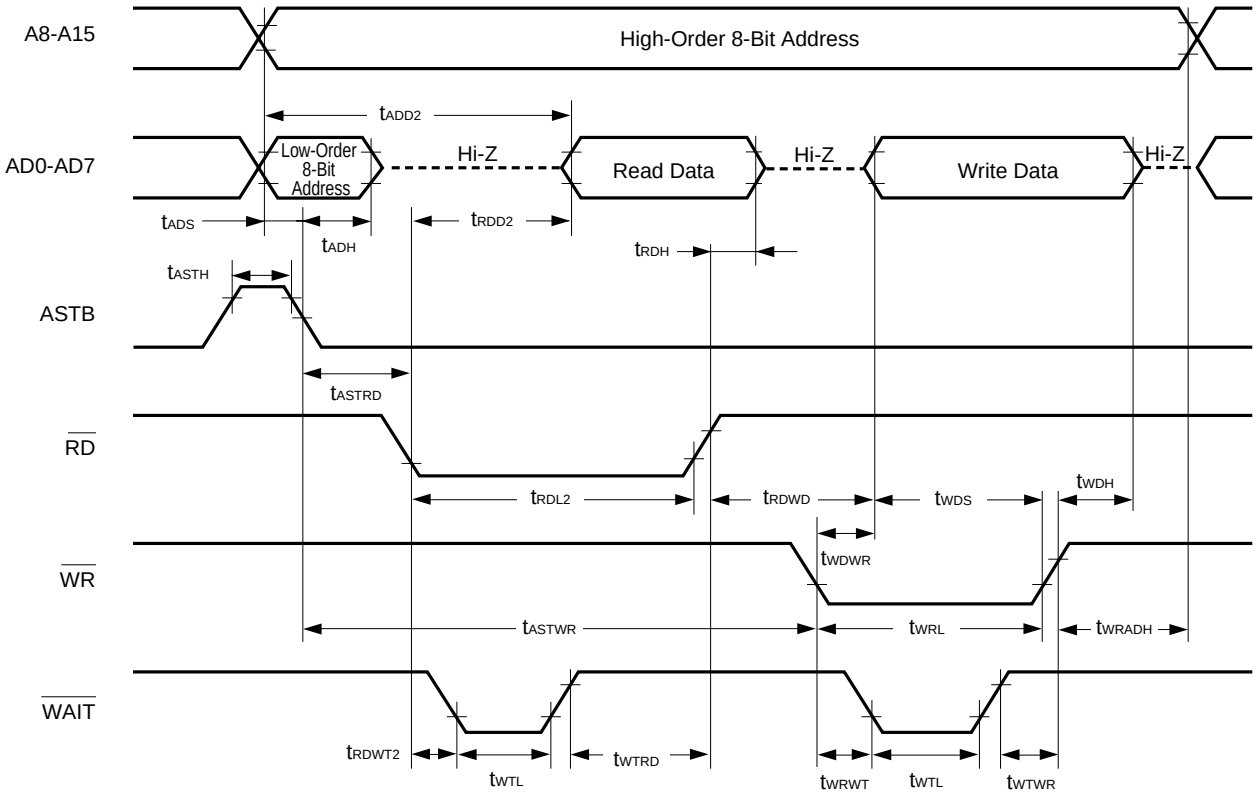
External fetch (wait insertion) :



External data access (no wait) :

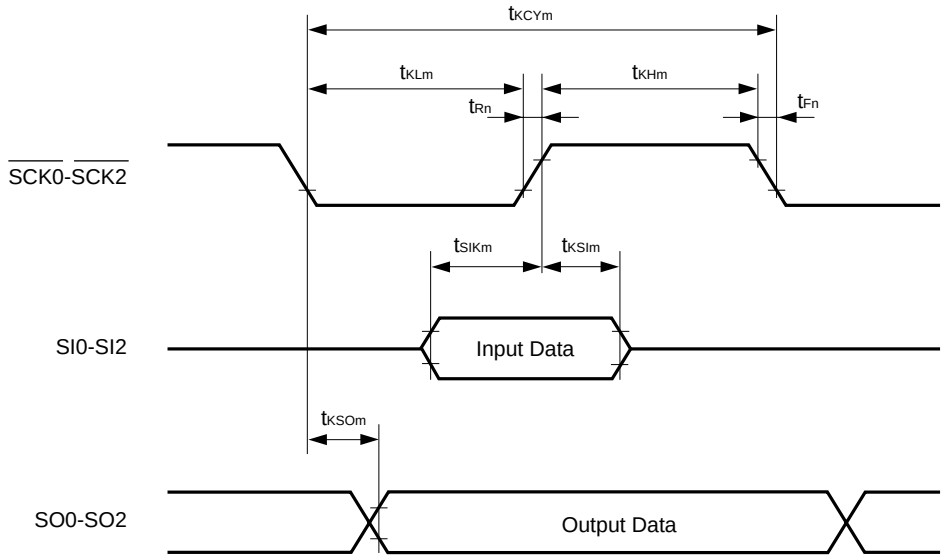


External data access (wait insertion) :



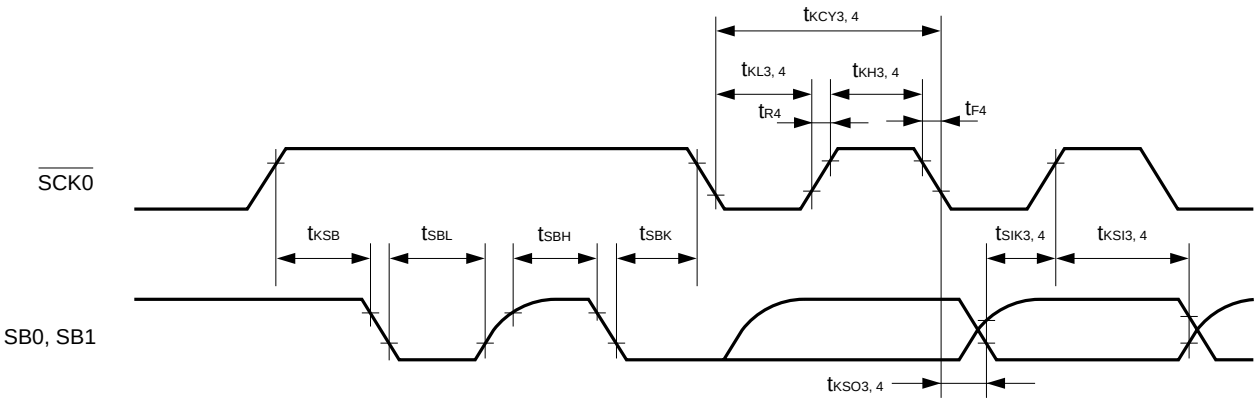
Serial Transfer Timing

3-wire serial I/O mode :

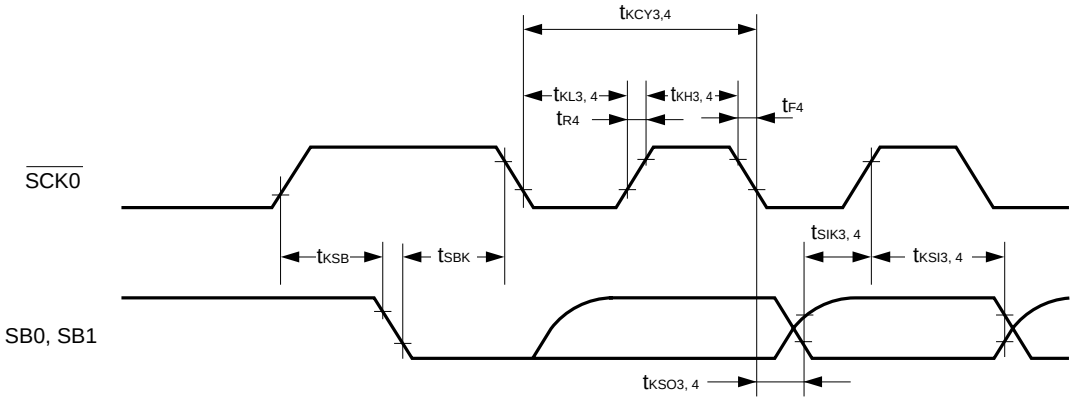


m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

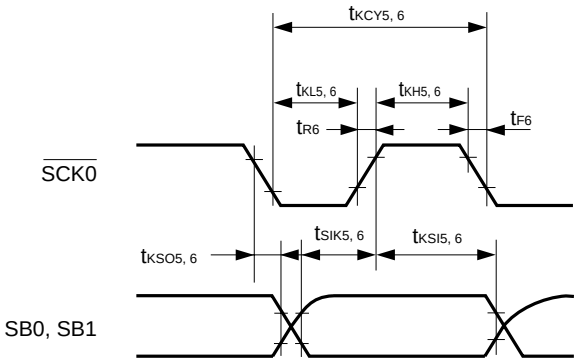
SBI mode (bus release signal transfer) :



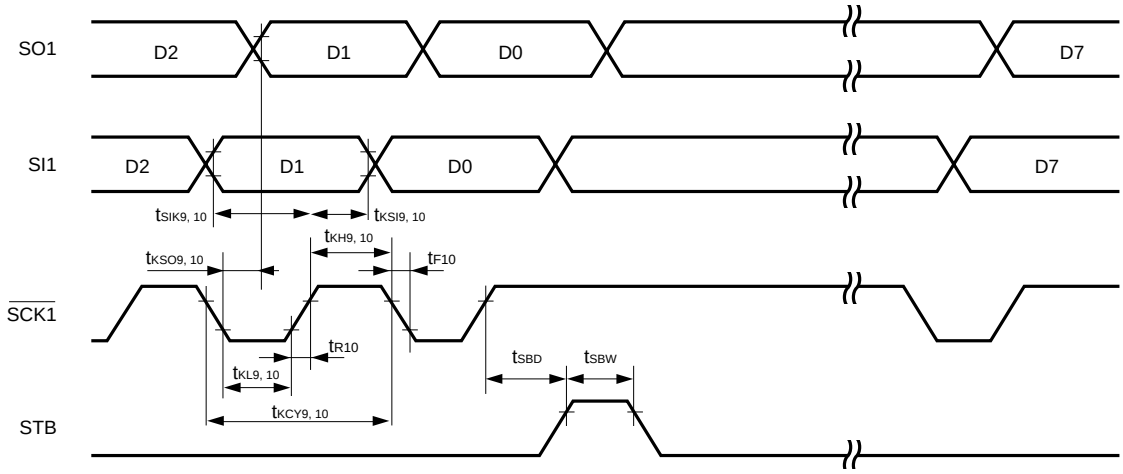
SBI mode (command signal transfer) :



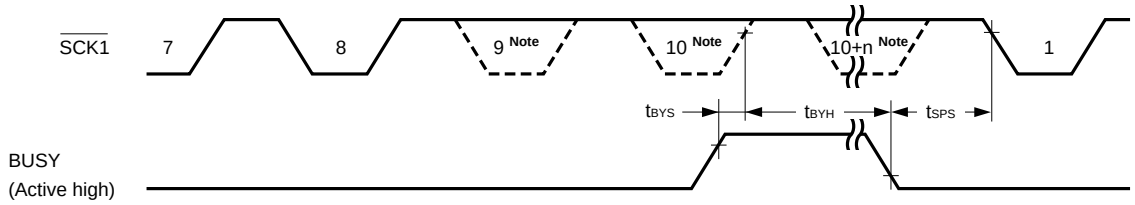
2-wire serial I/O mode :



3-wire serial I/O mode with automatic transmit/receive function :

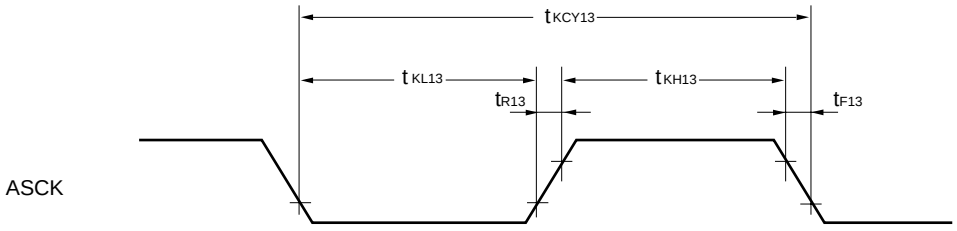


3-wire serial I/O mode with automatic transmit/receive function (busy processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART mode (external clock input) :



A/D Converter Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]					±1.0	%
Conversion time	t_{CONV}		16		100	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		AV_{DD}	V
AV_{REF0} current	I_{REF0}	When A/D converter is operating[Note 2]		500	1500	μA
		When A/D converter is not operating[Note 3]		0	3	μA
Resistance between AV_{REF0} and AV_{SS}	R_{REF0}	When A/D conversion is not performed	4	14		kΩ

Notes 1. Overroll error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.
2. The current flowing to AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 1.
3. The current flowing to AV_{REF0} pin when bit 7 (CS) of the A/D converter mode regidter (ADM) is 0.

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

D/A Converter Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error		R = 2 MΩ[Note 1]				1.2	%
		R = 4 MΩ[Note 1]				0.8	%
		R = 10 MΩ[Note 1]				0.6	%
Settling time		C=30pF[Note 1]	AV_{REF1} = 4.5 to 5.5 V			10	μs
						15	μs
Output resistance	R_O	**Note 2**			8		kΩ
Analog reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note 2**				2.5	mA
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]		4	8		kΩ

Notes 1. R and C denote D/A converter output pin load resistance and load capacitance, respectively.
2. Value for 1 D/A converter channel

Remark DACS0 and DACS1: D/A conversion value setting register 0 and 1

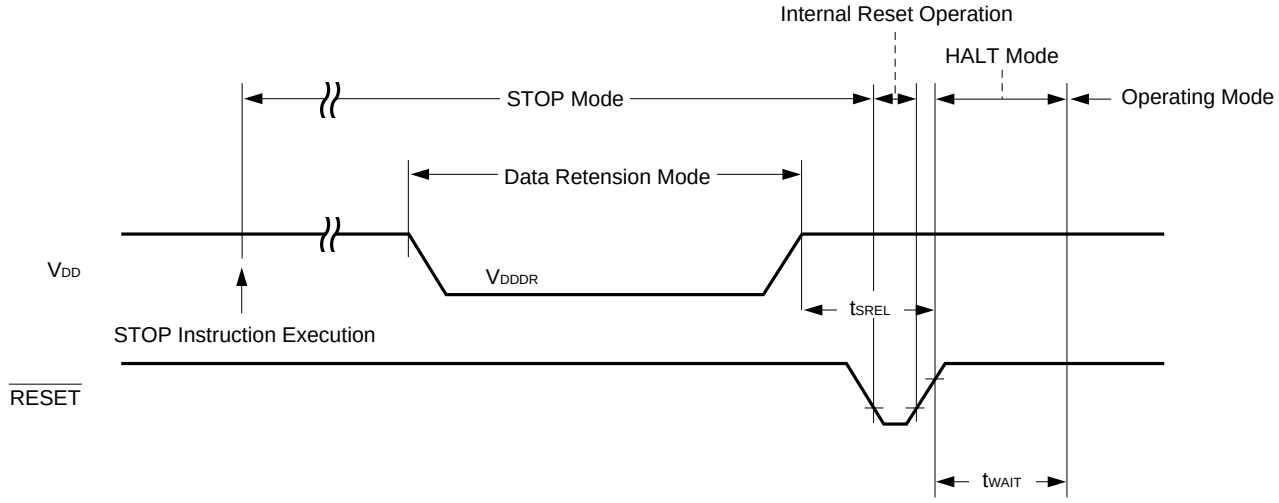
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabiliation wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt		**Note**		ms

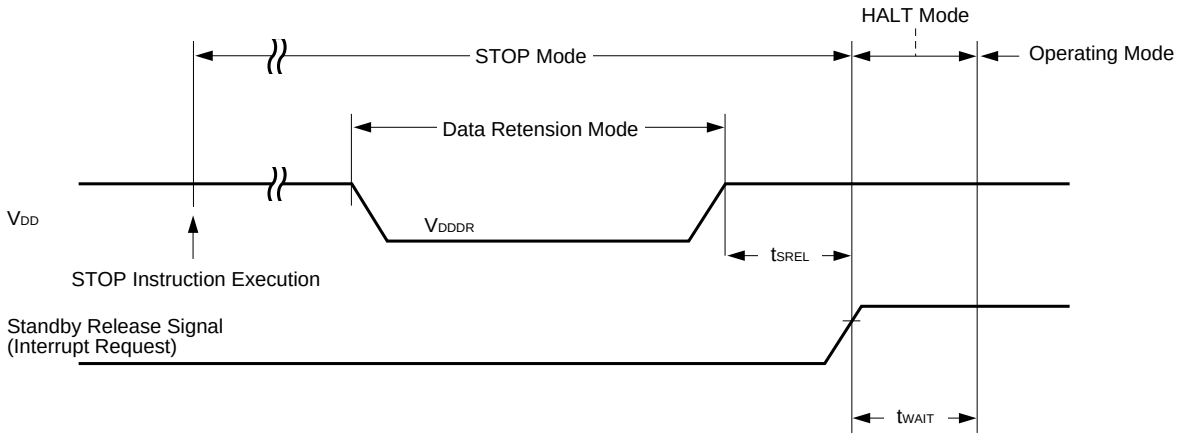
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS) , selection of 2^{12}/fxx and 2^{14}/fxx to 2^{17}/fxx is possible.

Remark fxx: Main system clock frequency (fx or fx/2)
fx : Main system clock oscillatior frequency

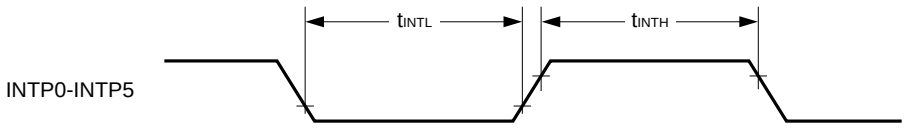
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



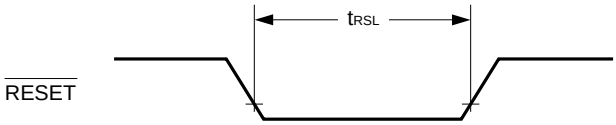
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Input Timing

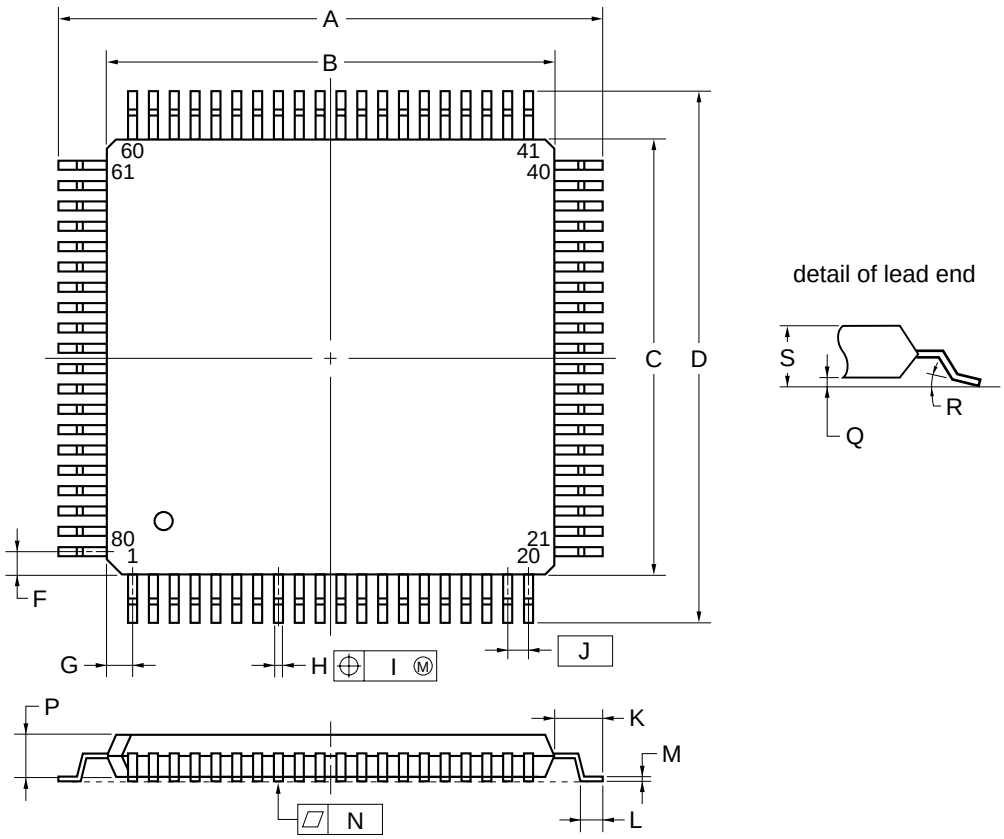


$\overline{\text{RESET}}$ Input Timing



12. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



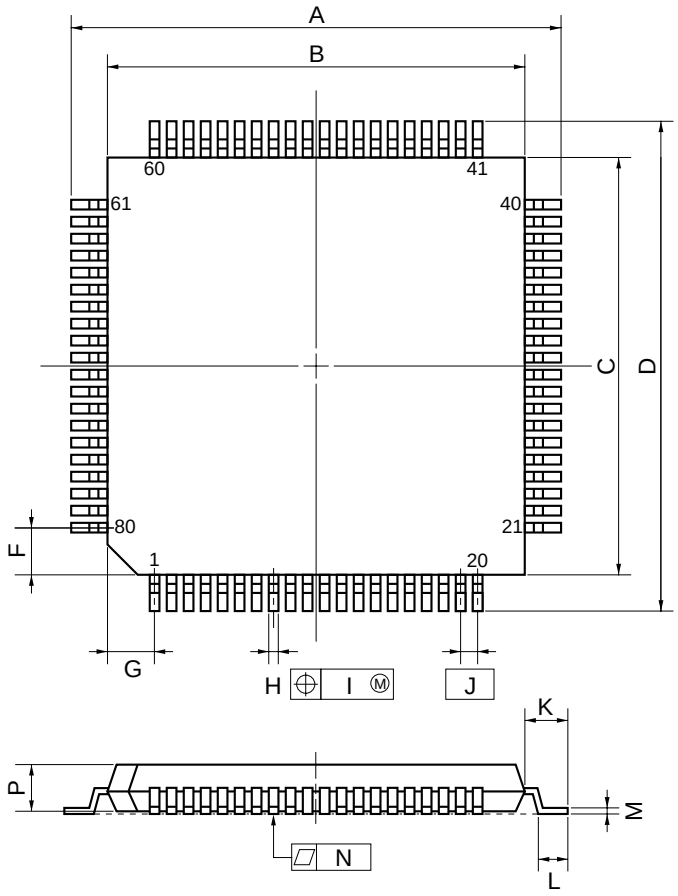
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

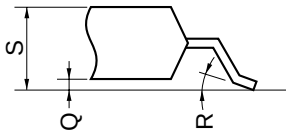
ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

★APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD780058 subseries. Refer to **(5) Cautions when the development tools are used.**

(1) Language processing software

RA78K/0	78K/0 series common assembler package
CC78K/0	78K/0 series common C compiler package
DF780058	Device file for the μPD780058 subseries
CC78K/0-L	78K/0 series common C compiler library source file

(2) Flash memory writing tools

Flashpro II (Part number: FL-PR2)	Dedicated flash programmer for microcomputers incorporating flash memory
FA-80GC[Note] FA-80GK[Note]	Adapter for flash memory writing

Note Under development

(3) Debugging tools

- **When using the IE-78K0-NS in-circuit emulator**

IE-78K0-NS[Note]	78K/0 series common in-circuit emulator
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C[Note]	Interface adapter necessary when a PC-9800 series computer (except notebook-type personal computer) is used as host machine
IE-70000-CD-IF[Note]	PC card and interface cable necessary when a PC-9800 series notebook-type personal computer is used as host machine
IE-70000-PC-IF-C[Note]	Interface adapter necessary when an IBM PC/AT™ or a compatible machine is used as host machine
IE-780308-NS-EM1[Note]	Emulation board common to the μPD780308 subseries
NP-80GC[Note]	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NP-80GK[Note]	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
TGK-080SDW	Conversion adapter to connect the board of the target system to be mounted on 80-pin plastic TQFP (GK-BE9 type) and NP-80GK
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-8BT type)
ID78K0-NS[Note]	Integrated debugger for IE-78K0-NS
SM78K0	78K/0 series common system simulator
DF780058	Device file for the μPD780058 subseries

Note Under development

- **When using the IE-78001-R-A in-circuit emulator**

IE-78001-R-A[Note]	78K/0 series common in-circuit emulator
IE-70000-98-IF-B IE-70000-98-IF-C[Note]	Interface adapter necessary when a PC-9800 series computer (except notebook-type personal computer) is used as host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C[Note]	Interface adapter necessary when an IBM PC/AT or a compatible machine is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as host machine
IE-780308-NS-EM1[Note] IE-780308-R-EM	Emulation board common to the μPD780308 subseries
IE-78K0-R-EX1[Note]	Emulation probe conversion board necessary when the IE-780308-NS-EM1 is used in the IE-78001-R-A.
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EP-78054GK-R	Emulaiton probe for 80-pin plastic TQFP (GK-BE9 type)
TGK-080SDW	Conversion adapter to connect the board of the target system to be mounted on 80-pin plastic TQFP (GK-BE9 type) and EP-78054GK-R
EV-9200GC-80	Socket to be mounted on the board of the target system made for the 80-pin plastic QFP (GC-8BT type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	78K/0 series common system simulator
DF780058	Device file for the μPD780058 subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 series
MX78K0	OS for 78K/0 series

(5) Cautions when the development tools are used

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780058.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF780058.
- Flashpro II, FA-80GC, FA-80GK, NP-80GC, and NP-80GK are products of Naito Densei Machida Mfg. Co., Ltd. (TEL: (044)822-3813). Contact an NEC distributor when purchasing these products.
- TGK-080SDW is a product of Tokyo Eletech Corp.
  Inquiry : Daimaru Kogyo, Ltd. Electronics Dept. (TEL: Tokyo (03) 3820-7112)
  Electronics 2nd Dept. (TEL: Osaka (06) 244-6672)
- Refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.
- Host machines and OSs compatible with the software are as follows:

Host Machine [OS] / Software	PC PC-9800 Series [Windows™] IBM PC/AT and compatible machines [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	○Note	○
CC78K/0	○Note	○
ID78K0-NS	○	–
ID78K0	○	○
SM78K0	○	–
RX78K/0	○Note	○
MX78K0	○Note	○

Note DOS based software

★ APPENDIX B. RELATED DOCUMENTS

Documents Related Devices

Document Name	Document No.	
	Japanese	English
μPD780058, 780058Y Subseries User's Manual	U12013J	U12013E
μPD780053, 780054, 780055, 780056, 780058 Data Sheet	U12182J	This document
μPD78F0058 Preliminary Product Information	U12092J	U12092E
78K/0 Series User's Manual - Instruction	U12326J	U12326E
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—

Development Tool Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
RA78K Series Structured Assembler Preprocessor		U12323J	EEU-1402
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-How	U13034J	U13034E
CC78K Series Library Source File		U12322J	—
IE-78K0-NS		Planned	Planned
IE-78001-R-EM		Planned	Planned
IE-780308-NS-EM1		Planned	Planned
IE-780308-R-EM		U11362J	U11362E
EP-78230		EEU-985	EEU-1515
EP-78054GK-R		EEU-932	EEU-1468
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0-NS Integrated Debugger PC Based	Reference	U12900J	Planned
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing your system.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Fundamentals	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257J	U12257E

Other Related Documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality/Reliability Handbook	C12769J	—
Microcomputer Product Series Guide	U11416J	—

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing your system.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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800-366-9782
Fax: 408-588-6130
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