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FUJITSU

DATA SHEET

MB87078

6-bit, 4-channel Electronic Volume Controller

The Fujitsu MB87078 is a 6-bit, 4-channel electronic volume controller. A digital signal input controls gain every 0.5 dB step from 0dB to −32dB. It has been fabricated in CMOS technology and designed to operate with low power. Its digital inputs and outputs are TTL compatible.

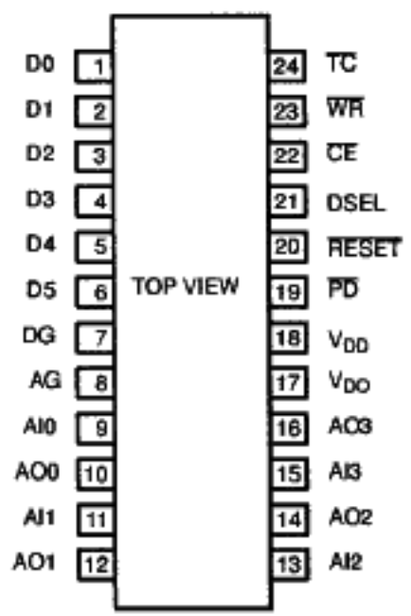
The MB87078 is available in 24-pin plastic DIP and 24-pin SOP packages.

- Gain variable range: 0 dB to −32 dB by 0.5dB or − ∞
- Gain variable range is expanded to connect two channels serially (0 dB to −64 dB)
- Each channel gain can be set respectively
- Low power consumption: 8.5 mW at +5 V
- Easy microprocessor interface (6-bit parallel I/O)
- Test function is provided (to confirm internal data)
- Data is initialized by reset signal (all channels are set to 0db)
- Single power supply: +5 V
- Logic I/O is TTL compatible
- Package and ordering information:
  - 24-pin plastic DIP, order as MB87078P
  - 24-pin plastic SOP, order as MB87078PF

Plastic DIP
(DIP-24P-M03)

Plastic SOP
(FPT-24P-M02)

Pin Assignment



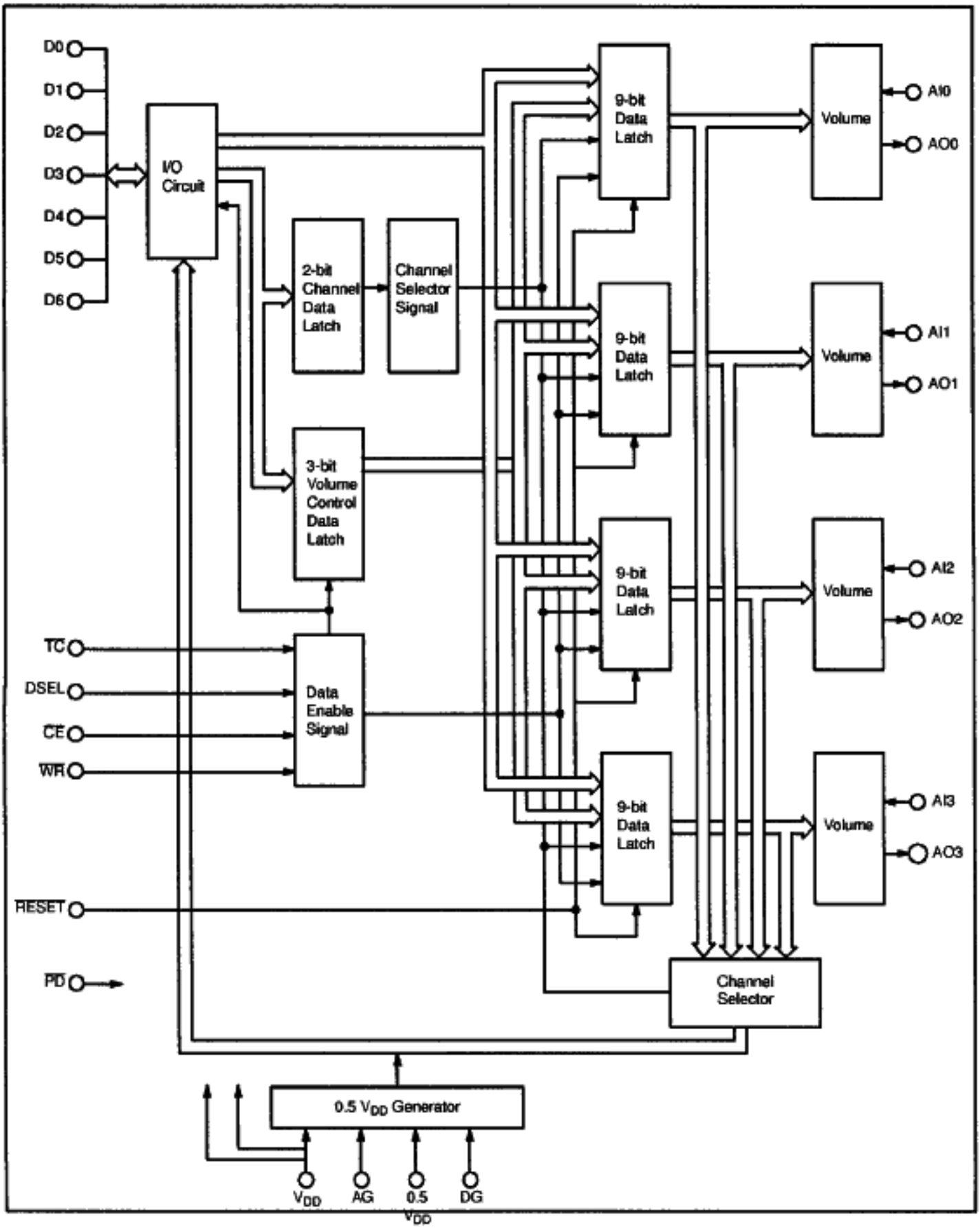
ABSOLUTE MAXIMUM RATINGS

Pareameter	Symbol	Pin Name	Value	Unit
Power Supply Voltage	V_{DD}	V_{DD}	−0.3 to +6	V
Digital Input Voltage	V_{DI}	All digital input pins	−0.3 to V_{DD} +0.3	V
Analog Input Voltage	V_{AI}	A_{10} to A_{13}	−0.3 to V_{DD} +0.3	V
Digital Output Voltage	V_{DO}	All digital output pins	−0.3 to V_{DD} +0.3	V
Analog Output Voltage	V_{AO}	A_{08} to A_{03}	−0.3 to V_{DD} +0.3	V
Digital Output Current	I_{DO}	All digital output pins	−10 to 10	mA
Analog Output Current	I_{AO}	A_{00} to A_{03}	−10 to 10	mA
Storage Temperature	T_{STG}		−40 to +125	°C

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



PIN DESCRIPTIONS

	Pin No.	Pin Name	Description
Power Supply	18	V_{DD}	Positive supply voltage, +5V
	8	AG	Ground for analog circuitry
	7	DG	Ground for digital circuitry
Digital Input	21	DSEL	Data select input (TTL interface). When this pin is set at high level, DSC1, DSC2, EN, C0 and C32 are in the write enable mode. When this pin is set at low level, GD0 to GD5 are in the write enable mode.
	22	$\overline{CE}$	Chip enable input (TTL interface). When this pin is set at low level, data input/output is available. When this pin is at high level, data input/output is inhibited and the pin is set to a high impedance state. This pin is pulled up by a high resistance.
	23	$\overline{WR}$	Data write clock input (TTL interface). Data is written at every rising edge of this clock.
	24	$\overline{TC}$	Digital signal input/output select input (TTL interface). When this pin is at high level, data can be written through D0 to D5. When this pin is at low level, data can be read output from D0 to D5. This pin is pulled up by a high resistance.
	19	$\overline{PD}$	Power down select input (TTL interface). When this pin is at low level, the power down mode is selected. When this pin is at high level, the operation mode is selected. This pin is pulled up by a high resistance.
	20	$\overline{RESET}$	Reset input (TTL interface). When this pin is at low level, the data latches for all channels are initialized and the value is set as 0 dB. This pin is pulled up by a high resistance.

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PIN DESCRIPTIONS

	Pin No.	Pin Name	Description
Digital I/O Pins	1	D0	When $\overline{TC}$ = H and $\overline{CE}$ = L, data can be written through D0 to D5. When $\overline{TC}$ = L and $\overline{CE}$ = L, data can be read out from D0 to D5. When DSEL is at high level, DSC1, DSC2, EN, C0 and C32 are in the read/write enable modes. When DSEL is at low level, GD0 to GD5 are in the read/write enable modes.
	2	D1	
	3	D2	
	4	D3	
	5	D4	
	6	D5	

Channel Setting

DSC2	DSC1	Channel
L	L	0
L	H	1
H	L	2
H	H	3

Digital I/O Setting

$\overline{TC}$	DSEL	D0	D1	D2	D3	D4	D5	I/O Modes
H	H	DSC	DSC	EN	C0	C32	X	Input mode (setting)
	L	GD0	GD1	GD2	GD3	GD4	GD5	
L	H	DSC	DSC	EN	C0	C32	L	Output mode (check)
	L	GD0	GD1	GD2	GD3	GD4	GD5	

Electrical Volume Setting

Data*										Gain (dB)
GD5	GD4	GD3	GD2	GD1	GD0	EN	C0	C32	D (G)	
1	1	1	1	1	1	1	0	0	63	0
1	1	1	1	1	0	1	0	0	62	−0.5
1	1	1	1	0	1	1	0	0	61	−1
1	1	1	1	0	0	1	0	0	60	−1.5
1	1	1	0	1	1	1	0	0	59	−2
1	1	1	0	1	0	1	0	0	58	−2.5
1	1	1	0	0	1	1	0	0	57	−3
1	1	1	0	0	0	1	0	0	56	−3.5
1	0	0	0	0	0	1	0	0	32	−15.5
0	1	1	1	1	1	1	0	0	31	−16
0	0	0	1	1	1	1	0	0	7	−28
0	0	0	1	1	0	1	0	0	6	−28.5
0	0	0	1	0	1	1	0	0	5	−29
0	0	0	1	0	0	1	0	0	4	−29.5
0	0	0	0	1	1	1	0	0	3	−30
0	0	0	0	1	0	1	0	0	2	−30.5
0	0	0	0	0	1	1	0	0	1	−31
0	0	0	0	0	0	1	0	0	0	−31.5
X	X	X	X	X	X	1	X	1	–	−32
X	X	X	X	X	X	1	1	0	–	0
X	X	X	X	X	X	0	X	X	–	−∞

* X = don't care.
When data is reset, data is set at 0 dB (code 111111100)

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PIN DESCRIPTIONS

	Pin No.	Pin Name	Description
Analog Input	9	AI0	Analog input of channel 0.
	11	AI1	Analog input of channel 1.
	13	AI2	Analog input of channel 2.
	15	AI3	Analog input of channel 3.
Analog Output	10	AO0	Analog output of channel 0. When in a power down mode, this pin is pulled down by a high resistance.
	12	AO1	Analog output of channel 1. When in a power down mode, this pin is pulled down by a high resistance.
	14	AO2	Analog output of channel 2. When in a power down mode, this pin is pulled down by a high resistance.
	16	AO3	Analog output of channel 3. When in a power down mode, this pin is pulled down by a high resistance.
	17	$0.5V_{DD}$	Output pin of a half level of V_{DD}. A condenser is usually connected between this pin and the AG pin.

TRUTH TABLE

PD	RESET	CE	TC	DSEL	WR	D0 to D5	Operator Mode
0	X	X	X	X	X		Power down mode
1	0	X	X	X	X		Gain is initialized
1	1	1	X	X	X	Inhibit data input/output (high impedance)	
1	1	0	0	1	X	Data stored in SCH1, SCH2, EN, C0, and C32 are output	Data output mode
1	1	0	0	0	X	Data stored in D0 to D5 are output	Data output mode
1	1	0	1	1	⌐↓	Data stored in SCH1, SCH2, EN, C0, and C32 are input	Data output mode
1	1	0	1	0	⌐↓	Data stored in D0 to D5 are input	Data output mode

Note: X = don't care.

Figure 2. Volume Data Setting Timing Diagram

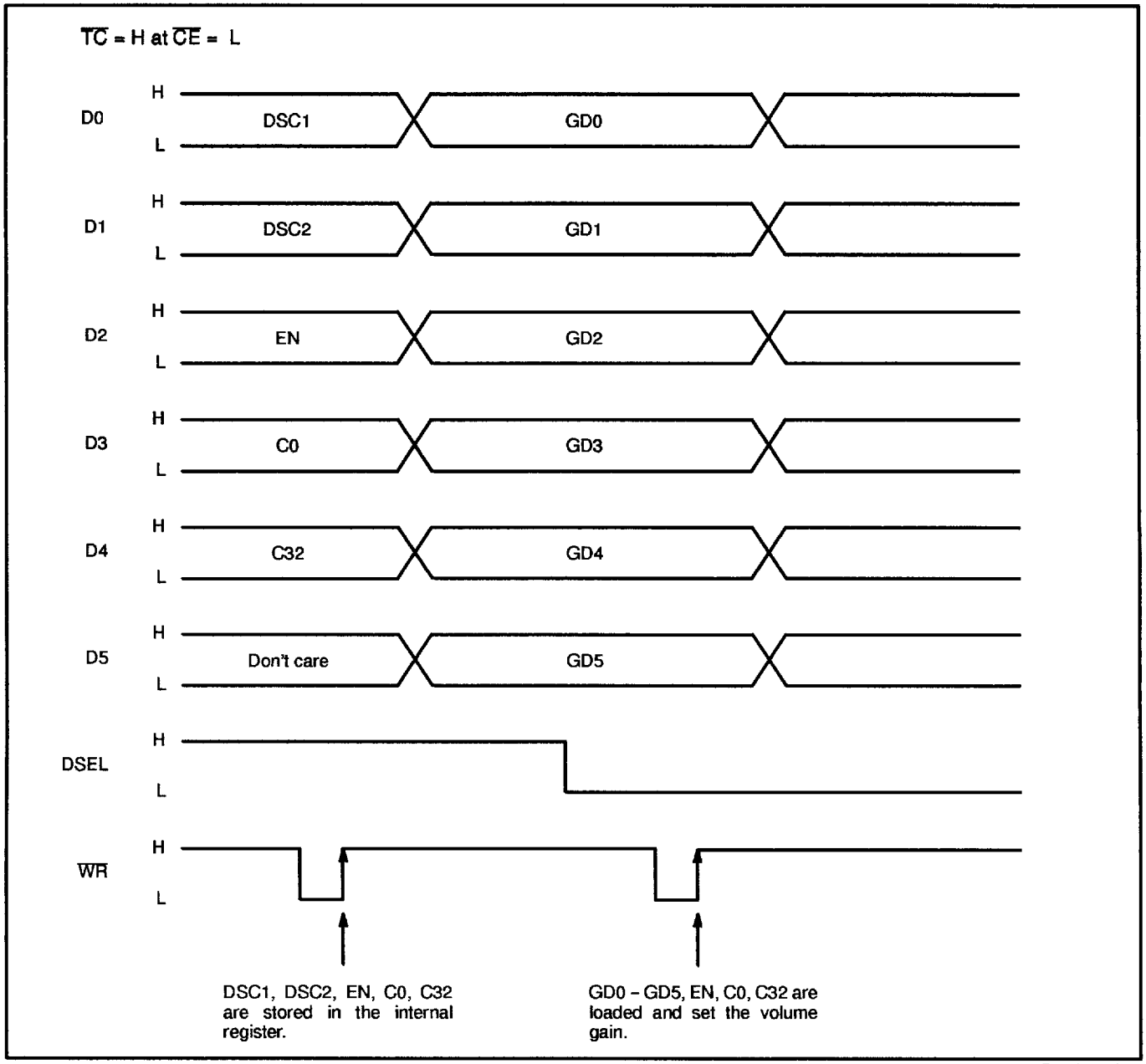

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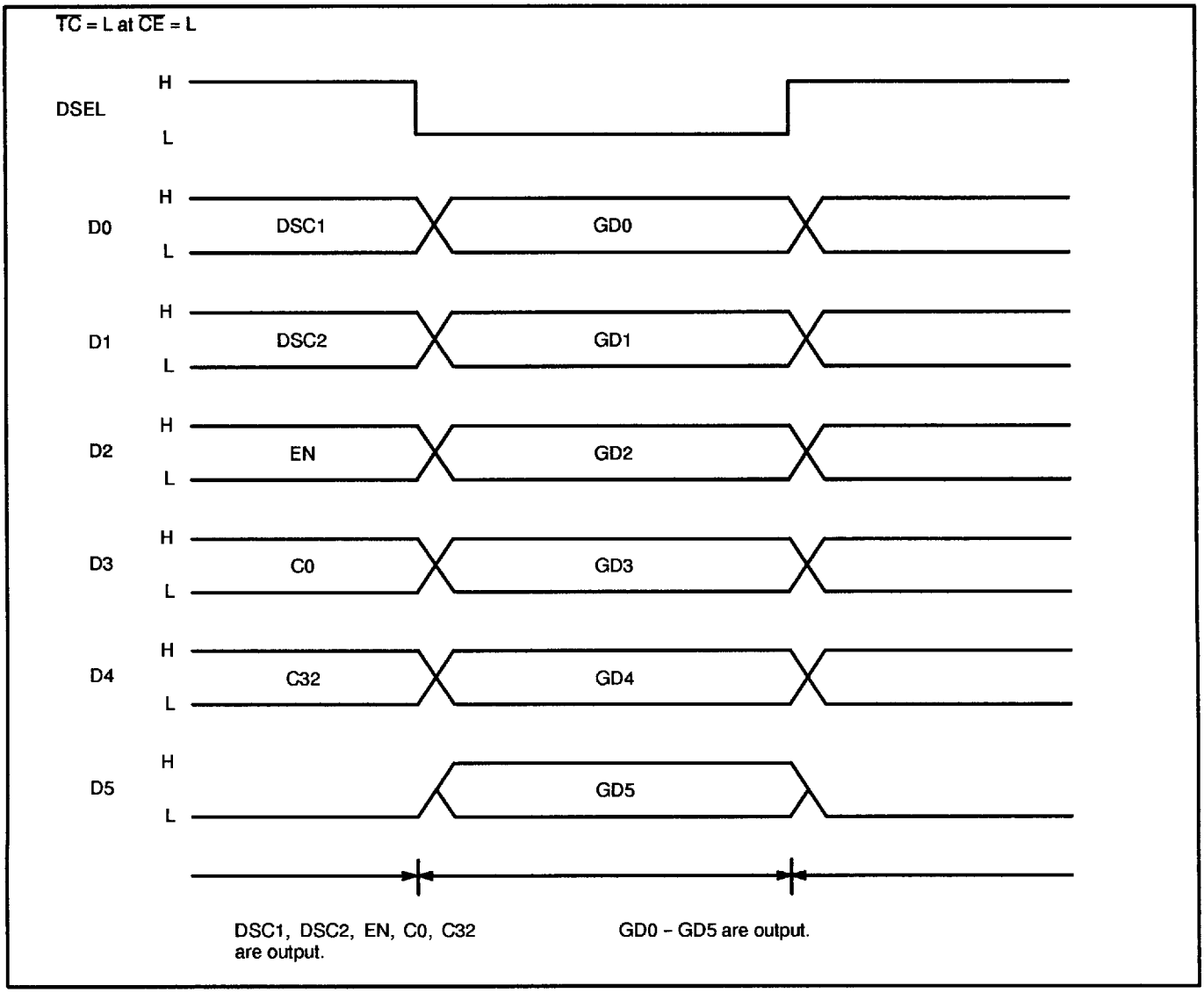
Figure 2. Volume Data Setting Timing Diagram



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name		Value			Unit
				Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}		4.75	5.0	5.25	V
Digital Input Voltage	V_{DI}	All digital input pins		0		V_{DD}	V
Analog Input Voltage	V_{AI}	All analog input pins	±5 V ±5%	1.25		V_{DD} −1.25	V
Analog Output Load Resistance	R_{AL}	AO0 – AO3		30			kΩ
Analog Output Load Capacitance	C_{AL}	AO0 – AO3				50	pF
Operating Temperature	T_A			−20		70	°C
Analog Input Frequency	f_{AI}			0		20	kHz

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5 V +5%, V_{SS} = −5 V + 5%, T_A = −20 to +70°C, dBm referenced to 600 Ω)

Parameter	Symbol	Pin Name	Condition		Value			Unit
					Min	Typ	Max	
Power Supply Current	I_{DD1}	V_{DD}	No Load	$\overline{PD}$ = H		1.2	2.0	mA
	I_{DD2}			$\overline{PD}$ = L			0.5	mA
Digital Input Low Voltage	V_{IL}	All digital input pins			0		0.8	V
Digital Input High Voltage	V_{IH}				2.2		V_{DD}	V
Digital Input Low Current	I_{IL}	D0 – D5 $\overline{WR}$, DSEL	V_I = GND		−10		10	µA
Digital Input High Current	I_{IH}		V_I = V_{DD}		−10		10	µA
Digital Output Low Voltage	V_{OL}	All digital output pins	I_{OL} = 2mA		0		0.4	V
Digital Output High Voltage	V_{OH}		I_{OH} = 2mA		2.6		V_{DD}	V
Supply Deviation Rejection Ratio	S_{VR}	V_{DD}, A0–A3	Supply Voltage Deviation ΔV_{SV} = ±150 mV (DC)		50			dB

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value Min	Value Typ	Value Max	Unit
Pull up Current	I_{PLU}	$\overline{\text{RESET}}$, TC $\overline{\text{PD}}$, $\overline{\text{CE}}$	V_I = GND	−100	−50	−25	µA
Analog Input Resistance	R_{AIN}	All Analog Output Pins		100	150	300	kΩ
Analog Output Voltage	V_{AO}	A0 – A3	Offset Voltage	−25	0	25	mV
			AC Volt. ±5 V ±5%	0		V_{DD} −2.5	Vp-p
Analog Output Maximum Gain	G_{MAX}		Analog Input 2.5 Vp-p, Gain code "111111"	−0.5	0	+0.5	dB
Analog Output Step	ΔG		Analog Input 2.5 Vp-p, 63>D(G)≥0	0.25	0.5	0.75	dB
Analog Output Gain	G		Below 20 kHz, 63>D(G)≥0	(Typ)−1	$\frac{D(G)-63}{2}$	(Typ)+1	dB
Harmonic Noise	N_{HH}		Input = 2.5 Vp-p 1 kHz, G = 0dB	60	80		dB
Output Noise	N_{IC1}		*Input = 0V, G = 0dB BW = 0.3 kHz – 20 kHz			−65	dBm
	N_{IC2}		*Input = 0V G = 0dB BW = 0.3 kHz – 3.4 kHz			−70	dBm
Cross Talk between Channels	N_{CT}		1 channel AIN = 2.5 Vp-p Remaining channels AIN = GND G = 0dB (N = 0 – 3)	70	80		dB

*A condenser (1µF) is connected between pins 8 and 17.

AC CHARACTERISTICS

(V_{DD} = +5 V +5%, V_{SS} = −5 V +5%, T_A = −20 to +70°C, dBm referenced to 600 Ω)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
$\overline{WR}$ High Width	t_{WHWR}	$\overline{WR}$	500			ns
$\overline{WR}$ Low Width	t_{WLWR}	$\overline{WR}$	500			ns
DATA Set up Time	t_{SD}	D0 – D5, $\overline{WR}$	200			ns
DSEL Set up Time	t_{SDS}	DSEL, $\overline{WR}$	200			ns
$\overline{TC}$ Set up Time	t_{STC}	$\overline{TC}$, $\overline{WR}$	200			ns
$\overline{CE}$ Set up Time	t_{SCE}	$\overline{CE}$, $\overline{WR}$	200			ns
DATA Hold Time	t_{HD}	D0 – D5, $\overline{WR}$	200			ns
DSEL Hold Time	t_{HDS}	DSEL, $\overline{WR}$	200			ns
$\overline{TC}$ Hold Time	t_{HTC}	$\overline{TC}$, $\overline{WR}$	200			ns
$\overline{CE}$ Hold Time	t_{HCE}	$\overline{CE}$, $\overline{WR}$	200			ns
Rise Time 1	t_{r1}	$\overline{WR}$	0		20	ns
Fall Time 1	t_{f1}	$\overline{WR}$	0		20	ns
Rise Time 2	t_{r2}	D0 – D5, $\overline{CE}$, $\overline{TC}$, DSEL	0		20	ns
Fall Time 2	t_{f2}	D0 – D5, $\overline{CE}$, $\overline{TC}$, DSEL	0		20	ns
Digital Input Low Width	t_{WLRP}	$\overline{RESET}$, $\overline{PD}$	1			µs
DATA Output Enable Switching Time 1	t_{DOE1}	$\overline{TC}$, D0 – D5			500	ns
DATA Output Enable Switching Time 2	t_{DOE2}	$\overline{TC}$, D0 – D5			500	ns
DATA Output Switching Time	t_{DCH}	$\overline{DSEL}$ D0 – D5			500	ns

Note: Please refer to the timing diagram for test conditions.

Figure 3. Timing Diagram

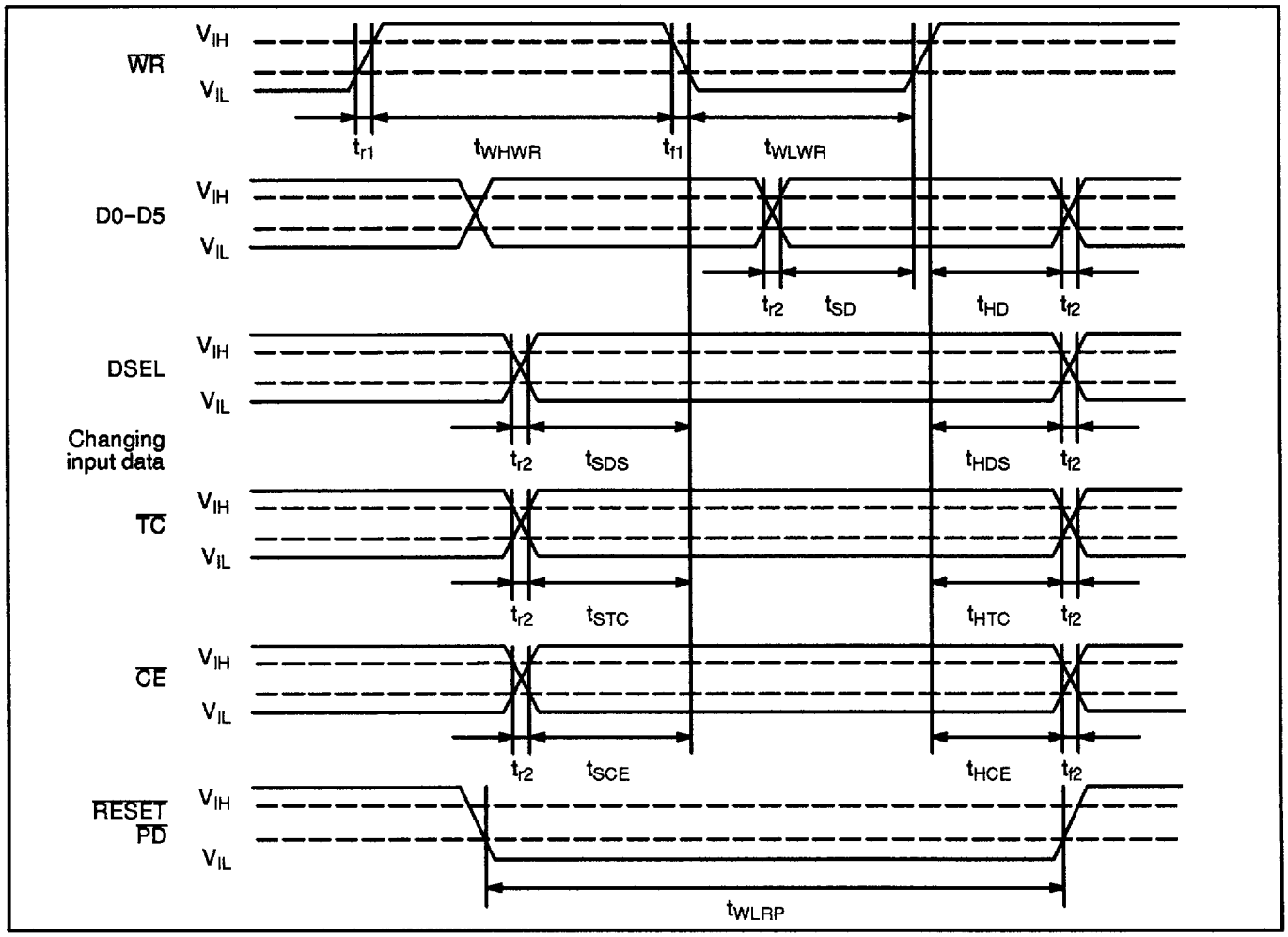


Figure 4. Timing Diagram ($\overline{CE}$ = L)

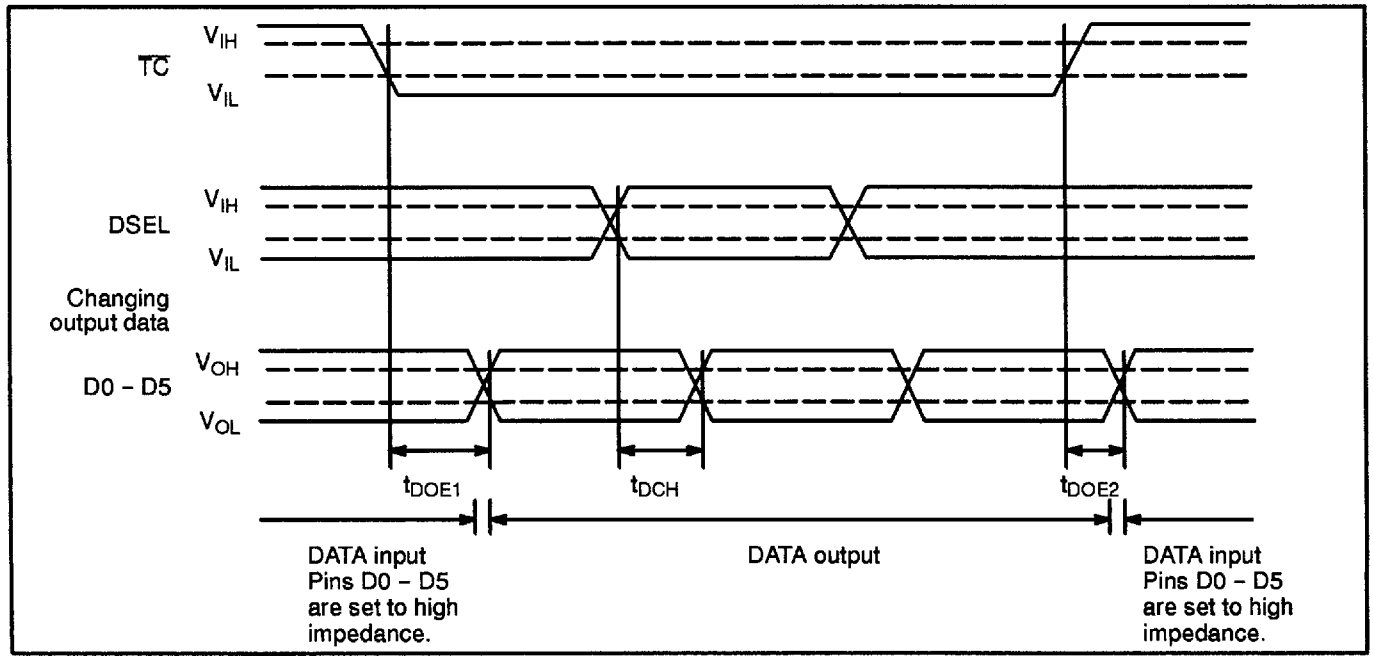
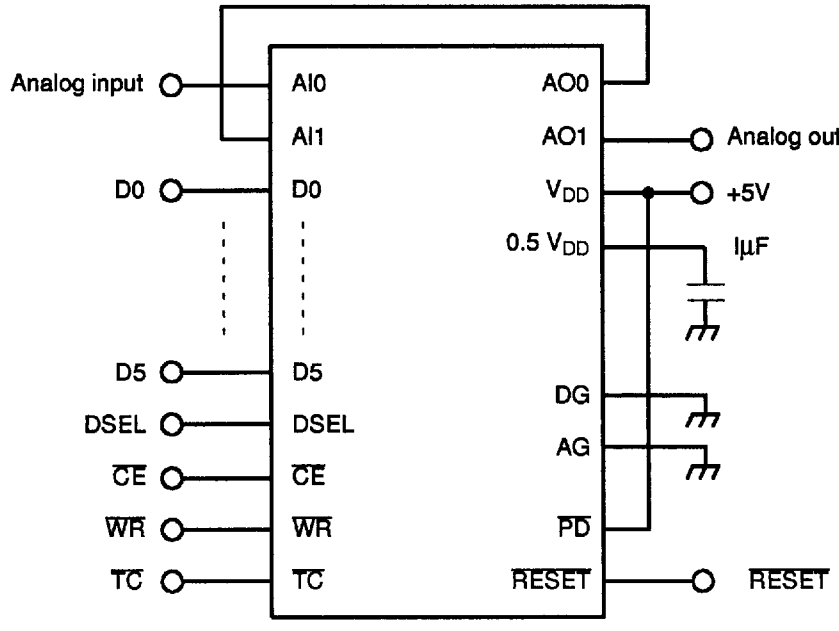


Figure 5. Application Example

Gain variable range is expanded (0 db to −64 dB by 0.5 dB steps) if two channels are connected in series.



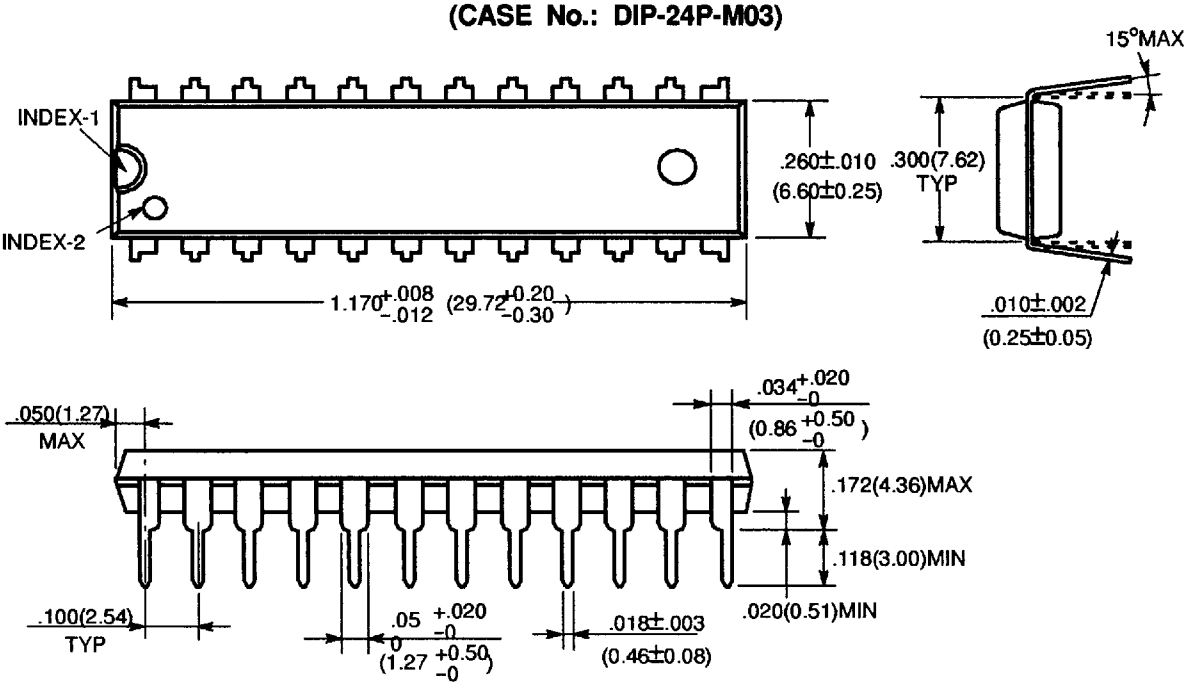
Setting Data

Setting Gain (dB)	Data Set (channel 0)									Data Set (channel 1)								
	GD5	GD4	GD3	GD2	GD1	GD0	EN	C0	C32	GD5	GD4	GD3	GD2	GD1	GD0	EN	C0	C32
0	X	X	X	X	X	X	1	1	0	1	1	1	1	1	1	1	0	0
−0.5	X	X	X	X	X	X	1	1	0	1	1	1	1	1	0	1	0	0
−1.0	X	X	X	X	X	X	1	1	0	1	1	1	1	0	1	1	0	0
⋮					⋮									⋮				
−31.0	X	X	X	X	X	X	1	1	0	0	0	0	0	0	1	1	0	0
−31.5	X	X	X	X	X	X	1	1	0	0	0	0	0	0	0	1	0	0
−32.0	1	1	1	1	1	1	1	0	0	X	X	X	X	X	X	1	0	1
−32.5	1	1	1	1	1	0	1	0	0	X	X	X	X	X	X	1	0	1
−33.0	1	1	1	1	0	1	1	0	0	X	X	X	X	X	X	1	0	1
⋮					⋮									⋮				
−63.0	0	0	0	0	0	1	1	0	0	X	X	X	X	X	X	1	0	1
−63.5	0	0	0	0	0	0	1	0	0	X	X	X	X	X	X	1	0	1
−64.0	X	X	X	X	X	X	1	0	1	X	X	X	X	X	X	1	0	1

Note: X = don't care.

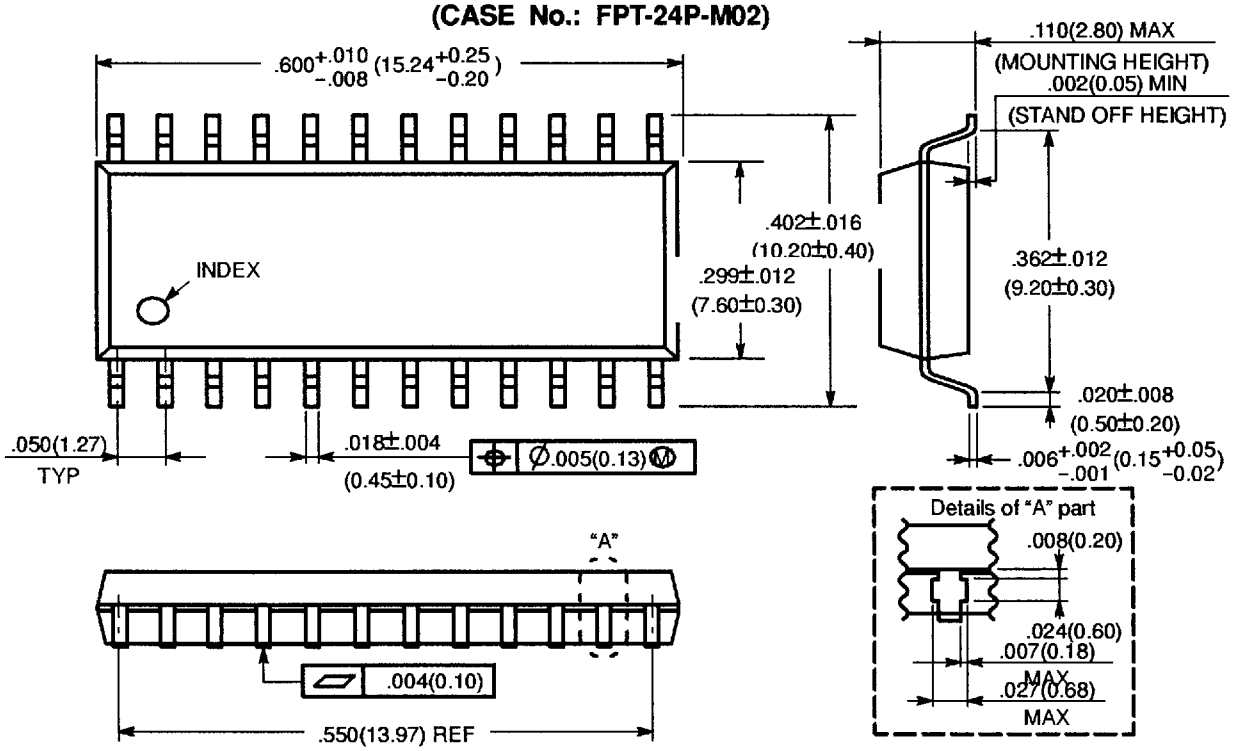
PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



Dimensions in inches (millimeters)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in inches (millimeters)