DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4502B
buffers
Strobed hex inverter/buffer

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Strobed hex inverter/buffer

HEF4502B buffers

DESCRIPTION

The HEF4502B consists of six inverter/buffers with 3-state outputs. When the output enable input ($\overline{EO}$) is HIGH all six outputs (O_1 to O_6) are in the high impedance OFF-state. When the enable input ($\overline{E}$) is HIGH all six outputs are switched to LOW. The outputs have a 2-TTL load drive capability.

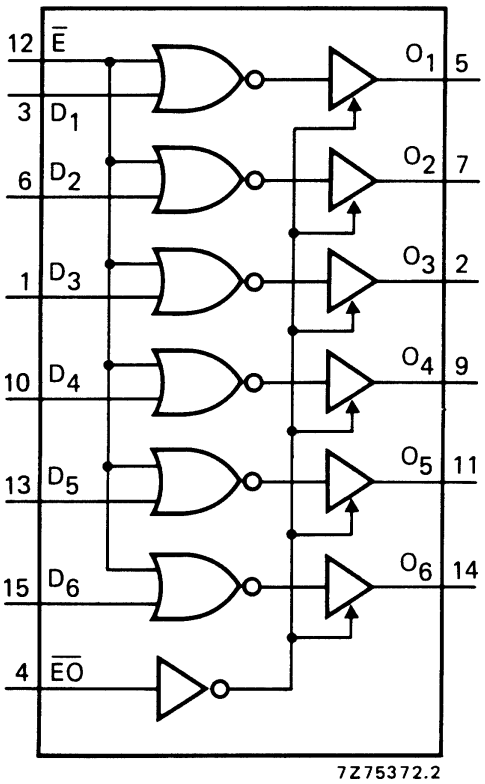

Fig.1 Functional diagram.

TRUTH TABLE

INPUTS			OUTPUT
D_n	$\overline{E}$	$\overline{EO}$	O_n
L	L	L	H
H	L	L	L
X	H	L	L
X	X	H	Z

Notes

1. H = HIGH state (the more pos. voltage)
   L = LOW state (the less pos. voltage)
   X = state is immaterial
   Z = high impedance off state

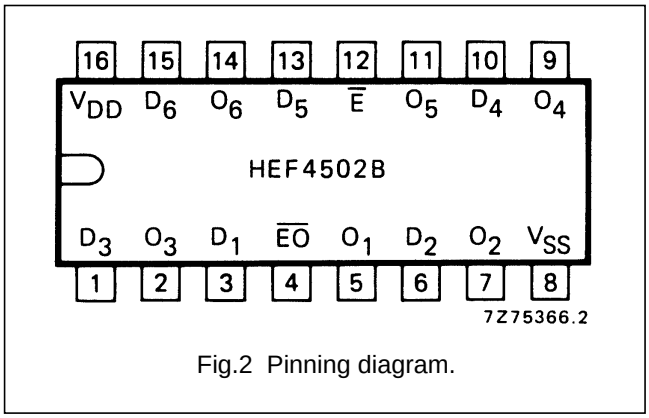

Fig.2 Pinning diagram.

HEF4502BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4502BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4502BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

D_1 to D_6	data inputs
$\overline{E}$	enable input
$\overline{EO}$	output enable input
O_1 to O_6	3-state outputs

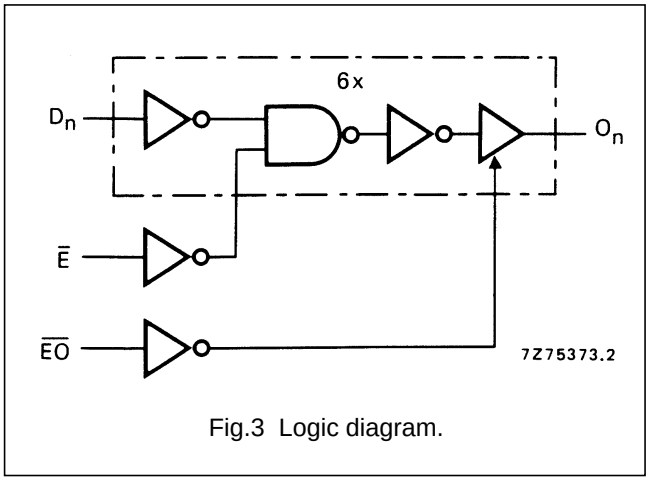

Fig.3 Logic diagram.

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	T_{amb} (°C)						
					−40		+ 25		+ 85		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output current	5	4,6			1,2		1,0		0,8		mA
HIGH	10	9,5		$-I_{OH}$	3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
Output current											
HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current	4,75		0,4		3,5		2,9		2,3		mA
LOW	10		0,5	I_{OL}	12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$5\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$25\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$85\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays					
D_n, $\overline{E} \rightarrow O_n$	5		85	170 ns	77 ns + (0,17 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	80 ns	37 ns + (0,06 ns/pF) C_L
	15		35	70 ns	33 ns + (0,04 ns/pF) C_L
	5		80	160 ns	66 ns + (0,28 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70 ns	28 ns + (0,13 ns/pF) C_L
	15		30	60 ns	25 ns + (0,10 ns/pF) C_L
Output transition times	5		25	50 ns	10 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	12	24 ns	7 ns + (0,11 ns/pF) C_L
	15		8	15 ns	5 ns + (0,07 ns/pF) C_L
	5		30	60 ns	5 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	15	30 ns	3 ns + (0,24 ns/pF) C_L
	15		12	24 ns	3 ns + (0,18 ns/pF) C_L
3-state propagation delays					
Output disable times					
$\overline{EO} \rightarrow O_n$	5		60	160 ns	
HIGH	10	t_{PHZ}	55	140 ns	
	15		55	140 ns	
	5		50	100 ns	
LOW	10	t_{PLZ}	35	70 ns	
	15		30	60 ns	
Output enable times					
$\overline{EO} \rightarrow O_n$	5		60	120 ns	
HIGH	10	t_{PZH}	35	70 ns	
	15		30	60 ns	
	5		55	110 ns	
LOW	10	t_{PZL}	25	50 ns	
	15		20	40 ns	