TC5092AP

TC5092AP C²MOS 13-BIT A/D CONVERTER

GENERAL DESCRIPTION

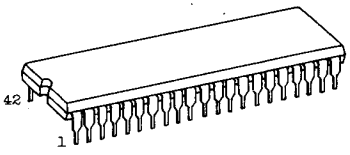
The TC5092AP is an integration 13-bit A/D converter of high precision and low power consumption.
The 13-bit, 3-state data output is capable of independent enable in 4 bits so as to be connected directly to 4-bit/8-bit/12-bit data bus. (LSB is common to lower order 4 bits.)
Further, since this converter has an 8-channel analog multiplexer, and a serial clock output function, it is most suitable as data collection unit of various industrial control instruments.

FEATURES:

- High precision.....±1 LSB(Typ.)
- Low power consumption.....10mW(Typ.)
- Single power supply.....V_{DD}=5V±0.5V
- High-speed conversion.....f_{CP} Max.=5MHz
- 8-channel analog multiplexer contained
- TLL/CMOS compatible digital Input/Output
- Capable of direct connection to 4-/8-/12-bit bus

APPLICATIONS:

- Various industrial control instruments
- Data collection modules



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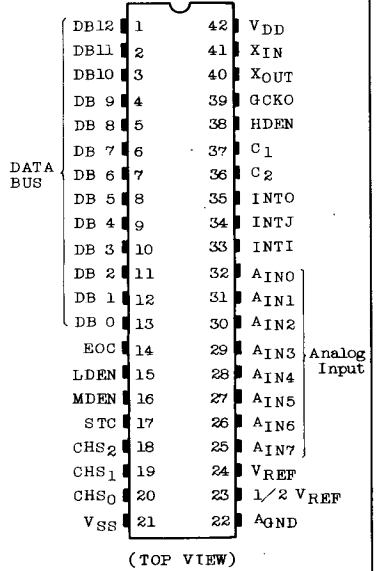
PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

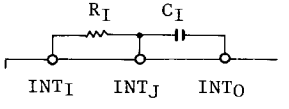
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+7	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Reference Supply Voltage	V_{REF}	V_{AGND} ~ V_{DD}+0.5	V
Analog Ground Voltage	V_{AGND}	V_{SS}-0.5 ~ V_{REF}	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

FUNCTION OF EACH PIN

PIN NO.	Symbol	NAME & FUNCTION
1	DB12	3-State Parallel Data Outputs DB12 : MSB DB 0 : LSB
2	DB11	
3	DB10	
4	DB 9	
5	DB 8	
6	DB 7	
7	DB 6	
8	DB 5	
9	DB 4	
10	DB 3	
11	DB 2	
12	DB 1	
13	DB 0	
14	EOC	End of Conversion EOC goes to "L" level at the fall of STC signal, and returns to "H" level at the end of conversion.
15	LDEN	Low Data Enable $DB_0 \sim DB_4$ are read by "H" level input.
16	MDEN	Medium Data Enable $DB_5 \sim DB_8$ are read by "H" level input.
17	STC	Start Conversion Conversion starts at the fall time, if pulse input at "H" level is provided. "L" level should be kept during conversion.
18	CHS_2	Channel Select Inputs These pins are address inputs for selecting eight analog inputs of AIN0 ~ AIN7, and are taken into the internal latch
19	CHS_1	
20	CHS_0	
21	V_{SS}	Digital Ground
22	AGND	Analog Ground

PIN NO.	Symbol	NAME & FUNCTION
23	$V_{REF/2}$	Reference voltage supply terminal, which supplies the voltage of $\frac{V_{REF} - A_{GND}}{2}$
24	V_{REF}	Reference voltage supply terminal
25	AIN7	Analog input terminal Input voltage range: AGND ~ V_{REF} Arbitrary input can be selected by CHS input.
26	A_{IN6}	
27	A_{IN5}	
28	A_{IN4}	
29	A_{IN3}	
30	A_{IN2}	
31	A_{IN1}	
32	AIN0	
33	INT_I	Integrator Input Integrator Junction Integrator Output The integrator consists of these three terminals.
34	INT_J	
35	INT_O	
36	C_2	Capacitors connection terminals for offset calibration.

CHS_0	CHS_1	CHS_2	A_{IN}
L	L	L	AIN0
H	L	L	AIN1
L	H	L	AIN2
H	H	L	AIN3
L	L	H	AIN4
H	L	H	AIN5
L	H	H	AIN6
H	H	H	AIN7



R_I and C_I should satisfy the following formula and be set as small a value as possible

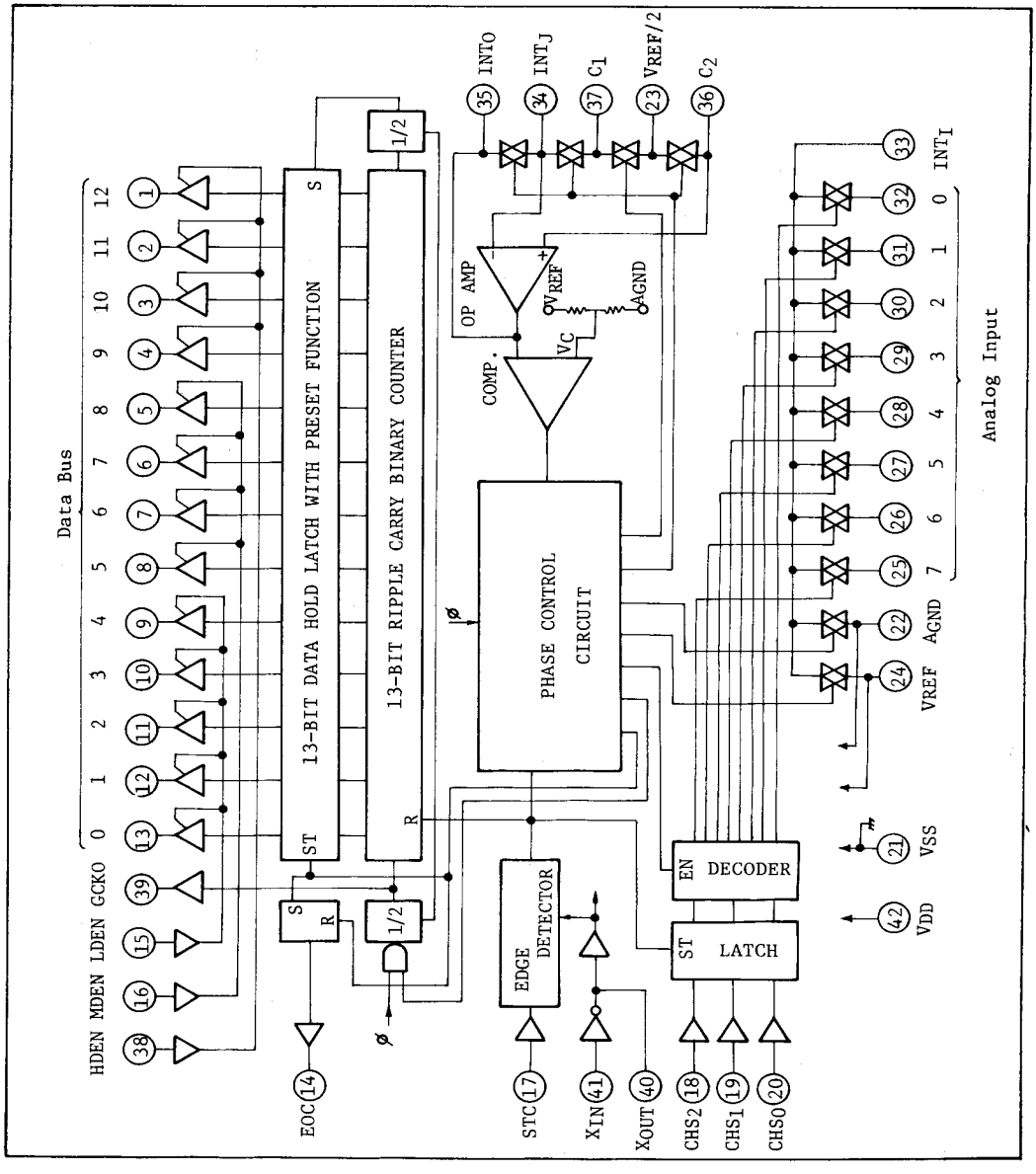
$$R_I \cdot C_I > \frac{13000}{f_{OSC}} \quad [S]$$

However, R of 1 ~ 2MΩ should be used.

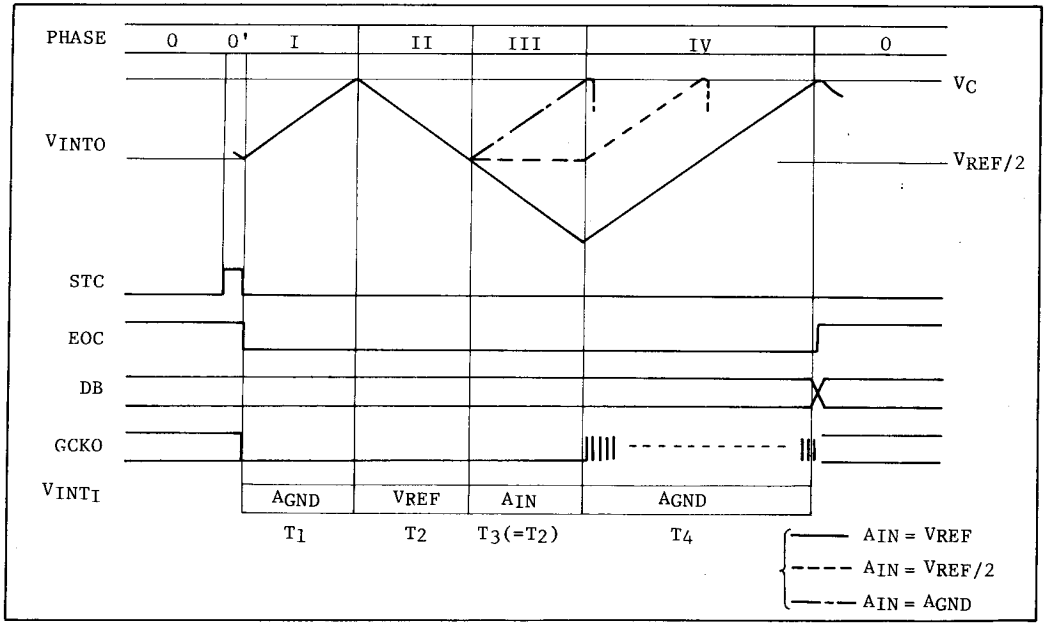
FUNCTION OF EACH PIN

PIN NO.	Symbol	NAME & FUNCTION
37	C_1	0.1μF is connected between C_2 and C_1, and 0.01μF C_1 and V_{SS}, respectively.
38	HDEN	High Data Enable $DB_9 \sim DB_{12}$ are read by "H" level input.
39	GCKO	Gated Clock Output Pulses of number equivalent to conversion data are output during conversion.
40	X_{OUT}	Terminals for system clock oscillation. Crystal oscillators are connected to both the ends of terminals.
41	X_{IN}	
42	V_{DD}	Supply Voltage 5V±0.5V

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Conversion cycle

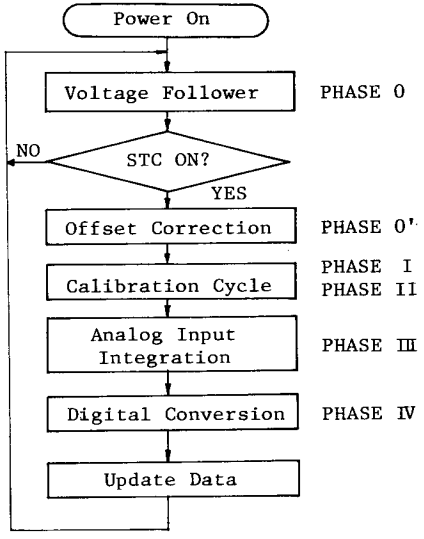
In the state of PHASE 0', the operation of L3I is at a stop and the integrating amplifier performs as voltage follower. Under this condition the external capactor (0.1μF across C_1 and C_2)

When STC is given, the offset voltage charged into external capacitors is applied to non-inversion of the integrator, thus cancelling the offset volage equivalently. In PHASE I, the integrator continues to integrate A_{GND} until its output reaches V_C.

In PHASE III the integrator integrates the analog input for the same period of time as T_2 after it has integrated V_{REF} for a fixed period of time (T_2) in PHASE II.

Finally, in PHASE IV the integrator continues to integrate A_{GND} until its output reaches V_C.

FUNCTIONAL DESCRIPTION



Let the time in PHASE IV be T_4. Then the following equation is made (formed) by omitting error factors such as offset drift.

$$V_{AIN} = \frac{T_4}{2T_2} V_{REF} \quad (AGND=0V) \quad \cdots \quad (1)$$

In case of this LSI, T_2 is designed by 4096 x $2 \cdot T_{OSC}$ (T_{OSC} denotes reference clock synchronization). Therefore, the above formula letting $2 \cdot T_{OSC}$ be T is changed as follows:

$$\frac{V_{AIN}}{V_{REF}} = \frac{T_4}{8192T} \quad \cdots\cdots\cdots\cdots\cdots \quad (2)$$

That is, 13-bit resolution A/D conversion of FS (full scale) = 8192 can be made by counting the period of T_4 by use of a clock having T frequency.

However, it is recommended that R_I and C_I composing the integrator be set to the values close to $13000/f_{OSC}$ as possible after having satisfied the following formula.

$$R_I C_I > 13000 / f_{OSC}, \quad R_I = 1 \sim 2M\Omega \text{ is used.} \quad \cdots\cdots\cdots \quad (3)$$

(2) Output data format

13-bit output data are output to 13 independent 3-state data buses $DB_0 \sim DB_{12}$. Since 13-bit outputs can be independently placed on 3-state every group of High, Medium and Low of 4 bits/4 bits/5 bits from the higher order, it is easy to connect the microcomputer to buses of 4, 8, 12 bits.

FUNCTIONAL DESCRIPTION

TRUTH TABLE

LDEN	MDEN	HDEN	Analog Input	DATA OUTPUTS (DB)												
				0	1	2	3	4	5	6	7	8	9	10	11	12
L	L	L	Don't Care	Z					Z				Z			
H	L	L		D	D	D	D	D								
L	H	L		Z					D	D	D	D				
H	H	L		D	D	D	D	D	D	D	D	D				
L	L	H		Z					Z				D	D	D	D
H	L	H		D	D	D	D	D					D	D	D	D
L	H	H		Z					D	D	D	D	D	D	D	D
H	H	H	<1/2LSB	L	L	L	L	L	L	L	L	L	L	L	L	L
			1/2LSB ∿ 3/2LSB	H	L	L	L	L	L	L	L	L	L	L	L	L
			.....	Straight Binary												
			"FS"-5/2LSB ∿ "FS"-3/2LSB	L	H	H	H	H	H	H	H	H	H	H	H	H
			"FS"-3/2 LSB <	H	H	H	H	H	H	H	H	H	H	H	H	H

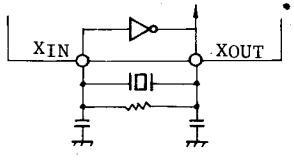
Note : FS ····· Full Scale, 1 LSB = (V_{REF}-AGND)/8192, Z ··· High Impedance

D ··· "H" or "L" Level

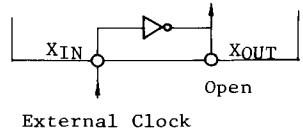
(3) Basic clock

Since this LSI operates on the basis of the frequency given to X_{IN} input, a stable clock ($\Delta f < 0.005\%$) must be used for the clock to be given to X_{IN}.

Therefore, it is proper that the oscillation circuit is configured as shown in the following figure (a) by the use of externally mounted crystal becuase the LSI has a built-in inverter for crystal oscillation.



(a)



External Clock

(b)

FUNCTIONAL DESCRIPTION

(4) How to give STC input, Conversion time, and Sampling cycle

STC input is taken in with the reference clock of LSI, but the positive pulse having the pulse width for at least two cycles is required for internal starting.

The conversion time of from the fall of STC input to the rise of EOC output. Letting this time be Tc MAX(Maximum conversion time), then the following equation is obtained.

$$TcMAX = 41000 \times T_{OSC} \text{ [S]} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (4)$$

(where T_{OSC} is oscillation cycle of basic clock.)

For example, when f_{CP}=5MHz, TcMAX=8.2ms. For one-time sampling, an accurate output can be obtained from the falling edge of STC input after the lapse of TcMAX.

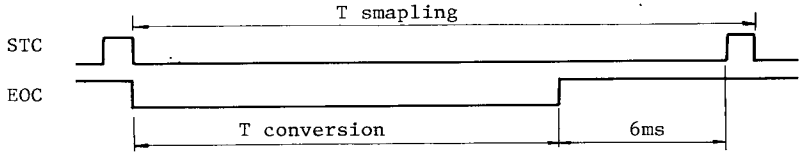
For consecutive sampling, however, STC input must be given after the lapse of a given period of time (6ms) from the rise of EOC. This period (6ms) is the time required for the recovery of LSI to normal state.

Therefore, the minimum sampling cycle TsMIN is as follows:

$$TsMIN = 41000 \times T_{OSC} + 0.006 + t_w(STC) \text{ [S]} \quad \cdots\cdots\cdots \quad (5)$$

Note: When power is set ON, following start-up procedure is required due to indefinite state of internal circuitry.

1. Applying clock, STC is to be set high over 10ms.
2. Complete at least one cycle as a dummy conversion cycle.

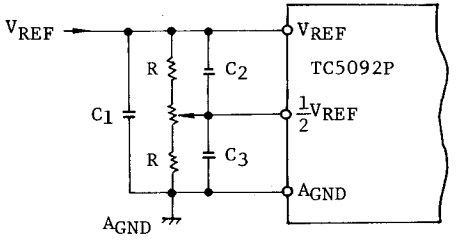


(5) Reference voltage

This LSI has three reference input voltage terminals of A_{GND}, $\frac{1}{2} V_{REF}$, and V_{REF}. Since analog input signal is quantized to 1/8192 in the range of $A_{GND} \sim A_{REF}$ for digitization, stable voltages must be supplied to $\frac{1}{2} V_{REF}$ and V_{REF}.

FUNCTIONAL DESCRIPTION

Espacially the value of $\frac{1}{2}$ V_{REF} voltage has direct effects upon conversion accuracy; therefore, it is recommonded that adjustment be made so as to agree output data with analog input by actually making A/D convert by use of input voltage at FS (full scale) or 1/2FS level.

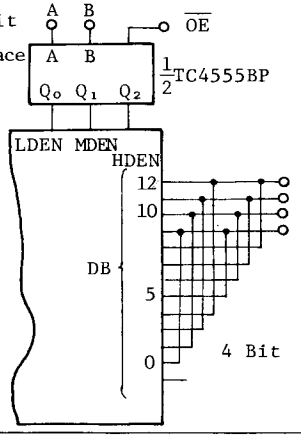


The left figure shows an example of reference voltage supplying circuit. $C_1 \sim C_3$ are filter capacitors for preventing reference voltage variations to be caused by ripple or induction noise. Generally the value of capacitor is about $0.01 \sim 0.1\mu F$, though it varies with the system.

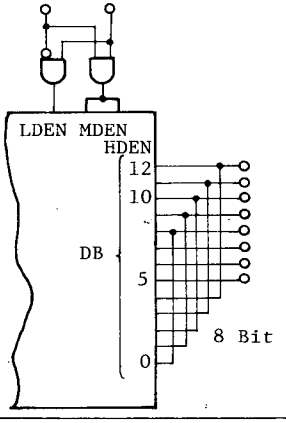
(6) BUS Interface

For connecting a microcomputer to BUS line, three independent enable terminals are used. These three enable terminals permit the processing in the unit of 4 bits (5 bits for the low order digit only). The microcomputer can be directly connected to the BUS of $4 \sim 12$ bits easily by allocating proper address of microcomputer to the TC5092AP.

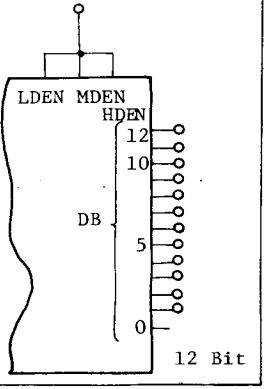
(a) 4 Bit Interface



(b) 8 Bit Interface



(c) 12 Bit Interface



RECOMMENDED OPERATING CONDITION

ITEM	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Digital Input Voltage	V_{IN}		0	-	V_{DD}	V
Analog Input Voltage	V_{AIN}		AGND	-	V_{REF}	-
Reference Supply Voltage	V_{REF}		4.0	-	V_{DD}	V
Analog Ground Voltage	V_{AGND}		0	0	0.5	V

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = -40 ~ 85°C)

ITEM	SYMBOL	TEST CONDITION		V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output High Voltage	V_{OH}	I_{OH}=-1μA, Digital output		5	4.9	5.0	-	V
Output Low Voltage	V_{OL}	I_{OL}=1μA, Digital output		5	-	0.0	0.1	
Input High Voltage	V_{IH}	Digital Input except X_{IN}		5	2.4	-	-	V
		X_{IN}		5	4.5	-	-	
Input Low Voltage	V_{IL}	Digital Input except X_{IN}		5	-	-	0.8	
		X_{IN}		5	-	-	0.5	
Output High Current	I_{OH}	V_{OH} = 2.4V Digital output except X_{OUT}		4.75	-1.0	-	-	mA
Output Low Current	I_{OL}	V_{OL} = 0.4V Digital output except X_{OUT}		4.75	1.6	-	-	mA
Output Disable Current	I_{DH}	V_{OH} = 5.5V, $DB_0 \sim DB_{12}$		5.5	-	10^{-3}	5	μA
	I_{DL}	V_{OL} = 0.0V, $DB_0 \sim DB_{12}$		5.5	-	-10^{-3}	-5	
Input Current	I_{IH}	V_{IN}=5.5V, Digital input		5.5	-	10^{-5}	1.0	
	I_{IL}	V_{IL}=0.0V, Digital input		5.5	-	-10^{-5}	-1.0	
Analog Switch Off-Leak	I_{OFF}	Analog input/output		5.5	-	±10^{-4}	-	μA
Analog Switch On Resistor	R_{ON}	R_L = 10kΩ		5	-		-	Ω
Operating Consumption Current	I_{DD}	V_{REF} = V_{DD} Digital output open Digital input GND	f_{CP}=5MHz	5	-	2	-	mA
			f_{CP}=1MHz	5	-	1	-	

SWITCHING CHARACTERISTICS (V_{DD} = 5V±10%, V_{SS} = 0V, Ta = 25°C, C_L = 50pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}	Digital output	-	50	150	ns
Output Fall Time	t_{THL}	Digital output	-	40	150	
Output Enable Time	t_{ZL} t_{ZH}	LDEN, MDEN, HDEN -DB Output	-	80	250	ns
Output Disable Time	t_{LZ} t_{HZ}		-	280	500	
Max. Clock Frequency	$f_{MAX\phi}$	X_{IN} Duty 40~60%	5.0	-	-	MHz
Min. Clock Frequency	$f_{MIN\phi}$	X_{IN} Duty 40~60%	-	-	-	
Input Capacity	C_{IN}	Digital input	-	5	-	pF
	C_{IN}	Analog input	-	-	-	
3-State Output Capacity	C_{OUT}	DB Output	-	8	-	

SYSTEM CHARACTERISTICS (V_{DD} = 5V±10%, V_{SS} = 0V, Ta = 25°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution	n		-	13	-	Bit
Conversion Time	Tc	f_{CP} = 5 MHz	-	-	8.2	ms
		f_{CP} = 1 MHz	-	-	41	
Sampling Cycle	T_{SPL}	f_{CP} = 5 MHz	14.2	-	-	ms
		f_{CP} = 1 MHz	47	-	-	
Nonlinearity		V_{DD} = V_{REF}	-	±1		LSB
Zero Scale Error	E_{ZP}		-	±2		
Full Scale Error	E_{FS}		-	±1		
STC Min. Pulse Width	t_w		-	-	2/f_{OSC}	S