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MA808

FRAME ALIGNER WITH OPTIONAL TIME SLOT ZERO RECEIVER

The MA808 Frame Aligner chip has been primarily designed for use in equipment operating at the CCITT standard of 2048 kbit/s tor 30 channel PCM data signals.

The basic function of the device is to accept a 2048 kbit/s data signal, whose frame structure conforms to CCITT recommendation G732 and frame synchronously align it to a local exchange/system clock.

The frame aligner operation is such that once a synchronisation sequence, as defined in CCITT recommendation G732, is received from a distant source synchronisation is established. Consequently the data stream is delayed such as to align it to the timing required at the local source. Once three successive sync. words are received containing errors, synchronisation is lost. The chip will remain out of sync. until the synchronising sequence is received.

The device can also, when configured in the 'enhanced mode' perform the additional function of time slot zero recovery.

A number of facilities are also provided to simplify the testing of the device and associated system.

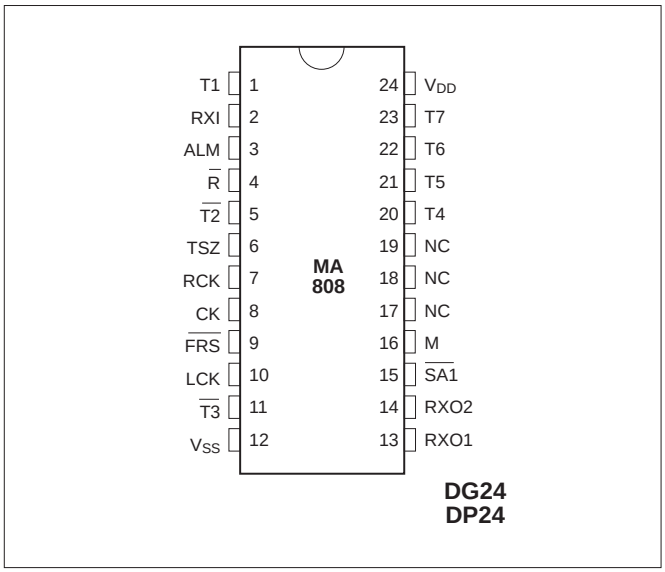

Figure 1: Basic Mode pin connections - top view. M tied to V_{SS}

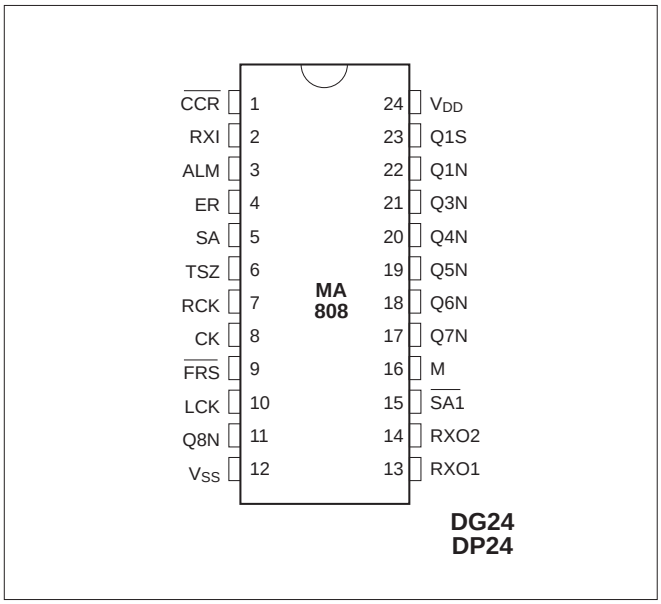

Figure 2: Enhanced Mode pin connections - top view. M tied to V_{DD}

FEATURES

- Fabricated in Low Power CMOS
- Optional Time Slot Zero Receiver
- Detection of Frame Alignment Signals for 30 Channel PCM Highways Operating at 2048 kbit/s in Accordance with CCITT Recommendations G732
- Delay Compensation and Clock Alignment between the Transmission Line system and the Exchange
- Compensation of Phase Jitter, Meeting the Requirements of CCITT
- Detection and Indication of Loss of Frame Alignment
- Provision of a Signal for Generation of AIS
- Slip Compensation
- Chip Functional Test Facilities
- TTL Compatible
- Operating Power Consumption 75mW max.
- Single + 5V Supply
- High Latch-up Immunity
- 256 kHz Clock Output

APPLICATIONS

- Digital Multiplex Equipment
- Interfaces between PCM Line and Switching Systems
- Concentrators

OPERATION IN BASIC MODE (M =V_{SS})

FRAME ALIGNMENT

The remote non-return-to-zero (NRZ) binary PCM data stream (RXI) required to be aligned must be applied to the frame aligner along with a synchronous clock (RCK). A time slot zero impulse (TSZ) as shown in Fig. 5 is also required to define the start ot the frame of input data.

A local clock (LCK) provides the timing from which the output data is clocked. Frame reset pulse ($\overline{FRS}$) is the data output timing pulse. The MA808 aligns the 16th bit of the incoming data to this pulse, as shown in Fig. 5, and the two NRZ binary outputs RXO1 and RXO2 are produced. RXO1 is purely a retimed version of the input data. RXO2 has the third bit of all time slot zero locations of the input data inverted, thereby deliberately corrupting the frame sync. and the frame sync. verification words. Once synchronisation has been established $\overline{FRS}$ may be removed. If synchronisation is lost, $\overline{FRS}$ must be reapplied in order to permit resynchronisation to be established.

SLIP COMPENSATION

Small differences in frequency between the local and remote clocks (LCK and RCK) are compensated for by the repetition of the previous frame, ('slipping in') or the omission of one complete frame of data ('slipping out').

INPUT ALARMS

Two input alarms ($\overline{SA1}$ and ALM) are provided which will set data output(s) to an 'all ones' condition. ALM sets only RXO2 and $\overline{SA1}$ sets both RXO1 and RXO2 high (Fig. 6).

TEST FEATURES

The operation of the internal memory of the MA808 is continuously monitored by performing a check sum comparison of the input and output data signals RXI and RXO1. When an error is detected, the time slot zero words of RXO1 and RXO2 are set 'high'.

When a 'low' is applied to test input T3, the outputs RXO1, RXO2 and CK are forced into a high impedance condition, thereby allowing associated circuitry to be tested independently of the MA808. Note that this facility is only available in the basic mode of operation.

OPERATION IN ENHANCED MODE (M=V_{DD})

When configured in the enhanced mode the chip performs time slot zero (TS0) recovery in addition to the frame alignment function. TS0 recovery may also be performed independently.

FRAME ALIGNMENT

The operation of frame alignment is essentially the same as the basic mode, except that the TSZ pulse is an output rather than an input, in accordance with the operation of the TS0 receiver, as shown in Fig. 7. The operation of the input alarms to set the output data 'high' is the same as described in the basic mode (Fig. 6).

TIME SLOT ZERO RECEIVER

Two output signals (TSZ and $\overline{CCR}$) are provided so that the time slot zero receiver may be used independently of the frame alignment function. $\overline{CCR}$ is a channel reset pulse (as shown in Fig. 7) which goes 'low' for one RCK period following a sync. word (every alternate frame) when the device is in sync. When the device is out of sync. the reset pulse occurs after each time slot zero.

The TS0 receiver accesses information contained within time slot zeros and processes it to offer the facilities of synchronisation alarm (SA), error output (ER) and time slot zero spare bits (Q1S, Q1N, Q3N-Q8N).

SYNCHRONISATION ALARM (SA)

SA indicates loss of sync. as shown in Fig. 8. With the frame aligner operating in sync., SA will be 'low'. Following the receipt of 3 successive sync. words containing errors, SA will become active. SA will remain 'high' until the correct synchronising sequence as defined in CCITT recommendations G732 has been received.

ERROR OUTPUT (ER)

A logic signal, ER, indicating errors in sync. words, is provided as shown in Fig. 8, from which an AIS alarm may be generated. ER is activated at the beginning of the second bit of time slot 1 two frames after the receipt of a sync. word containing errors. If successive sync. words contain errors, the signal will remain active.

If synchronisation is lost, ER will remain active but will go 'low' for one period of the remote clock during the second bit of time slot 1, two frames after the receipt of the last valid sync. word, as long as synchronisation is not regained at this time.

If synchronisation is regained, ER will go 'low' for the two frames following the sync. word which caused synchronisation to be regained. The signal indicating an error in the sync. word two frames prior to synchronisation being regained will be delayed by one further sync. frame period. Consequently, it may be concluded that all errors in sync. words are accounted for in this signal, hence error monitoring in accordance with CCITT recommendation G732.3.1.6.1 may be performed.

TIME SLOT ZERO SPARE BITS

The spare bits contained in both time slot zero words are converted from serial to parallel format (Q1N, Q3N-Q8N inc. and Q1 S) are shown in Fig. 9.

PIN DESCRIPTIONS - BASIC MODE

Pin	Def.	Function	Description
1	T1	Test input	Active high. To be tied to logic low during normal operation.
2	RXI	Data input	Recovered distant data input.
3	ALM	Alarm input	A logic high on this input sets RXO2 to an all 1 s condition.
4	R	Reset input	'Low' resets the device tied 'high' normally.
5	$\overline{T2}$	Test input	Active low. To be tied to logic high during normal operation.
6	TSZ	TSO input	Remote TS0 timing signal.
7	RCK	Clock input	Recovered distant clock in sync. with RXI.
8	CK	256kHz output	256kHz square wave clock output synchronous with LCK.
9	$\overline{FRS}$	Timing input	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock input	Local clock input.
11	$\overline{T3}$	Test input	Active low. To be tied to logic high during normal operation.
12	V_{SS}	Negative supply	Nominally 0V.
13	RXO1	Data output	Retimed data output to LCK.
14	RXO2	Data output	As RXO1 except that bit 3 of each TS0 word is inverted.
15	$\overline{SA1}$	Set to all 1s input	A logic low sets RXO1 and RXO2 to an all 1s condition.
16	M	Mode input	Connected to Vss for basic mode operation.
17	NC	No connection	To be left O/C during normal operation.
18	NC	No connection	To be left O/C during normal operation.
19	NC	No connection	To be left O/C during normal operation.
20	T4	Test input	Active when clocked by LCK (pin 10). To be tied to logic low during normal operation.
21	T5	Test input	Active when clocked by RCK (pin 7). To be tied to logic low during normal operation.
22	T6	Test output	To be left O/C during normal operation.
23	T7	Test output	To be left O/C during normal operation.
24	V_{DD}	Positive supply	Nominally + 5V.

PIN DESCRIPTIONS - ENHANCED MODE

Pin	Def.	Function	Descrlption
1	$\overline{CCR}$	Channel reset	An output used to reset other devices within the system.
2	RXI	Data input	Recovered distant data input.
3	ALM	Alarm input	A logic high on this input sets RXO2 to an all 1 s condition.
4	ER	Error output	A TS0 word error is signalled when ER goes to logic high.
5	SA	Sync. alarm O/P	Loss of sync. is signalled when SA goes to logic high.
6	TSZ	TSO output	Remote TS0 output signal, (internally connected to the on-chip frame aligner).
7	RCK	Clock input	Recovered distant clock in sync. with RXI.
8	CK	256kHz output	256kHz square wave clock output synchronous with LCK.
9	$\overline{FRS}$	Timing input	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock input	Local clock input.
11	Q8N	Output signal	Signal corresponding to bit 8 of the TS0 sync. verification word.
12	V_{SS}	Negative supply	Nominally 0V
13	RXO1	Data output	Retimed data output to LCK
14	RXO2	Data output	As RXO1 except that bit 3 of each TS0 word is inverted.
15	$\overline{SA1}$	Set to all 1s input	A logic low sets RXO1 and RXO2 to an all 1s condition.
16	M	Mode input	Connected to V_{DD} for enhanced mode operation.
17	Q7N	Output signal	Signal corresponding to bit 7 of the TS0 sync. verification word.
18	Q6N	Output signal	Signal corresponding to bit 6 of the TS0 sync. verification word.
19	Q5N	Output signal	Signal corresponding to bit 5 of the TS0 sync. verification word.
20	Q4N	Output signal	Signal corresponding to bit 4 of the TS0 sync. verification word.
21	Q3N	Output signal	Signal corresponding to bit 3 of the TS0 sync. verification word.
22	Q1 N	Output signal	Signal corresponding to bit 1 of the TS0 sync. verification word
23	Q1 S	Output signal	Signal corresponding to bit 1 of the TS0 sync. word.
24	V_{DD}	Positive supply	Nominally +5V.

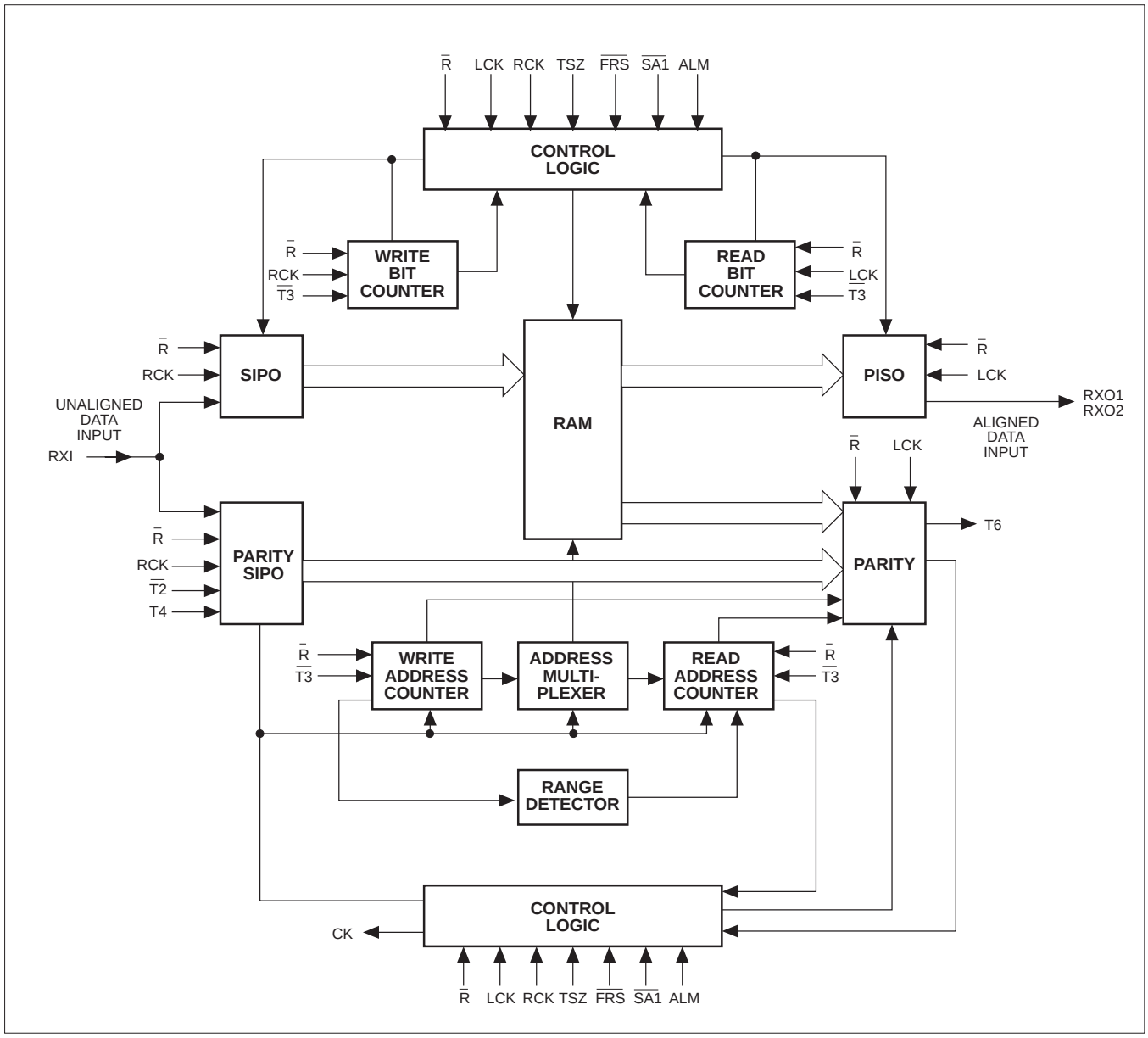

Figure 3: Frame aligner block diagram

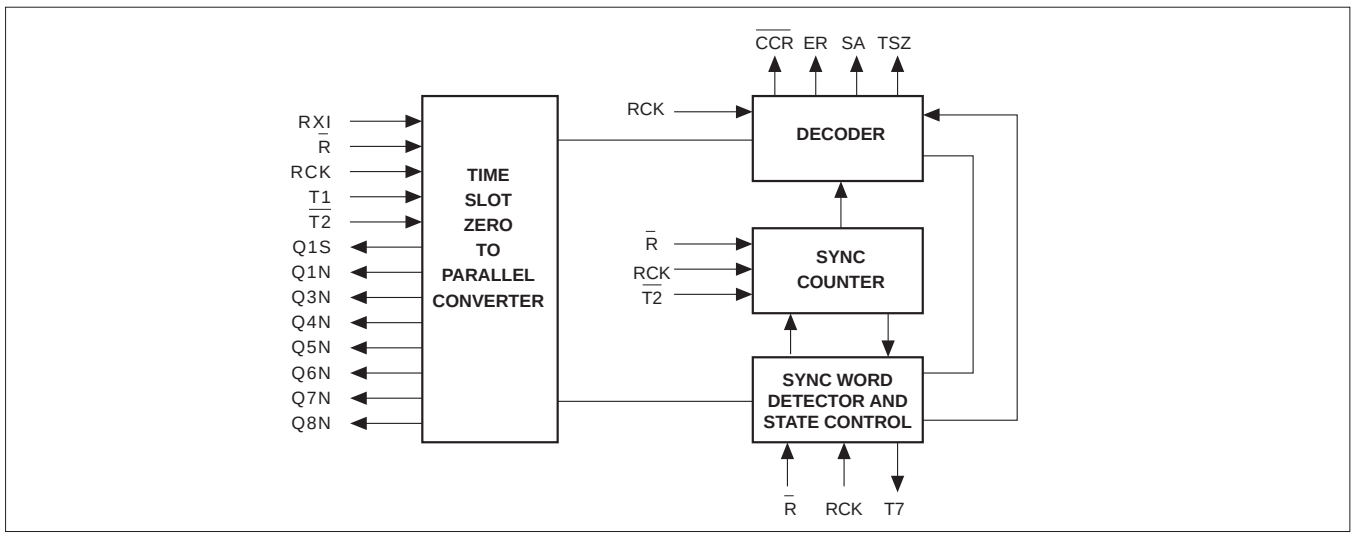

Figure 4: TSO receiver block diagram

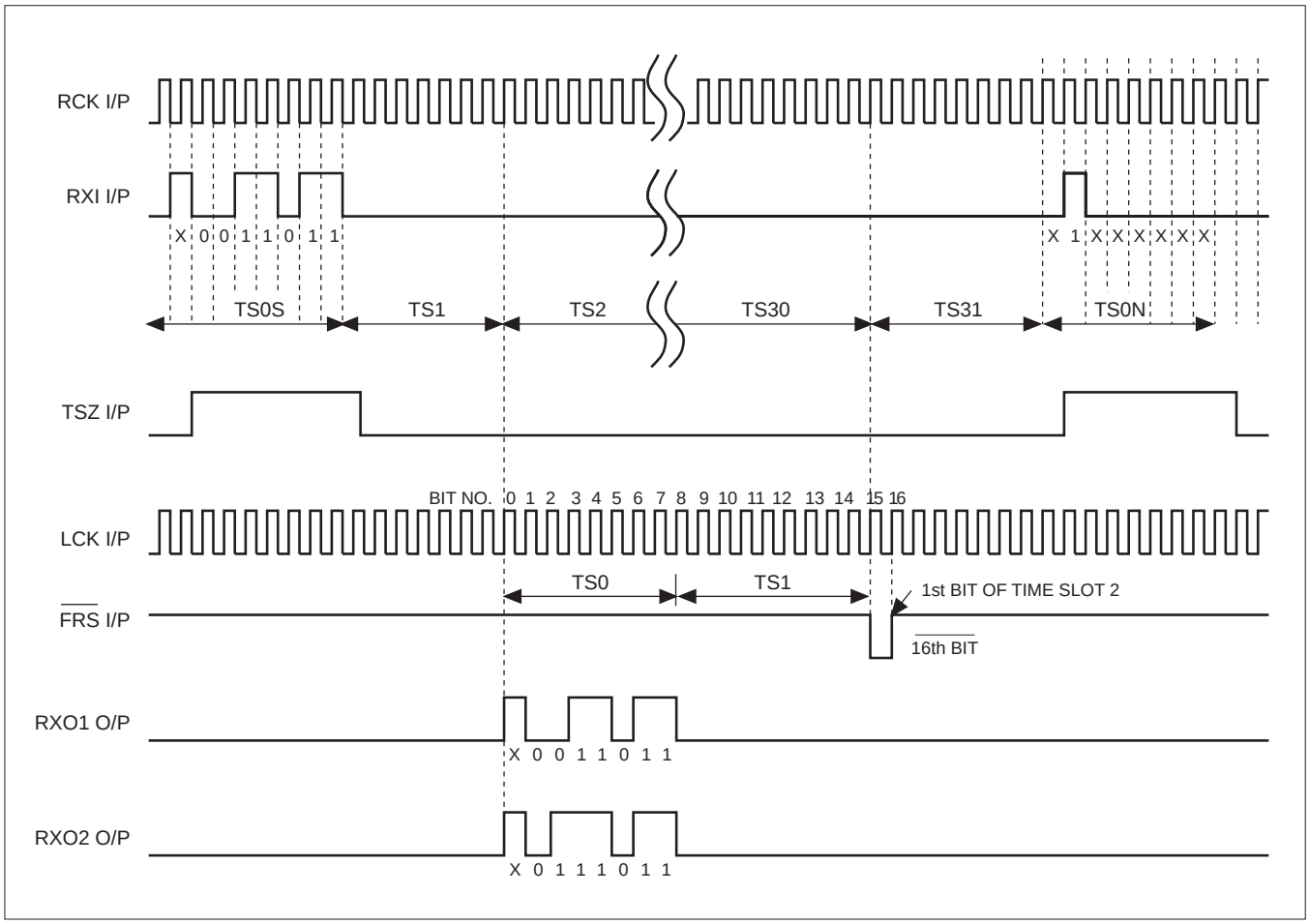

Figure 5: Timing diagram - basic mode: general operation of frame alignment

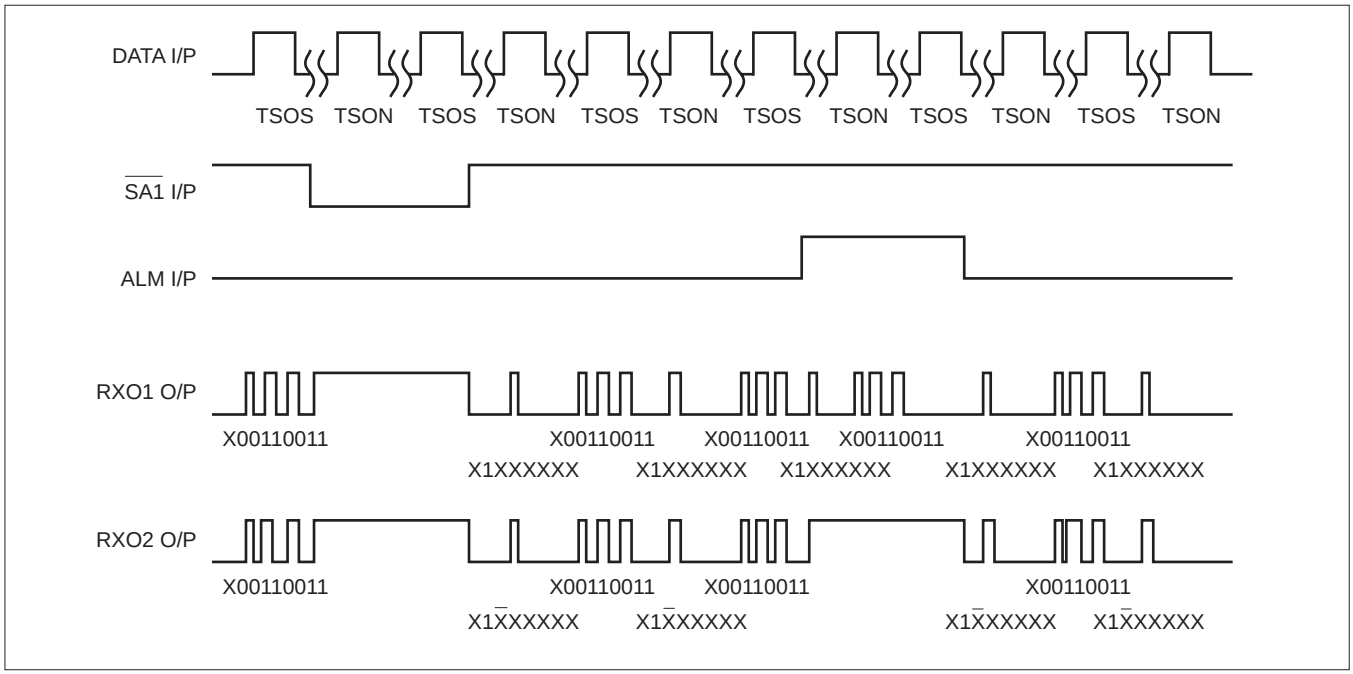

Figure 6: Timing diagram: protocol timings of the alarm signals

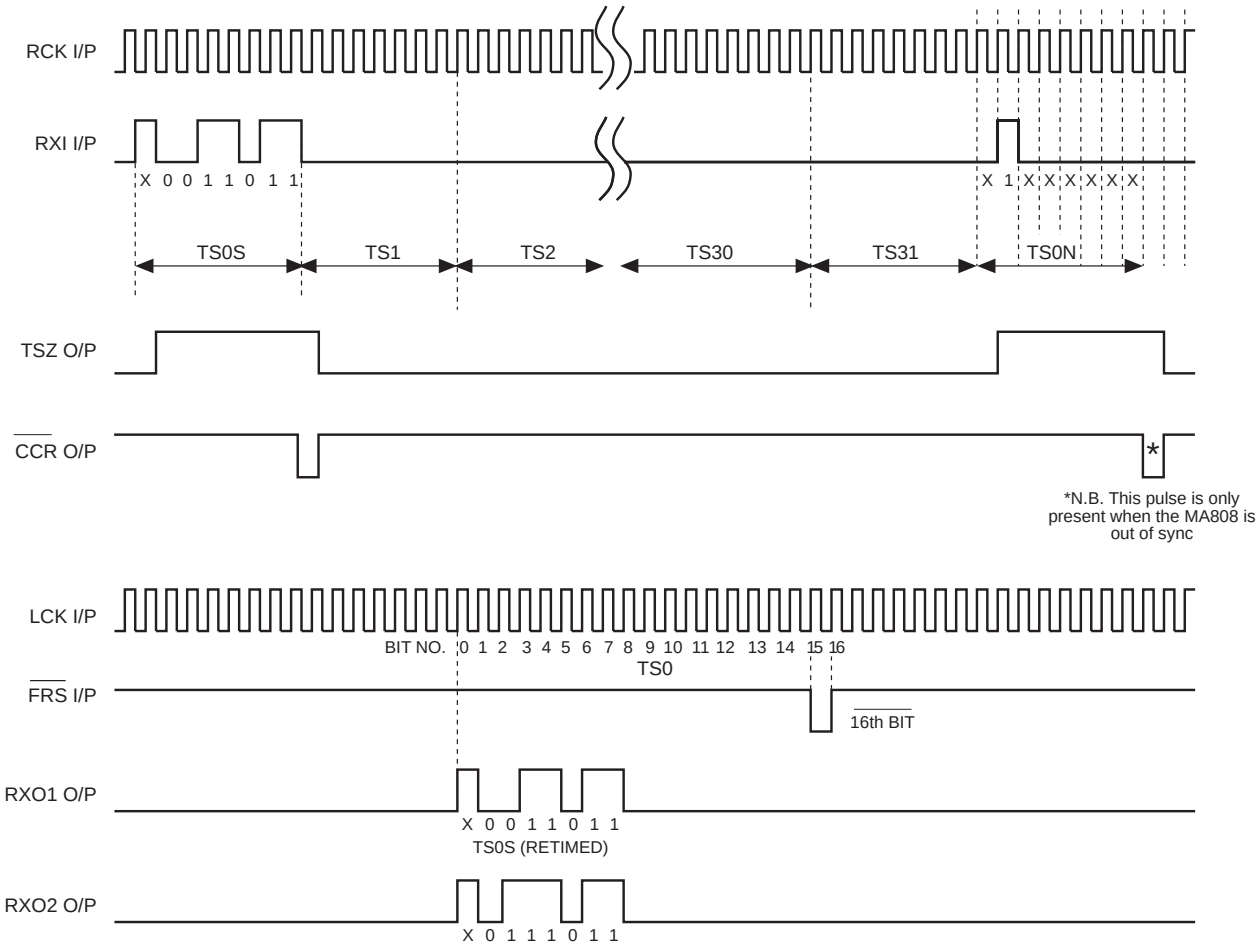

Figure 7: Timing diagram - enhanced mode: general operation of frame aligner

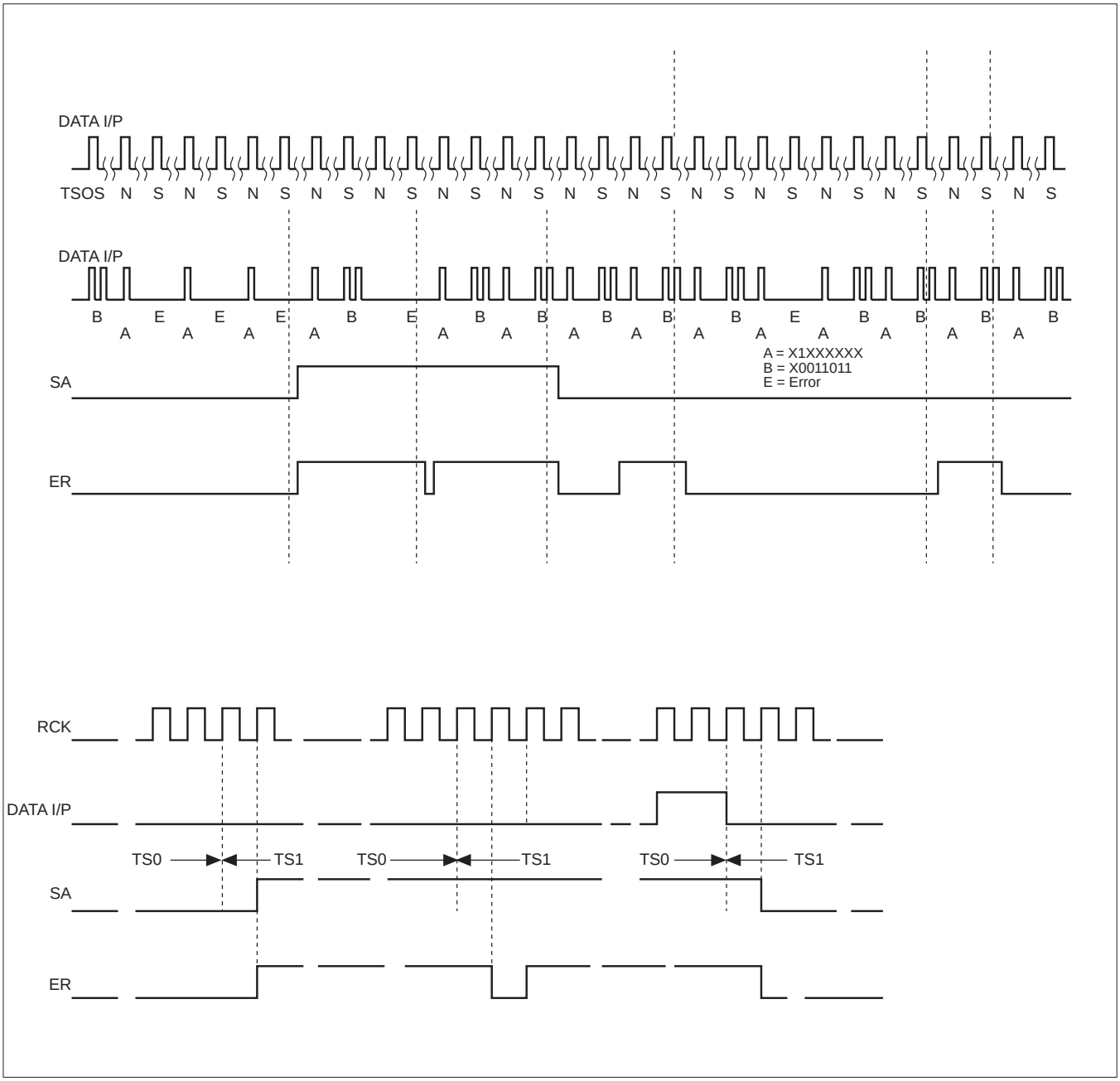

Figure 8: Timing diagram - enhanced mode: protocol timings of TSO receiver alarms

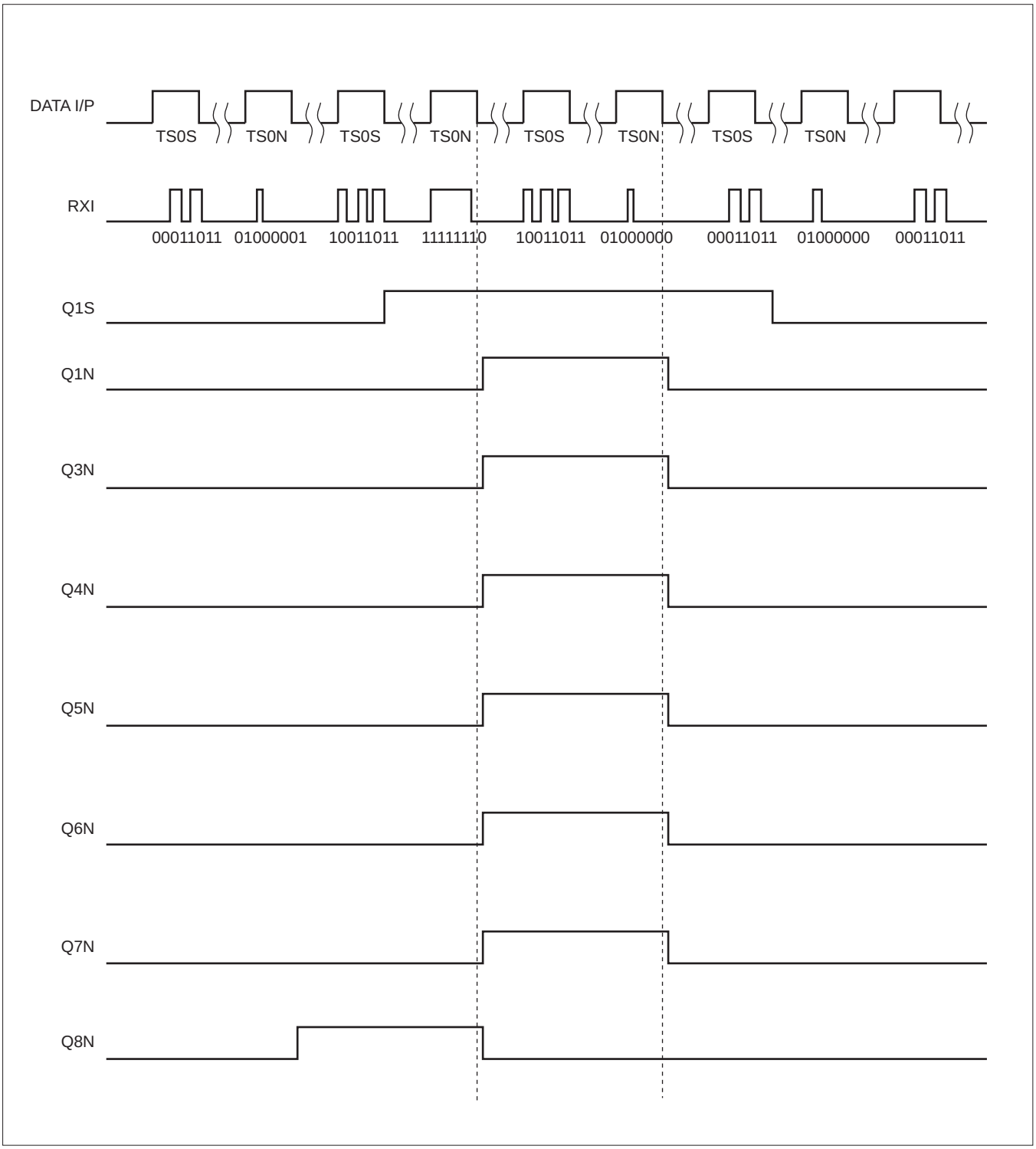

Figure 9: Timing diagram - enhanced mode: protocol timings of the signal lines

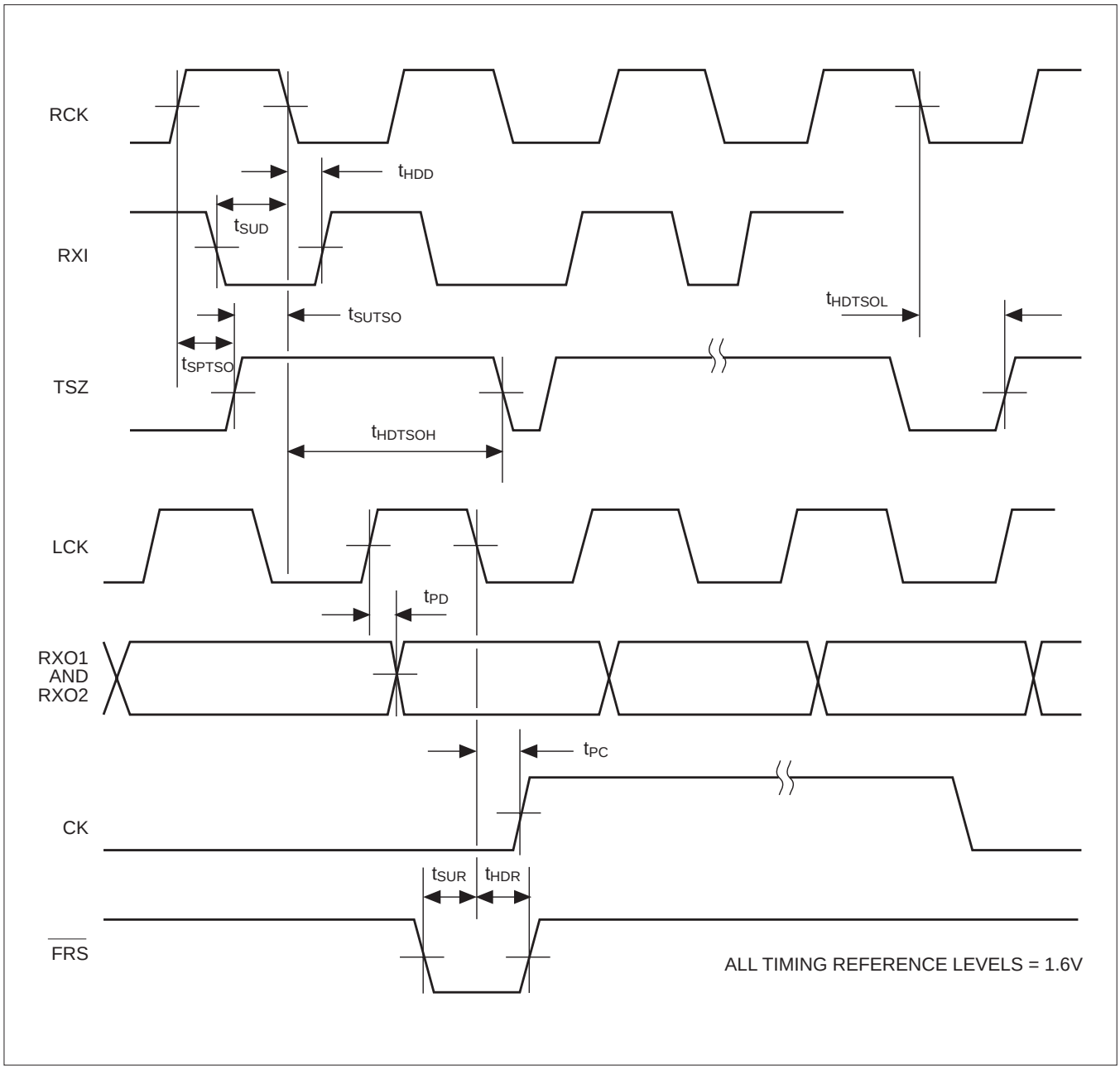

Figure 10: Timing diagram - basic and enhanced mode timing waveforms

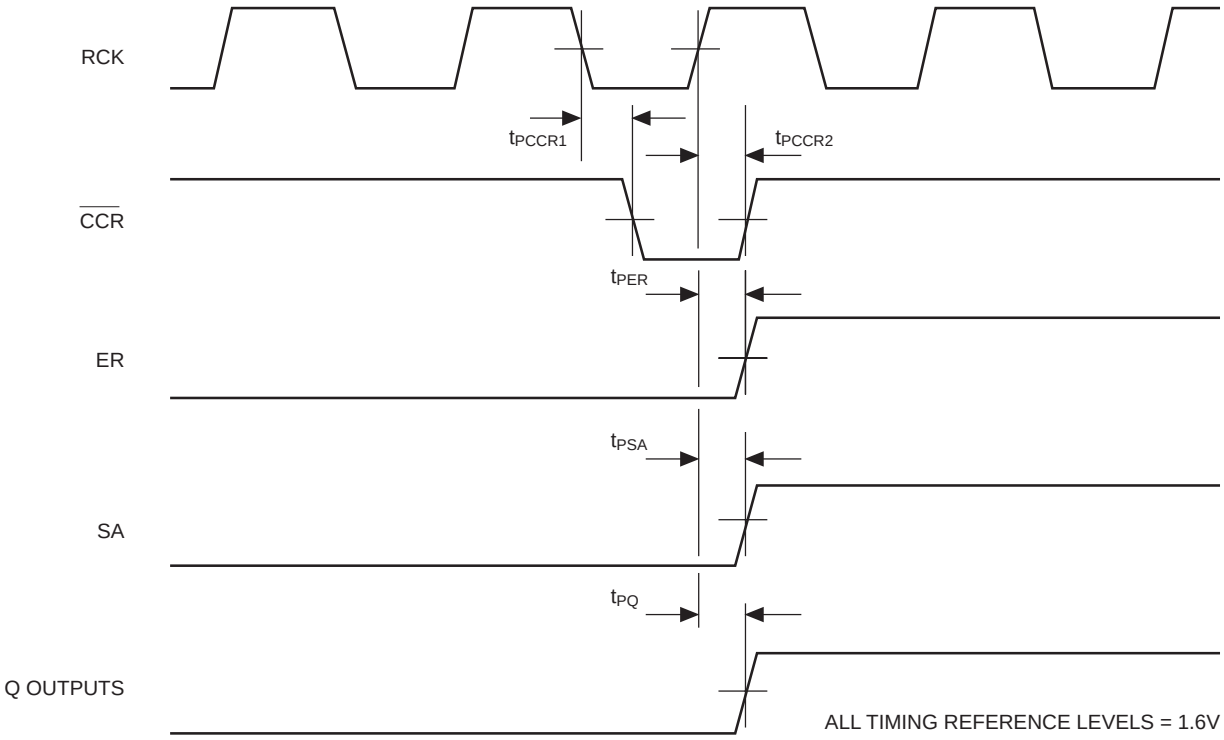

Figure 11: Timing diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

T_{AMB} = + 25 ° C

DC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}			0.8	V	V_{DD} = 4.75V
High level input voltage	V_{IH}	2.4			V	V_{DD} = 5.25V
Low level input current	I_{IL}			10	µA	$V_{IN} = V_{SS}$. V_{DD} = 5.25V
High level input current	I_{IH}			10	µA	$V_{IN} = V_{DD}$ = 5.25V
Low level output voltage	V_{OL}			0.5	V	I_{OL} = 2mA, V_{DD} = 4.75V
High level output voltage	V_{OH}	2.8				I_{OH} = 0 2mA V_{DD} = 4.75V
Output leakage current	I_{OL}			±10	µA	$V_{SS} < V_{OUT} < V_{DD}$, V_{DD} = 5.25V
Dynamic supply current	I_{DDD}			15	mA	
Static supply current	I_{DDS}			1	mA	

AC TIMING CHARACTERISTICS (REFER TO FIGS. 10 AND 11)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Set up time RXI to RCK (H→L)	t_{SUD}	25			ns	
Set up time TSZ to RCK (H→L)	t_{SUTSO}	20			ns	
Set up time $\overline{FRS}$ to LCK (H→L)	t_{SUR}	150			ns	
Data hold time wrt RCK (H→L)	t_{HDD}	100			ns	
TSZ (L) hold time wrt RCK (H→L)	t_{HDTSOL}	50			ns	
TSZ(H) hold time wrt RCK (H→L)	t_{HDTSOH}	100			ns	
$\overline{FRS}$ hold time wrt LCK (H→L)	t_{HDR}	150			ns	
Nominal frequency	f		2.048		MHz	
Propagation delay, LCK to RXO1 and RXO2	t_{PD}	30		150	ns	
Propagation delay, LCK (H→L) to CK	t_{PC}	0		175	ns	
Propagation delay, RCK (H→L) to $\overline{CCR}$ (H→L)	t_{PCCR1}	0		150	ns	Outputs loaded
Propagation delay, RCK (L→H) to $\overline{CCR}$ (L→H)	t_{PCCR2}	0		200	ns	to10pF,
Propagation delay, RCK (L→H) to TSZ	t_{PTSO}	20		200	ns	f_{CLOCK}=2.048MHz
Propagation delay, RCK (L→H) to ER	t_{PER}	20		200	ns	
Propagation delay, RCK (L→H) to SA	t_{PSA}	20		200	ns	
Propagation delay, RCK (L→H) to Q8N-Q3N, Q1N and Q1S	t_{PQ}	20		200	ns	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 7.0V
Voltage on any pin (V_{IN}) (See note 1)	V_{SS} - 0.3V to V_{DD} + 0.3V
Current through any pin (See note 1)	± 20mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to+55°C

NOTES

1. Guaranteed no latch-up conditions.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

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