Ordering number: EN※4605

CMOS LSI

No.※4605

LC8213

Image Data Compression/Expansion Processor

Overview

The LC8213 is a IC that compresses (codes) and expands (decodes) binary image data used for facsimiles, etc. This LC8213 can be used in office automation equipment such as G3/G4 facsimiles, image file systems, digital photocopiers, and workstations.

The coding method is based on the MH (Modified Huffman), MR (Modified Relative Element Address Designate), and MMR (Modified MR) coding methods regulated by CCITT T.4 and T.6.

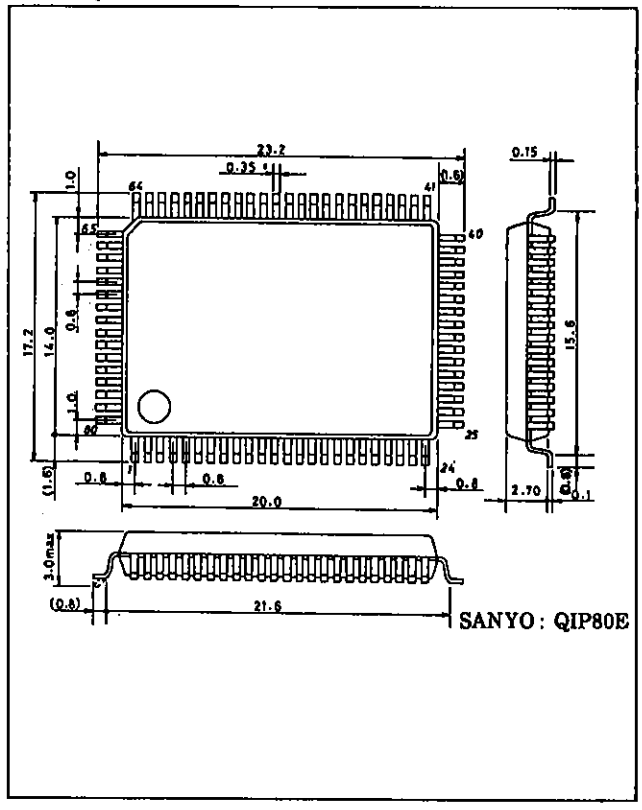
Features

- CCITT T.4 and T.6 MH, MR, MMR coding methods
- Compatible with G3 and G4 facsimiles
- No. of main scanning direction pixels Max. 64k bits
- Line skip mode
- 8/16 bit image memory bus, 8-bit CPU bus
- Transfer of data between CPU bus and image memory bus
- DMA transfer function between image memory and I/O device
- System clock Max. 20MHz
- CMOS low power consumption

Package Dimensions

(unit : mm)

3174-QIP80E



Specifications

Absolute maximum ratings at Ta = 25°C, V_{SS} = 0V

Parameter		Symbol	Condition	Rating	Unit
Maximum supply voltage		V_{DD} max		−0.3 to +7.0	V
Input/output voltage		V_I, V_O		−0.3 to V_{DD} +0.3	V
Maximum		Pd max	Ta ≤ 70°C	350	mW
Operation ambient temperature		Topr		−30 to +70	°C
Storage ambient temperature		Tstg		−55 to +125	°C
Resistance against solder heat	Manual solder		3 seconds	350	°C
	Reflow		10 seconds	235	°C

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Allowable Operating ranges at Ta = −30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage range	V_{IN}	0		V_{DD}	V

DC Characteristics at Ta = −30 to +70°C, V_{SS} = 0V, V_{DD} = 4.5 to 5.5V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input high level voltage	V_{IH}	TTL compatible	2.2			V
Input low level voltage	V_{IL}	TTL compatible			0.8	V
Input leak current	I_L	$V_{IN} = V_{SS}, V_{DD}$	−25		+25	μA
Output high level voltage	V_{OH}	I_{OH} = −3mA	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output leak current	I_{OZ}	During high impedance output	−100		+100	μA
Oscillation frequency	f_{osc}	CLK			20	MHz
Current consumption	I_{DD}			15	30	mA

AC Characteristics

Clock Reset Timing

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock cycle time	tCLK	50			ns
Clock low level width	tCKL	15			ns
Clock high level width	tCKH	15			ns
Reset pulse width	tRSTW	6 tCLK			ns

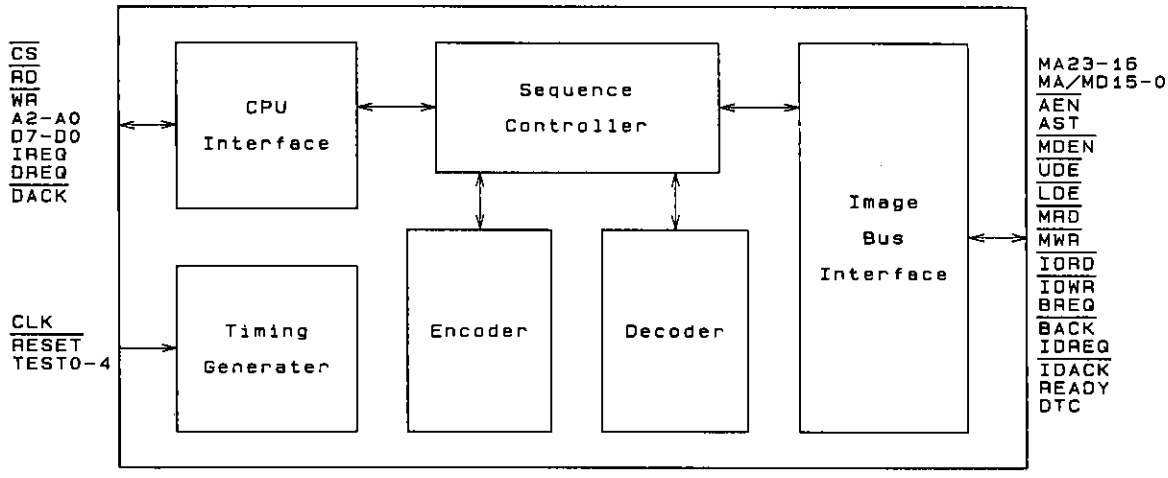
CPU Interface

Parameter	Symbol	Rating			Unit
		min	typ	max	
Address setup time	tAS	20			ns
Address hold time	tAH	10			ns
Read pulse width	tRW	100			ns
Read data delay time	tRD			100	ns
Read data hold time	tRH	10			ns
Write pulse width	tWW	100			ns
Write data setup time	tDS	20			ns
Write data hold time	tWH	10			ns
DACK setup time	tDAS	20			ns
DACK hold time	tDAH	10			ns
DREQ delay time	tDRQ			2 tCLK + 70	ns

Image Memory Interface

Parameter	Symbol	Rating			Unit
		min	typ	max	
AEN ↓ delay time	tAEL			70	ns
AEN ↑ delay time	tAEH			70	ns
AST ↑ delay time	tASH			70	ns
AST ↓ delay time	tASL			70	ns
Control signal valid delay time	tRWV			70	ns
Control signal invalid delay time	tRWH			70	ns
MRD, IORD ↓ delay time	tRDL			70	ns
MRD, IORD ↑ delay time	tRDH			70	ns
MWR, IOWR ↓ delay time	tWRL			70	ns
MWR, IOWR ↑ delay time	tWRH			70	ns
UDE, LDE ↓ delay time	tDEL			70	ns
UDE, LDE ↑ delay time	tDEH			70	ns
MDEN ↓ delay time	tMDL			70	ns
MDEN ↑ delay time	tMDH			70	ns
Address valid delay time	tMAV			100	ns
Address hold time	tMAH	25			ns
Read data setup time	tDSR	10			ns
Read data hold time	tDHR	0			ns
Write data delay time	tDDW			80	ns
Write data hold time	tDHW	10			ns
BREQ ↑ delay time (for IDREQ ↑)	tBRH	2 tCLK + 20		4 tCLK + 70	ns
BREQ ↓ delay time	tBRL			70	ns
IDACK ↓ delay time (for BACK ↓)	tDACD	3 tCLK + 20		13 tCLK + 70	ns
IDACK ↓ delay time (for CLK ↑)	tDACL			70	ns
IDACK ↑ delay time	tDACH			70	ns
DTC ↑ delay time	tDTCH			70	ns
DTC ↓ delay time	tDTCL			70	ns
READY setup time	tRDYS	30			ns
READY hold time	tRDYH	30			ns

Block Diagram



Block Diagram

· CPU interface

This is an interface circuit with the general purpose 8-bit CPU. The operation mode can be set, etc., by accessing the interface register and parameter register.

· Sequence controller

Each block is controlled by the coded and decoded process algorithm.

· Coding section

The change points of the pixels are detected and judged, and a code in each mode is generated. The coded data is transferred to the data bus via the FIFO (EFIFO) for 8-bit×4-word coding.

· Decoding section

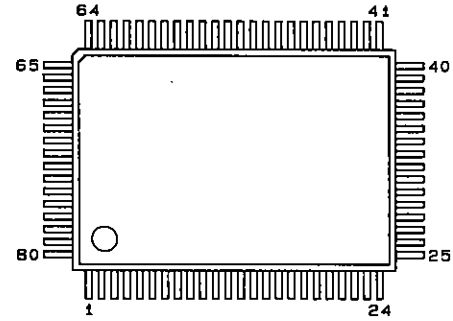
The coded data in each mode is judged and the reproduced pixel data is generated. The coded data is transferred to the data bus via the FIFO (DFIFO) for decoding.

· Image memory interface

Reading and writing of the image memory and control of the DMA transfer on the image memory bus is performed.

Pin Assignment

I : Input pin
O : Output pin
B : Bidirectional pin
P : Power pin
NC : Not connected



No.	Pin name	Type
1	$\overline{CS}$	I
2	$\overline{RD}$	I
3	WR	I
4	A2	I
5	A1	I
6	A0	I
7	V_{DD}	P
8		NC
9	D7	B
10	D6	B
11	D5	B
12	D4	B
13	V_{SS}	P
14	D3	B
15	D2	B
16	D1	B
17	D0	B
18		NC
19	V_{DD}	P
20	IREQ	O
21	DREQ	O
22	$\overline{DACK}$	I
23		NC
24		NC
25		NC
26		NC
27	$\overline{RESET}$	I
28	CLK	I
29	V_{SS}	P
30	TEST4	I

No.	Pin name	Type
31	V_{DD}	P
32	TEST3	I
33	TEST2	I
34	TEST1	I
35	TEST0	I
36		NC
37	BREQ	O
38	$\overline{BACK}$	I
39	IDREQ	I
40	$\overline{IDACK}$	O
41	$\overline{AEN}$	O
42	AST	O
43	$\overline{MDEN}$	O
44	$\overline{MRD}$	O
45	$\overline{MWR}$	O
46	$\overline{IORD}$	O
47	$\overline{IOWR}$	O
48	$\overline{LDE}$	O
49	$\overline{UDE}$	O
50	READY	I
51	DTC	O
52	V_{SS}	P
53	V_{DD}	P
54	MA23	O
55	MA22	O
56	MA21	O
57	MA20	O
58	MA19	O
59	MA18	O
60	MA17	O

No.	Pin name	Type
61	MA16	O
62	MA/MD15	O
63	V_{SS}	P
64	MA/MD14	B
65	MA/MD13	B
66	MA/MD12	B
67	MA/MD11	B
68	MA/MD10	B
69	MA/MD9	B
70	MA/MD8	B
71	MA/MD7	B
72	V_{SS}	P
73	V_{DD}	P
74	MA/MD6	B
75	MA/MD5	B
76	MA/MD4	B
77	MA/MD3	B
78	MA/MD2	B
79	MA/MD1	B
80	MA/MD0	B

Pin Descriptions

CPU Interface

Pin name	Pin No.	I/O	Descriptions
$\overline{CS}$	1	I	Chip select for the CPU to access the LC8213 (low active).
$\overline{RD}$	2	I	Read. Set to "L" when the CPU is to read out the LC8213 register.
$\overline{WR}$	3	I	Write. Set to "L" when the CPU is to write to the LC8213 register.
A2 A1 A0	4 5 6	I	Address input for when the CPU accesses LC8213.
D7 D6 D5 D4 D3 D2 D1 D0	9 10 11 12 14 15 16 17	I/O 3 states	Bidirectional 8-bit data bus
IREQ	20	O	Interrupt request signal for the CPU. By reading out the INTR (interrupt request register) the CPU can find the cause of the interruption. IREQ is set to "L" when the CPU reads INTR.
DREQ	21	O	DMA request signal for the external DMA controller. This will be set to "H" in the following cases. * Data exists in the EFIFO during the coding processes. * An empty space exists in the DFIFO during decoding processes. * The DBUF can read/write during data transfer between the image memory bus and CPU bus.
$\overline{DACK}$	22	I	DMA acknowledge signal from the external DMA controller. If $\overline{DACK}$ is set to "L" during coding or decoding, EFIFO and DFIFO will be accessed. DBUF will be accessed if $\overline{DACK}$ is set to "L" during data transfer between the image memory bus and CPU bus.

Image Memory Interface

Pin name	Pin No.	I/O	Descriptions
MA23 MA22 MA21 MA20 MA19 MA18 MA17 MA16	54 55 56 57 58 59 60 61	O 3 states	High-order 8-bit address of the image memory.
MA/MD15 MA/MD14 MA/MD13 MA/MD12 MA/MD11 MA/MD10 MA/MD9 MA/MD8 MA/MD7 MA/MD6 MA/MD5 MA/MD4 MA/MD3 MA/MD2 MA/MD1 MA/MD0	62 64 65 66 67 68 69 70 71 74 75 76 77 78 79 80	I/O 3 states	Low-order 16-bit address and 16-bit data bus for the image memory.
$\overline{AEN}$	41	O	This is set to "L" when the LC8213 is the bus master to the image memory. If $\overline{AEN}$ = "H", MA/MD, $\overline{MRD}$, $\overline{MWR}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{UDE}$ and $\overline{LDE}$ will be a HiZ output.
AST	42	O	This signal indicates that an address is being output to MA/MD15 to MA/MD0.
$\overline{MDEN}$	43	O	This signal indicates that the LC8213 is using MA/MD15 to MA/MD0 as data buses.
$\overline{UDE}$	49	O 3 states	This signal indicates that the high-order bits of the data bus are being used.
$\overline{LDE}$	48	O 3 states	This signal indicates that the low-order bits of the data bus are being used.
$\overline{MRD}$	44	O 3 states	This is set to "L" when data is being read out of the image memory.
$\overline{MWR}$	45	O 3 states	This is set to "L" when data is being written into the image memory.

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Pin name	Pin No.	I/O	Descriptions
$\overline{IORD}$	46	O 3 states	This is set to "L" when data is being read out of the I/O device.
$\overline{IOWR}$	47	O 3 states	This is set to "L" when data is being written into the I/O device.
BREQ	37	O	This signal is used for the LC8213 to request usage rights from the image memory bus.
$\overline{BACK}$	38	I	Input signal allowing the LC8213 to use the image memory bus.
IDREQ	39	I	Input signal used for the I/O device to request DMA from the LC8213.
$\overline{IDACK}$	40	O	DMA acknowledge signal from LC8213.
READY	50	I	This signal is used to delay the read/write signal when using low speed image memory or an I/O device.
DTC	51	O	This signal indicates that the DMA transfer has been completed.

Others

Pin name	Pin No.	I/O	Descriptions
CLK	28	I	External clock (Max. 20MHz)
$\overline{RESET}$	27	I	Reset
TEST0 TEST1 TEST2 TEST3 TEST4	35 34 33 32 30	I	For testing This is normally fixed to "L".
V_{DD}	7, 9, 31, 53, 73		Power supply (+ 5V)
V_{SS}	13, 29, 52, 63, 72		GND

Explanation of Function

- Coding method

  The coding method follows the CCITT T.4, T.6 MH, MR and MMR coding methods that are the standard for the G3 and G4 facsimiles.

- Processing mode

  A maximum of 64k lines for processing can be set, and processing per block is possible. Processing per line is also possible. The coding and decoding FIFOs are built-in, and coding and decoding can be performed alternately for several lines at a time.
  When coding, the LC8213 reads the image data in order from the start address of the image memory set in the register. This data is coded and written into the coding FIFO. When the set number of lines have been processed, the CPU is interrupted.
  When decoding, the LC8213 reads the coded data from the decoding FIFO, reproduces the image data, and writes it into the image memory. When the set number of lines have been processed or a decoding error occurs, the CPU is interrupted.

- Line skip mode

  This mode allows the coded amount of blank lines to be decreased to half of the minimum transmission bits. The line skip bit (blank line judgment bit) is added to the end of the EOL code, and a fill bit is added to the blank line so that the coded amount is half of the minimum transmission bits. For lines that are not completely blank, the normal codes are transmitted after the line skip bit.

- CPU interface

  This interface has an 8-bit data bus, and various operation modes can be set by accessing the interface register. As interface terminals for the external DMA controller are built-in, DMA transfer between the LC8213 and the CPU bus memory is possible.

- Image memory interface

  The image memory address space has 16M bytes.
  The data bus size can be selected from 8-bit or 16-bit.

- DMA transfer function

  DMA transfer is performed between the image memory and I/O device with the internal DMA controller. A maximum of 64k lines can be set for transferring.

- Data transfer function

  Data transfer can be performed without coding/decoding between the CPU bus and image memory bus.

- Pad bit processing

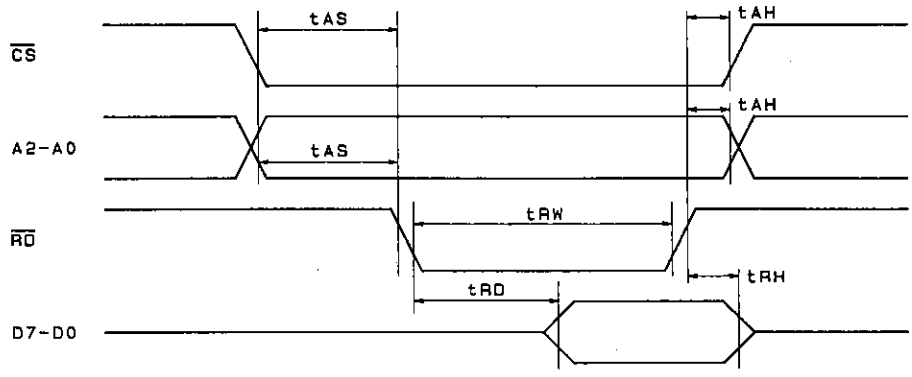
  Pad bit processing can be selected. Pad bit processing is a function that outputs a "0" after 1 line of coded data so that it is an 8-bit unit.

- Parameter settings

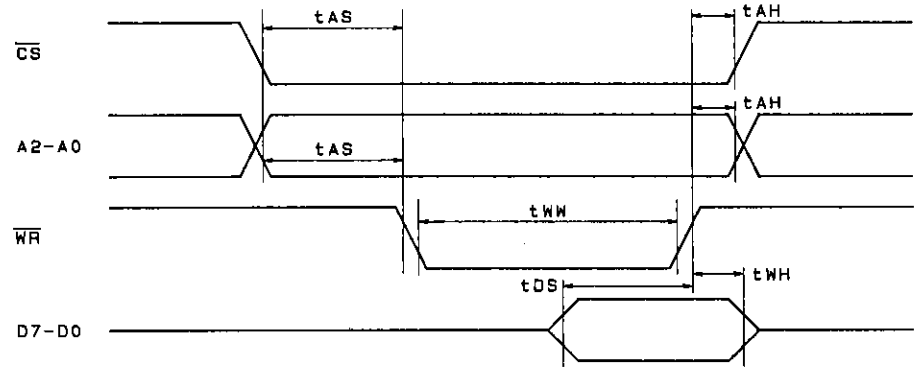
  The following parameters can be set to the listed values.

· No. of processing bits per line (byte unit)	1 to 8k bytes
· Document width (byte unit)	1 to 8k bytes
· No. of processing lines	1 to 64k
· Minimum transmission bits per line	0 to 64k
· K parameters during MR coding	0 to 64k
· No. of processing lines for DMA transfer	1 to 64k
· No. of EOL that structure RTC code	0 to 255

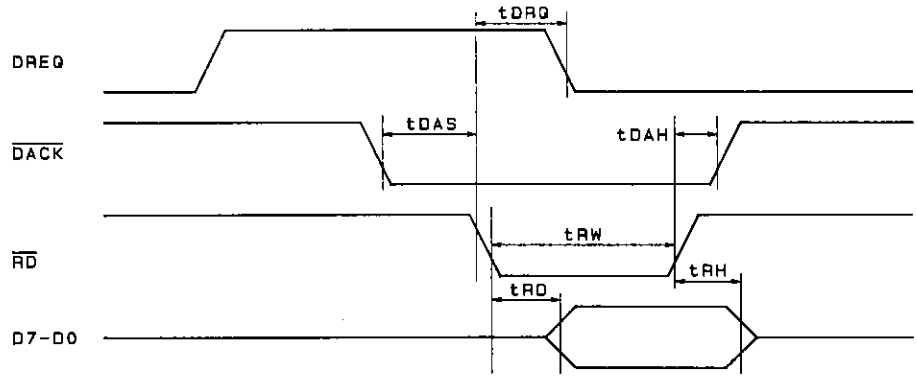
  The document width and no. of processing bits per line can be set separately, so a part of the document can be cut and coded or decoded.



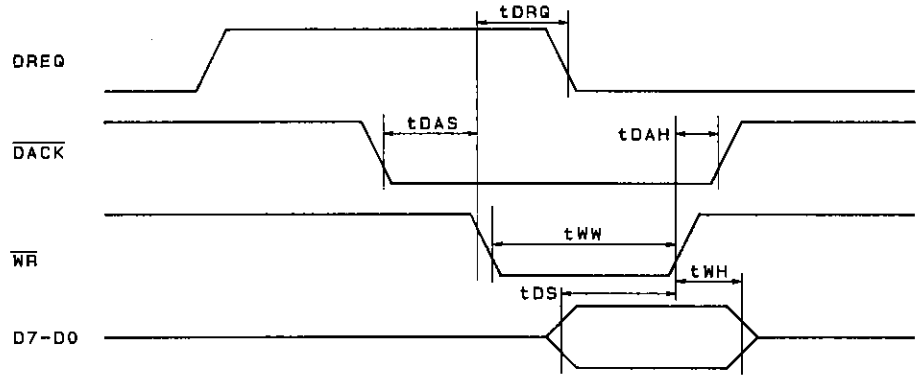
CPU read timing



CPU write timing



DMA controller read timing



DMA controller write timing

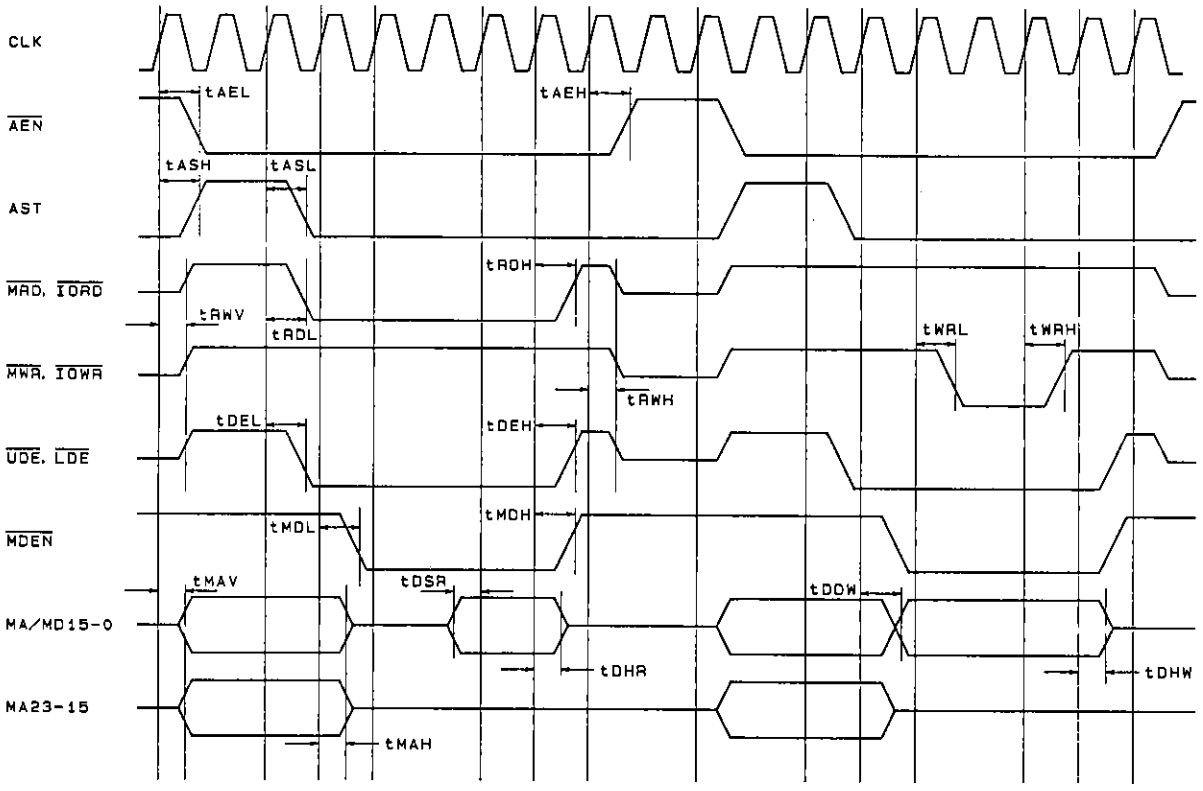
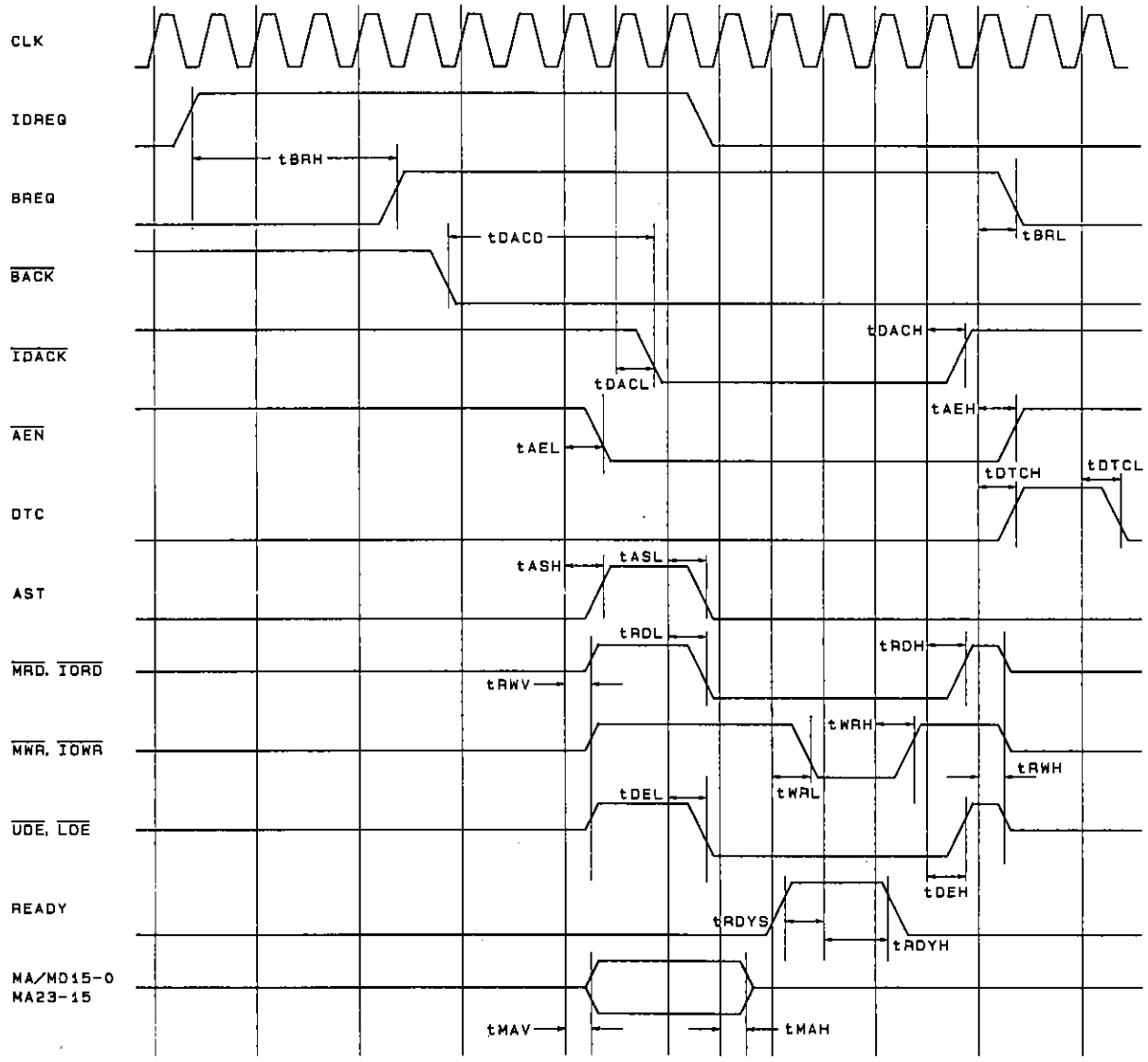
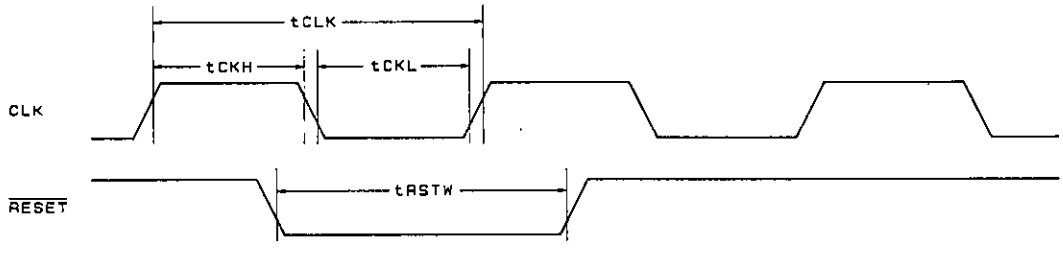


Image memory access



DMA transfer



Clock reset timing