SONY

CXD2564AM

1-bit Audio D/A Converter (with Digital Filter)

Description

The CXD2564AM is a 1-bit stereo D/A converter with a 8× oversampling digital filter (512fs master clock).

Characteristics

Digital filter unit

- Ripple: Less than 0.002dB
- Attenuation: More than –75dB

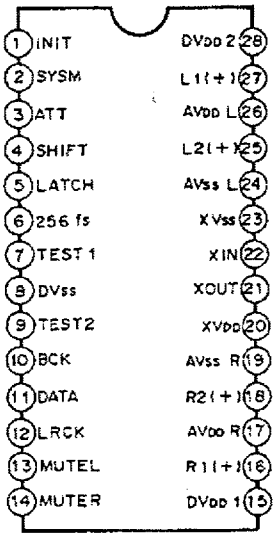
DAC unit

- Dynamic range: 110dB (theoretical value)
- S/N ratio: Better than 100dB
- Distortion: Less than 0.003%

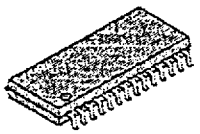
Features

- 512fs master clock
- Sony's original new type of 3rd-order noise shaper
- PLM type of pulse conversion output (complementary PLM)
- Direct digital sync
- 18 or 16 bits selectable as input word length

Pin Configuration (Top View)



28 pin SOP (Plastic)



Structure

Silicon gate CMOS IC

Applications

DATs, Mini Disc players, Digital AV amplifiers, etc.

Absolute Maximum Ratings

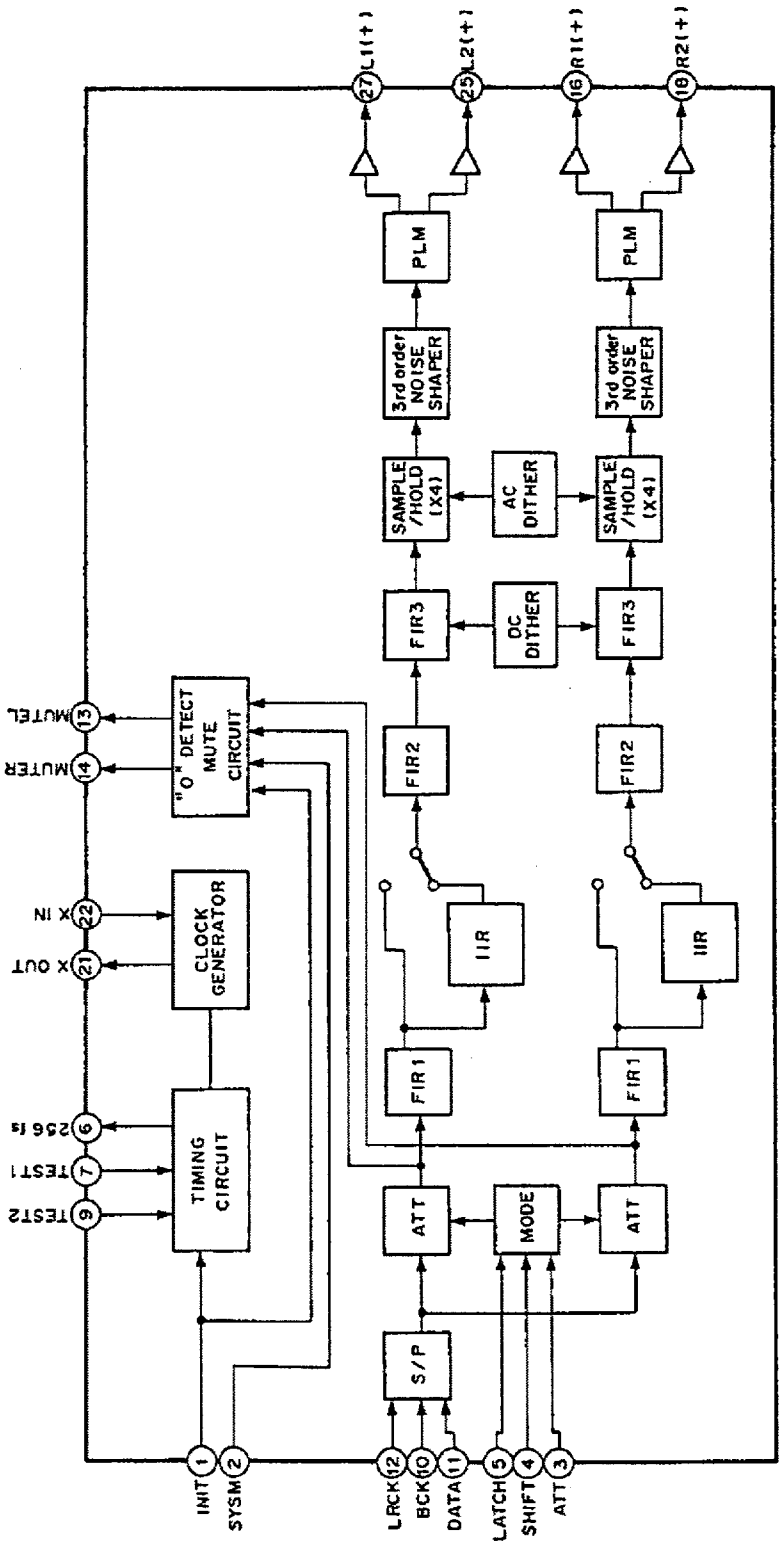
• Supply voltage	V_{DD}	–0.5 to 6.5	V
• Input voltage	V_I	–0.3 to V_{DD}+0.3	V
• Allowable power dissipation	P_D (Ta=60 °C)	500	mW
• Storage temperature	Tstg	–55 to 150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Ta	–10 to 60	°C
• Oscillation frequency	Fx (512fs)	16.3 to 24.6	MHz

E92Z10 - ST

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	INIT	I	Resynchronized at the rising edge of this signal.
2	SYSM	I	System mute input.
3	ATT	I	Serial control data input.
4	SHIFT	I	Shift clock input.
5	LATCH	I	Latch clock input.
6	256fs	O	256fs clock output.
7	TEST1	I	Test pin; normally fixed low.
8	DVss	—	Digital GND.
9	TEST2	I	Test pin; normally fixed low.
10	BCK	I	BCK input.
11	DATA	I	Data input.
12	LRCK	I	LRCK input.
13	MUTEL	O	Left channel mute flag output.
14	MUTER	O	Right channel mute flag output.
15	$DV_{DD}1$	—	Digital power supply.
16	R1(+)	O	Right channel PLM output 1 (positive phase).
17	$AV_{DD}R$	—	Right channel analog power supply.
18	R2 (+)	O	Right channel PLM output 2 (positive phase).
19	AVssR	—	Right channel analog GND.
20	XV_{DD}	—	Master clock power supply.
21	XOUT	O	Crystal oscillator output (512fs).
22	XIN	I	Crystal oscillator input (512fs).
23	XVss	—	Master clock GND.
24	AVssL	—	Left channel analog GND.
25	L2 (+)	O	Left channel PLM output 2 (positive phase).
26	$AV_{DD}L$	—	Left channel analog power supply.
27	L1 (+)	O	Left channel PLM output 1 (positive phase).
28	$DV_{DD}2$	—	Digital power supply.

Electrical Characteristics

DC characteristics

(DV_{DD}=XV_{DD}=$AV_{DD}R$=$AV_{DD}L$=5.0V±5%, DVss=XVss=AVssL=AVssR=0V, Ta=−10 to 60°C)

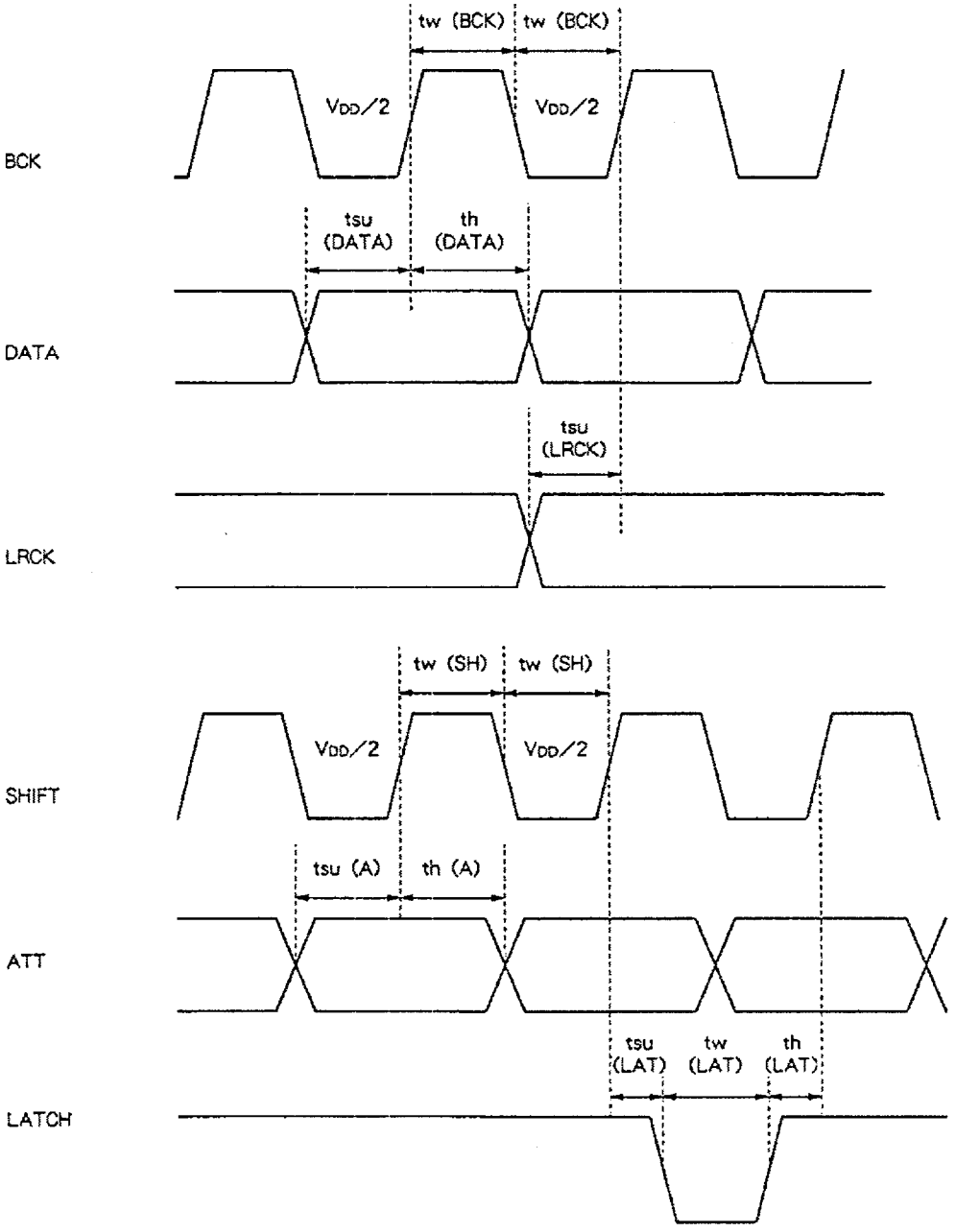
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage	XIN	V_{IHX}		0.90V_{DD}			V
	Others	V_{IH}		0.76V_{DD}			V
Low input voltage	XIN	V_{ILX}				0.10V_{DD}	V
	Others	V_{IL}				0.24V_{DD}	V
Input leak current		I_I		−5.0		5.0	µA
High output voltage	256fs	V_{OH}	I_O=−0.4mA	V_{DD}−0.5			V
	R1, R2 (+) L1, L2 (+)	V_{OHA}	I_O=−12mA	V_{DD}−0.5			V
	XOUT	V_{OHX}	I_O=−1.2mA	V_{DD}−0.5			V
	MUTEL, MUTER	V_{OHM}	I_O=−1.0mA	V_{DD}−0.5			V
Low output voltage	256fs	V_{OL}	I_O=0.4mA			0.4	V
	R1, R2 (+) L1, L2 (+)	V_{OLA}	I_O=12mA			0.5	V
	XOUT	V_{OLX}	I_O=1.2mA			0.5	V
	MUTEL, MUTER	V_{OLM}	I_O=1.0mA			0.4	V
Current consumption		I_{DD}			20	60	mA

AC characteristics

(DV_{DD}=XV_{DD}=$AV_{DD}R$=$AV_{DD}L$=5.0V±5%, DVss=XVss=AVssL=AVssR=0V, Ta=−10 to 60°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BCK pulse width	tw (BCK)		160			nsec
DATA setup time	tsu (DATA)		20			nsec
DATA hold time	th (DATA)		20			nsec
LRCK setup time	tsu (LRCK)		50			nsec
XIN duty	duty (XIN)	V_{DD}/2 at 25MHz		50		%
SHIFT pulse width	tw (SH)		100			nsec
ATT setup time	tsu (A)		20			nsec
ATT hold time	th (A)		20			nsec
LATCH setup time	tsu (LAT)		20			nsec
LATCH hold time	th (LAT)		100			nsec
LATCH pulse width	tw (LAT)		100			nsec

Input/AC timing



Analog characteristics (DVDD=XVDD=AVDDR=AVDDL=5.0V, DVSS=XVSS=AVSSL=AVSSR=0V, Ta=25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD+N	Input data 1kHz, 0dB (Fs=44.1kHz)			0.0030	%
S/N ratio	S/N	Input data 1kHz, 0/– ∞ 0dB (Fs=44.1kHz)	100			dB

Description of Functions

1) Mute function

(1) Zero data detection
Detection is performed after attenuation processing.
- The zero detection flag is output when the upper 14 bits of the input data are all "0" or all "1", and the remaining lower bits are continually in the DC state.
- The detection time can be selected as either 60ms or 300ms by serial control.
- Even if the zero detection flag is being output, the digital filter operates normally.

(2) Digital filter mute (D/F MUTE)
- MUTE is active when it is high in serial control ATT mode.
- Output from the D/F section is set to ["0"+DC offset].
- The internal operations of the digital filter are performed normally.

(3) Noise shaper mute (NS MUTE)
- NS mute is active when it is high in serial control system mode and any of the following conditions are met:
  - The zero detection flag has been set.
  - A high signal is input to the input pin SYSM (=mute).
  - The D/F MUTE flag has been set.
- The noise shaper output is switched to output with a DC offset component added on by the D/F section.
- The internal operations of the noise shaper are performed normally, and after muting is turned off, the output immediately switches to that from the noise shaper.

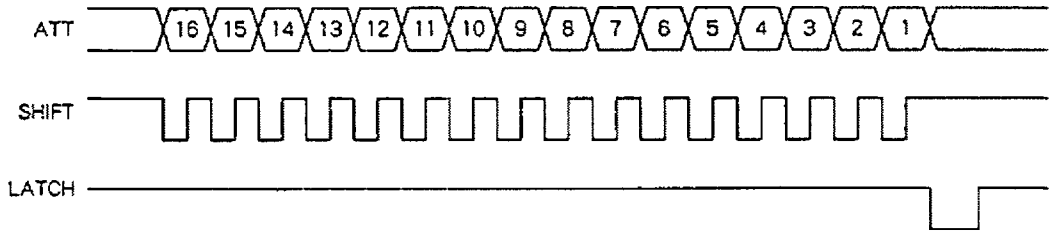
(4) INIT low mute
- The D/F section input data is set to "0".
- Clears the internal RAM.
- The D/F section output is set to ["0"+DC offset].
  (After the internal RAM is cleared, and before the internal INIT.)
- After the internal INIT goes low, the noise shaper section registers are cleared including the pre-value hold section, and the output is set to duty 50% PWM (equivalent to "0").

2) Mute flag output (MUTEL, MUTER pins)

- When any of the following conditions are met, the mute active flag is output from the MUTEL and MUTER pins. (The polarity of the flag can be selected by the serial control.)
  - The zero detection flag has been set.
  - A high signal (=mute) is input to the input pin SYSM.
  - The D/F MUTE flag has been set.
  - The external INIT is active.

3) Serial control

- The mode is set by transferring mode data to the ATT, SHIFT, and LATCH pins.
- The transfer format is shown below.



- Bit 1 data is always "0".
- When bit 2 data is "0", attenuate mode is set.
  When bit 2 data is "1", system mode is set.
- The setting is made after the external INIT is released.
  (The mode setting table is shown on the following page.)

* SYNC function
- When SYNC is set high in the serial control system mode, resynchronization is performed only once at the rising edge.
- A minimum period of 4fs and a maximum period of 5fs are required until internal synchronization is achieved.

Serial control

- **Attenuate mode**

Bit	Mode flag	Function	High	Low
1	MODE1	MODE switching	Test mode	Normal mode
2	MODE2	MODE switching	System mode	Attenuate mode
3	EMP	De-emphasis	ON	OFF
4	MUTE	"0"+ DC offset output	ON	OFF
5	ATT1	Attenuate data (MSB)		
6	ATT2	Attenuate data		
7	ATT3	Attenuate data		
8	ATT4	Attenuate data		
9	ATT5	Attenuate data		
10	ATT6	Attenuate data		
11	ATT7	Attenuate data		
12	ATT8	Attenuate data		
13	ATT9	Attenuate data		
14	ATT10	Attenuate data		
15	ATT11	Attenuate data		
16	ATT12	Attenuate data (LSB)		

* When INIT is set low, MODE1, MODE2, EMP and MUTE are reset low and ATT is set to 400H.

• System mode

Bit	Mode flag	Function	High	Low
1	MODE1	MODE switching	Test mode	Normal mode
2	MODE2	MODE switching	System mode	Attenuate mode
3	IFORM	Input data format	LSB first	MSB first
4	IBIT	Input data word length	18 bits	16 bits
5			don't care	
6			don't care	
7			don't care	
8	TEST1	Test mode setting	Normally fixed low	
9	TEST2	Test mode setting	Normally fixed low	
10	NS	Noise shaping	don't care	
11	MT1	Zero data detection time	60ms	300ms
12	MT2	Zero mute flag polarity	Mute when high	Mute when low
13	FS32	De-emphasis fs selection	* Refer to the table below	
14	FS48	De-emphasis fs selection	* Refer to the table below	
15	SYNC	I/O synchronization	ON	OFF
16	NSMUTE	NS mute function	ON	OFF

* When INIT is set low, all are reset low.
* De-emphasis fs selection

		32.0k	44.1k	48.0k	37.8k
13	FS32	High	Low	Low	High
14	FS48	High	Low	High	Low

4) INIT function

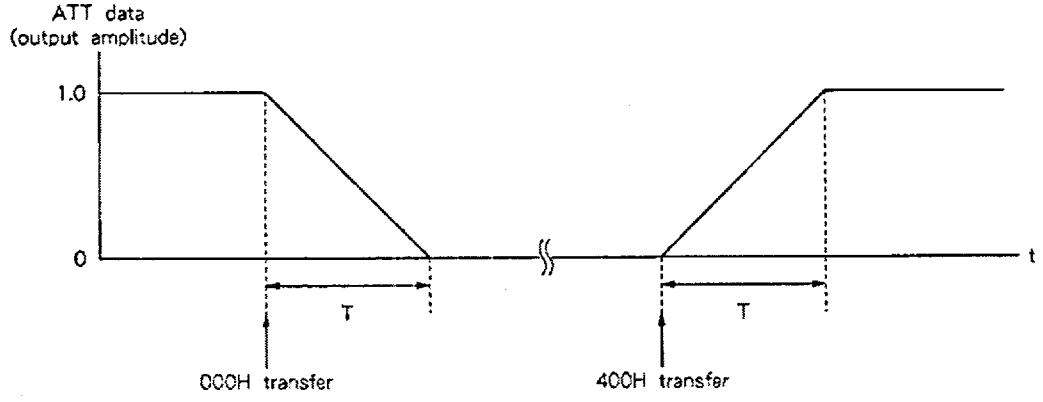
- After the rising edge of the external INIT signal, once resynchronization has been performed, the D/F and NS sections are immediately and simultaneously released from the reset state.
- The external LRCK is not changed by the external INIT signal, so that after the rising edge of the external INIT signal the phase of the internal LRCK is synchronized with the initial external LRCK at the master clock level.
- A minimum period of 4fs and a maximum period of 5fs are required until internal synchronization is achieved.
- The internal INIT is delayed by approximately 2 to 2.5ms after the falling edge of the external INIT signal.

5) Double-speed operation

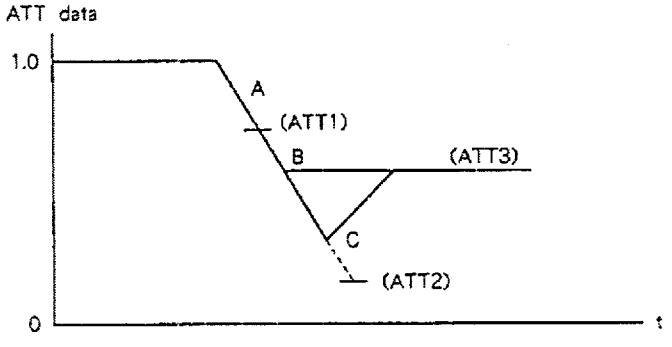
- Synchronization is maintained for signals input at double speed, while internal operations are performed at normal speed.

6) Attenuator

- ATT data is transferred using the 12 bits from bit 5 (MSB) to bit 16 (LSB). The size is 000H (0.0) to 400H (1.0). When the INIT is low, the ATT data is set to 400H.

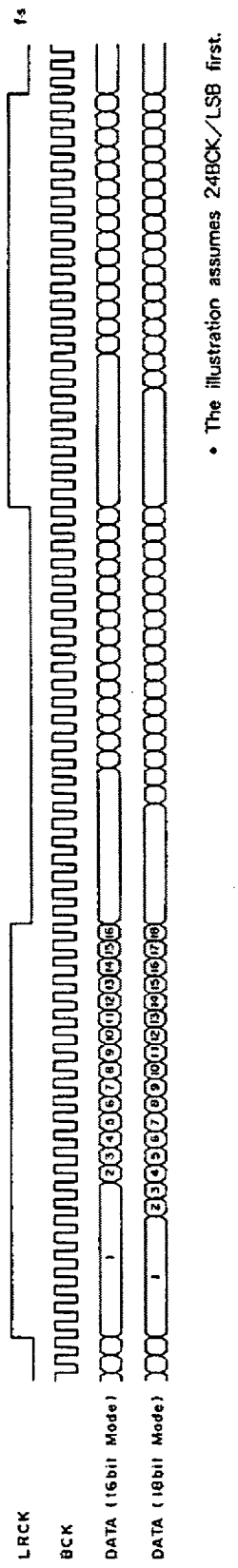


The soft muting is performed by transferring 000H as the ATT data. To release this function, the ATT data prior to soft muting (400H in the above illustration) is transferred.



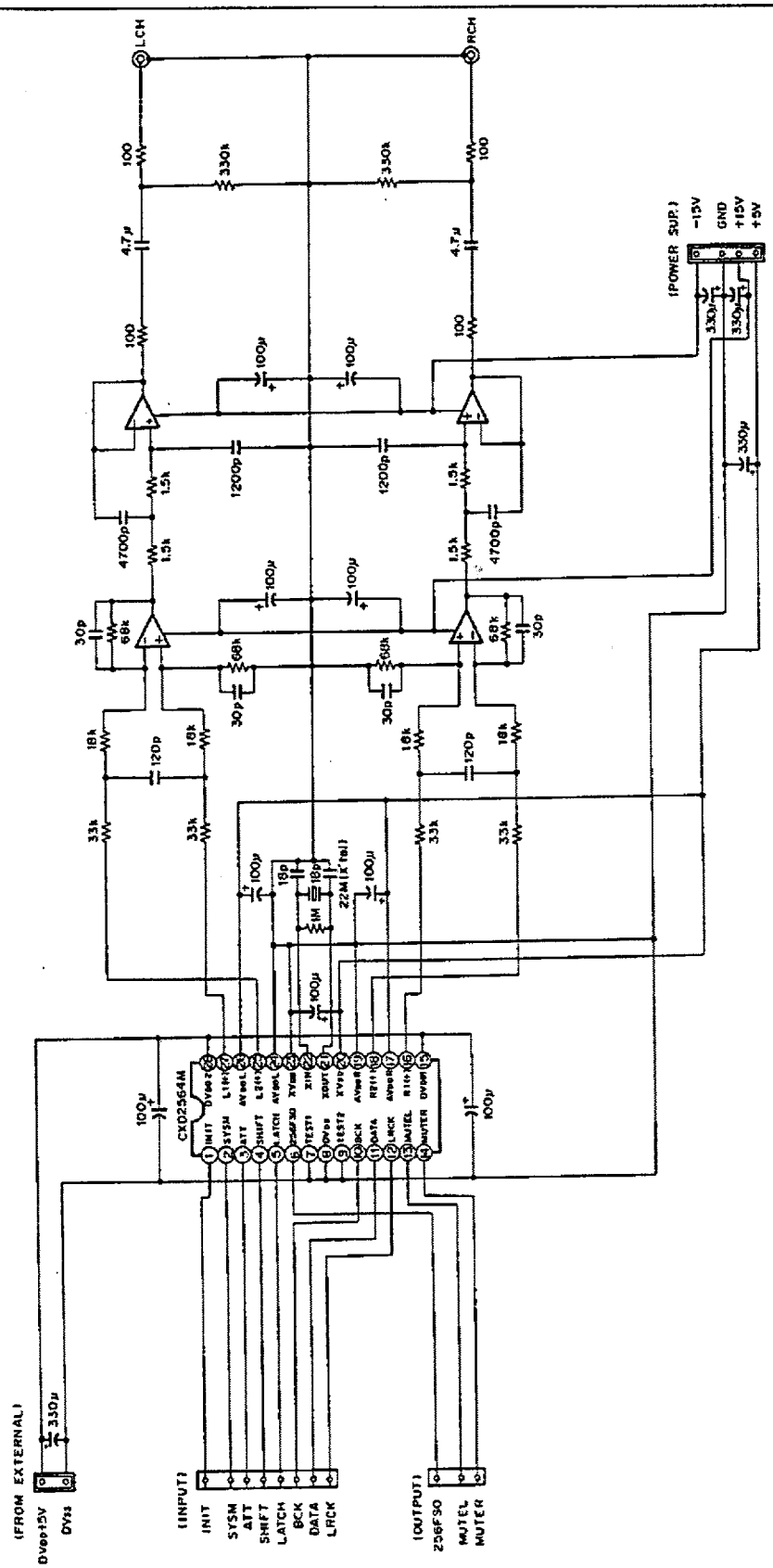
In this way, ATT data is always sent through the soft muting operation. In the above illustration, assume ATT data where ATT1>ATT3>ATT2, and that first ATT1 is transferred, followed by ATT2. If ATT2 was transferred before the ATT1 value was attained (state "A" in the illustration), ATT1 is ignored and the value approaches ATT2. Next, ATT2 is transferred, and if ATT3 is transferred before the ATT2 value is attained ("B" or "C" in the illustration), ATT2 is ignored and the value approaches ATT3.

Data Input Timing



• The illustration assumes 24BCK/LSB first.

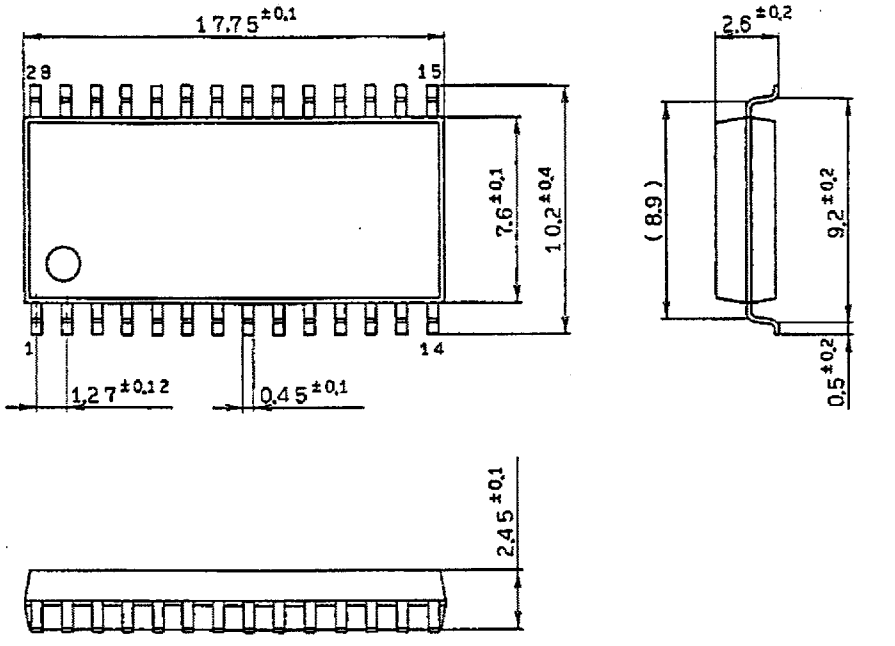
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

28pin SOP (Plastic) 375mil



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