SONY

CXA1484M/N

Low Current Consumption FM IF Amplifier for Double Conversion Pagers

Description

The CXA1484M/N is a low current consumption FM IF amplifiers which employ the newest bipolar process. It is suitable for double conversion pagers for overseas through built-in second mixer.

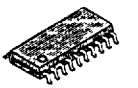
Features

- Low current consumption 1.4mA (typ. at Vcc=1.5V)
- Built-in second mixer oscillator
- Low voltage operation Vcc=1.0 to 4.0V
- Few external parts for needless of IF decoupling capacitor
- Built-in reference power supply for operational amplifier and comparator
- Small package 20-pin VSOP

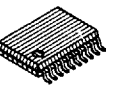
Functions

- Second mixer and oscillator
- Second IF and limiter amplifiers
- FM detector
- Quaternary LPF operational amplifier
- FSK comparator
- Regulator output for RF amplifier and first mixer
- Low voltage detection circuit

CXA1484M
20 pin SOP (Plastic)



CXA1484N
20 pin VSOP (Plastic)



Applications

Double conversion pagers for overseas

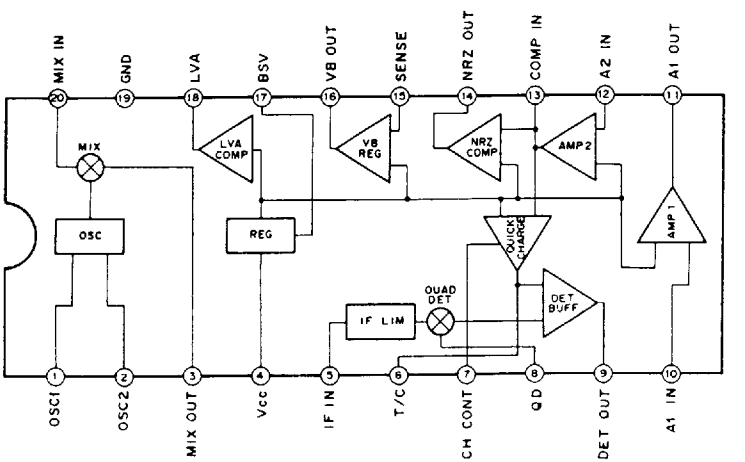
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	Vcc	12.0	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C

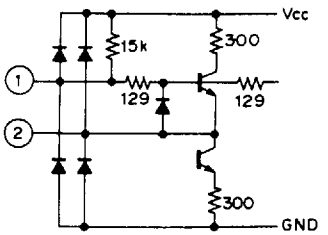
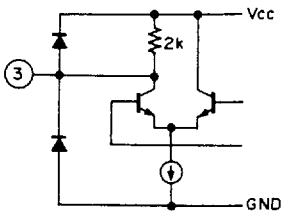
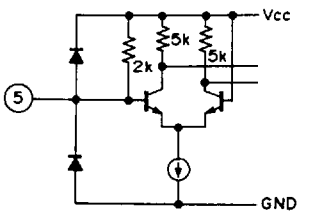
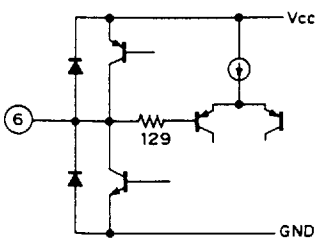
Operating Condition

Supply voltage	Vcc	1.0 to 4.0	V

Block Diagram



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 2	OSC1 OSC2	1.5V 0.8V		Connecting pin of external parts for crystal oscillator circuit. Connects a capacitor and crystal oscillator to these pins and Vcc.
3	MIX OUT	1.3V		Mixer output. Connect a 455kHz ceramic filter between this pin and IF IN.
4	Vcc			Vcc
5	IF IN	1.5V		IF limiter amplifier input.
6	T/C	0.2V		Connects a capacitor that determines the low cut-off frequency for the entire system.

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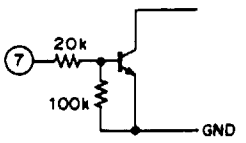
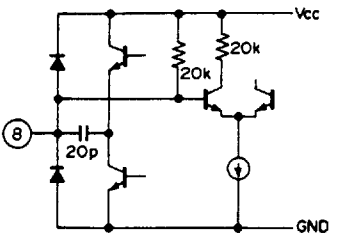
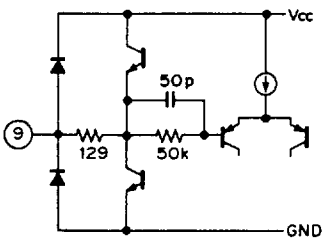
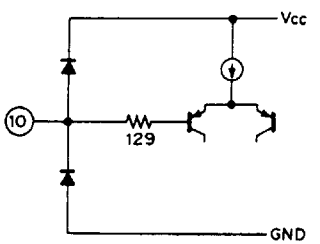
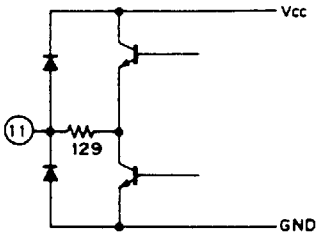
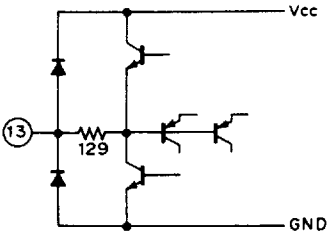
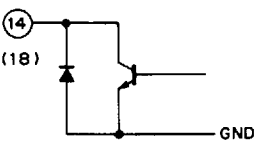
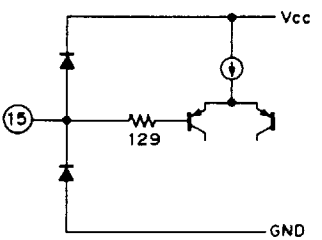
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7	CH CONT	0V		Controls the ON/OFF operation of the quick-charge circuit. (Input voltage range: –0.5 to +7.0V)
8	QD	1.5V		Connects to the phase shifter of FM detector circuit.
9	DET OUT	0.2V		FM detector output.
10 12	A1 IN A2 IN	0.2V 0.2V		Input for operational amplifiers 1 and 2 (AMP1, AMP2).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	A1 OUT	0.2V		Output for operational amplifier 1 (AMP1).
13	COMP IN	0.2V		NRZ comparator input. Output for operational amplifier 2 (AMP2) is output.
14 18	NRZ OUT LVA OUT	— —		NRZ and LVA comparator output and are open collectors. (Applied voltage range: –0.5 to +7.0V)
15	SENSE	0.2V		Input pin for internal constant-voltage source amplifier. This pin is controlled to maintain 200mV.

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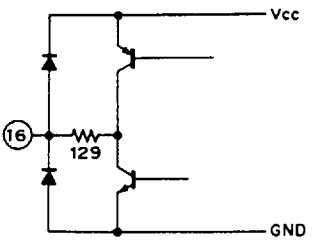
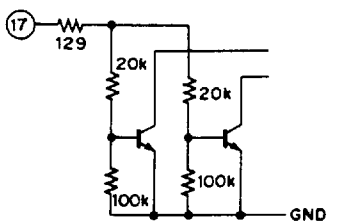
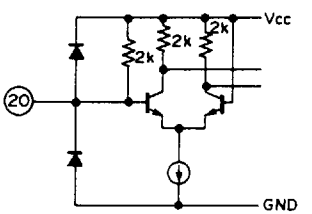
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	VB OUT	—		Output pin for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 200 μA)
17	BSV	—		Controls battery saving. Setting this pin low suspends the operation of IC. (Input voltage range: –0.5 to +7.0V)
19	GND	—		GND
20	MIX IN	1.5V		Mixer input.

Electrical Characteristics (Vcc=1 5V, Ta=25℃, Fs=21.7MHz, FMOD=256Hz, FDEV=2.3kHz, AMMOD=30%)

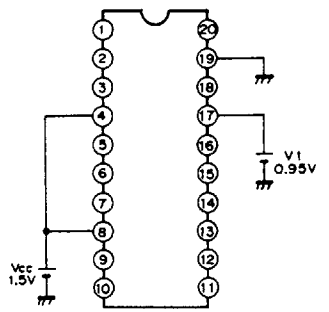
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Icc	Test circuit 1	1.0	1.4	1.8	mA
Current consumption	Iccs	Test circuit 1, V1=0.3V			20	μA
AM rejection ratio	AMRR	Test circuit 3	25			dB
Op amp. input bias current	IBIAS	Test circuit 2		40	100	nA
Op amp. open loop gain	Av	Test circuit 4	45	60		dB
Op amp. output voltage amplitude	Vo	Test circuit 5	0.65			Vp-p
NRZ output saturation voltage	VSATNRZ	Test circuit 8			0.4	V
NRZ output leak current	ILNRZ	Test circuit 7			5.0	μA
NRZ hysteresis width	VTWNRZ	Test circuit 6	5	10	17	mV
VB output current	IOUT	——			200	μA
VB output saturation voltage	VSATVB	Test circuit 9			0.4	V
VB SENSE voltage	VSENVB		200	215	230	mV
LVA operating voltage	VLVA	Test circuit 10	1.10	1.15	1.20	V
LVA hysteresis	VTHLVA	Test circuit 10	10	50	100	mV
LVA output leak current	ILLVA	Test circuit 10			5.0	μA
LVA output saturation voltage	VSATLVA	Test circuit 10			0.4	V
Detector output voltage	VODET	Test circuit 3	16	20	28	mV
Logic input voltage high level	VTHBSV	——	0.9			V
Logic input voltage low level	VTLBSV	——			0.35	V
Limiting sensitivity	VIN (LIM)	Test circuit 3		7	14	dBμ

3

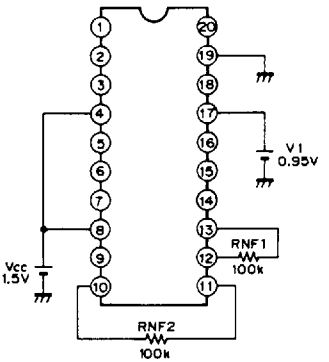
Design Data

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Mixer input resistance	RINLIM		1.6	2.0	2.4	kΩ
Mixer input capacitance	CINMIX			3.0		pF
Mixer output resistance	ROUTMIX		1.6	2.0	2.4	kΩ
IF limiter input resistance	RINLIM		1.6	2.0	2.4	kΩ
IF limiter gain stability	GSLIM		−6		+6	dB
DET OUT output resistance	ROUTDET				200	Ω
Op amp. maximum input voltage		Vcc=1.1V	0.39			V
Op amp. minimum input voltage					0.05	V
Comparator maximum input voltage		Vcc=1.1V	0.39			V
Comparator minimum input voltage					0.05	V
Op amp. offset voltage					3.0	mV

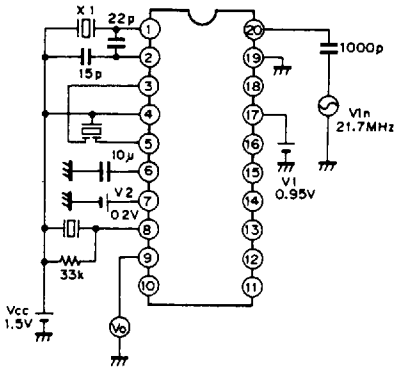
Test Circuit



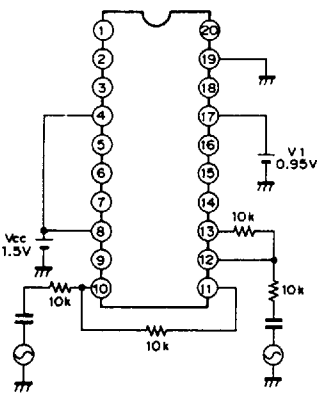
Test circuit 1



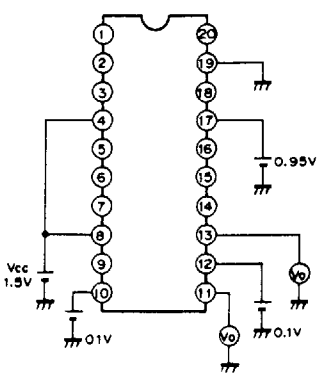
Test circuit 2



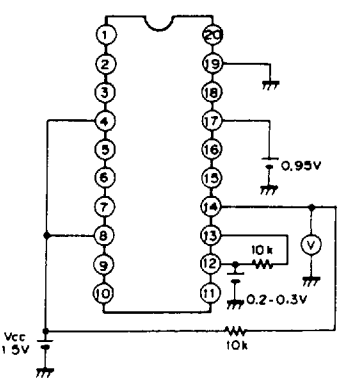
Test circuit 3



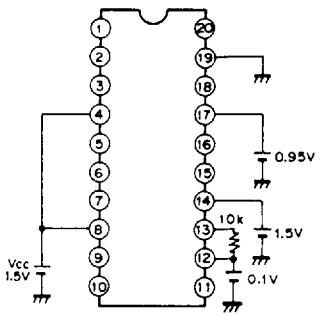
Test circuit 4



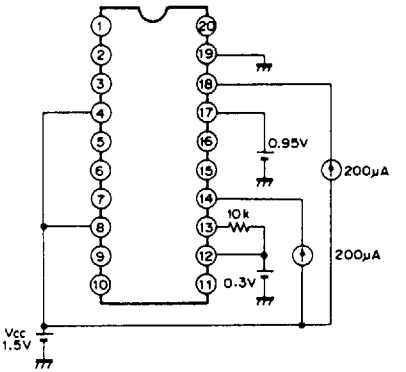
Test circuit 5



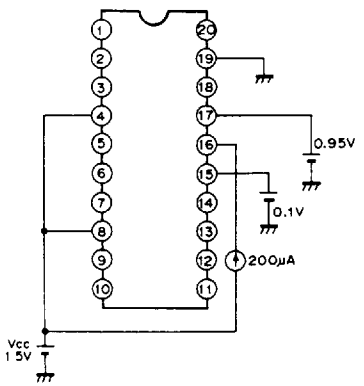
Test circuit 6



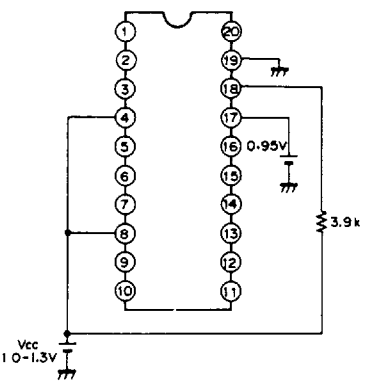
Test circuit 7



Test circuit 8



Test circuit 9



Test circuit 10

1) Power Supply

The CXA1484M/N, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.0 to 4.0V. Decouple the wiring to Vcc (Pin 4) as close to the pin as possible.

2) Oscillator Input

Oscillator input method

a) Using Pin 1 and 2, input self-excited oscillation signal through the composition of a Colpitts type crystal oscillator circuit.

b) Directly input a local oscillation signal to Pin 1.

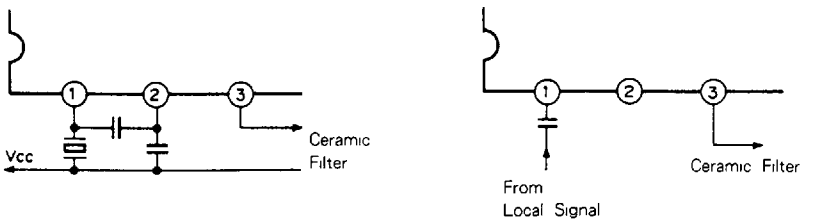


Fig. 1

3) Mixer

The mixer is of double-balance type. Pin 20 is the input pin. Input through a suitable matching circuit. The input impedance is 2.0kΩ .
Pin 3 serves as the output pin for the mixer, and a load resistance of 2.0kΩ is built in.

4) IF Filter

The filter to be connected between this mixer and the IF limiter amplifier should have the following specifications.

Input impedance : 2.0kΩ ± 10%
Band width : Changes according to applications

5) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100dB so that, note that the following points about wiring to the IF limiter amplifier input pin (Pin 5).

a) Be sure to wire to the IF limiter amplifier input (Pin 5) as short as possible.

b) As the IF limiter amplifier output appears at QD (Pin 8), be sure to wire to the RLC and ceramic discriminator connected to QD as short as possible and reduce the interference on the mixer output and IF limiter amp input.

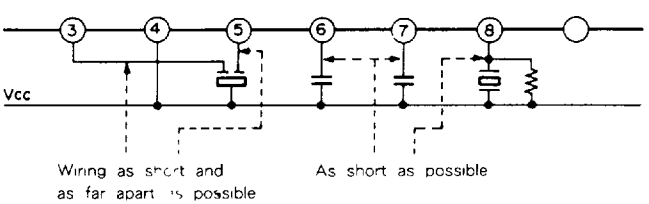


Fig. 2

6) Quick Charge

In order to hasten the rising time from when power is turned on or when reception standby, the CXA1484M/N features a quick charge circuit.
Therefore, the quick charge circuit eliminates the need to insert capacitor between the detector output and the LPF as is the case with conventional ICs, but connects capacitor to Pin 6 to determine the average signal level during steady-state reception.
Connect a signal for controlling the quick charge circuit to Pin 7. Setting this pin high enables the quick charge mode, setting this pin low enables the steady-state reception mode.
Connect Pin 7 to GND when quick charge is not being used.

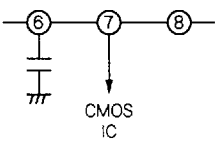
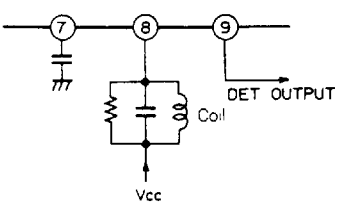


Fig. 3

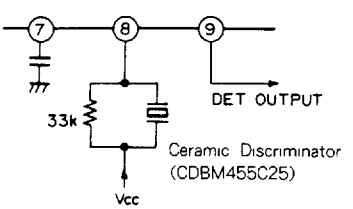
7) Detector

The detector is a quadrature type. To perform phase shift, connect RLC resonator circuit or ceramic discriminator to Pin 8.
The phase shifting capacitor for the quadrature detector is built in.
This detector attenuates the high frequency components of the demodulated FM (FSK) signal with the internal CR-constructed LPF, and outputs it to DET OUT (Pin 9).
DET OUT output impedance is 200Ω or less.

The CDBM455C25 (MURATA MFG. CO., LTD.) ceramic discriminator for the CXA1484M is recommended.



a) Coil



b) Ceramic Discriminator

Fig. 4

8) AMP, NRZ OUT

Two operational amplifiers are built in this IC.
One of them is connected internally to an NRZ comparator.

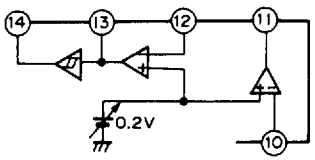


Fig. 5

Using these two operational amplifiers to construct an LPF, remove noise from the demodulated signal and input to the NRZ comparator, which is the next stage.
The NRZ comparator molds waveform of this input signal and outputs it as a square wave. The NRZ comparator output stage is for open collector.
Thus, if the CPU is a CMOS-type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

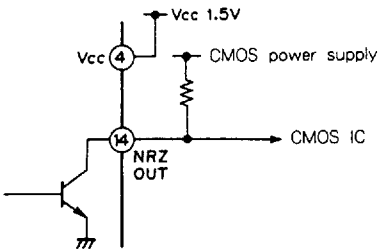


Fig. 6

9) VB SENSE, VB OUT

Controls the base bias of the external transistors.

10) LVA OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device as can NRZ OUT. The setting voltage of the LVA is 1.15V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50mV (typ.).

11) BSV

Operation of the CXA1484M/N can be halted by setting this pin low. This pin also can be connected directly to CMOS device. Also, the current consumption for BSV is 20 μA or less (at 1.5V).

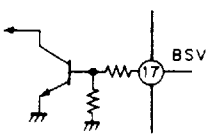


Fig. 7

Principle of Quick Charge Operation

BUF in Fig. 8 is the detector buffer amplifier, and AMP1 and AMP2 are operational amplifiers to construct LPF. COMP is the NRZ comparator. Coupling on conventional system is performed by placing a capacitor between the detector buffer and the LPF operational amplifier, matching of DC is not performed . Thus, this matching capacitor must be charged when restoring the system from reception standby mode to reception mode, within which time signals from the comparator appear at the NRZ output.

To shorten this rise time, as shown in Fig.8 the CXA1484 adds feedback loop from the comparator input to the input circuit of output. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set inside the feedback loop. Switching the current of quick change circuit enables reduction of the rise time.

In this block, CHG is comparator which compares the input voltage and outputs current based on this comparison. The current on CHG is switched between high and low at Pin 7. To shorten the time constant when switching from reception standby mode to reception mode, switch the current to high and increase the charge current at C in Fig. 8. During steady-state reception mode, switch the current to low, lengthening the charge time constant, and allowing for stable data retrieval.

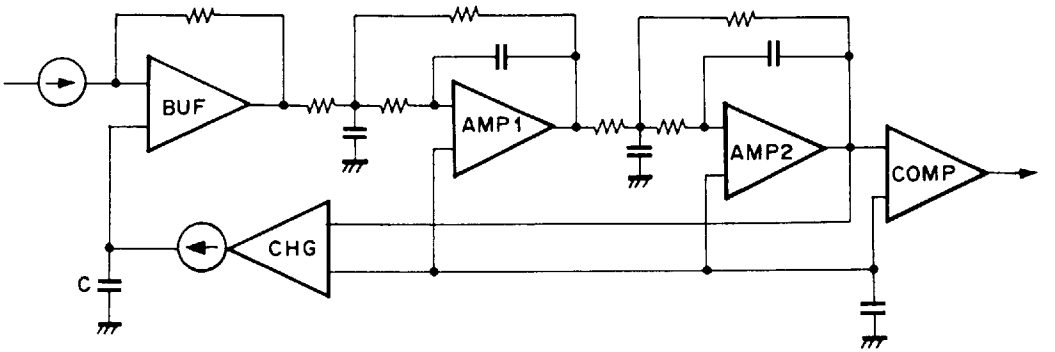
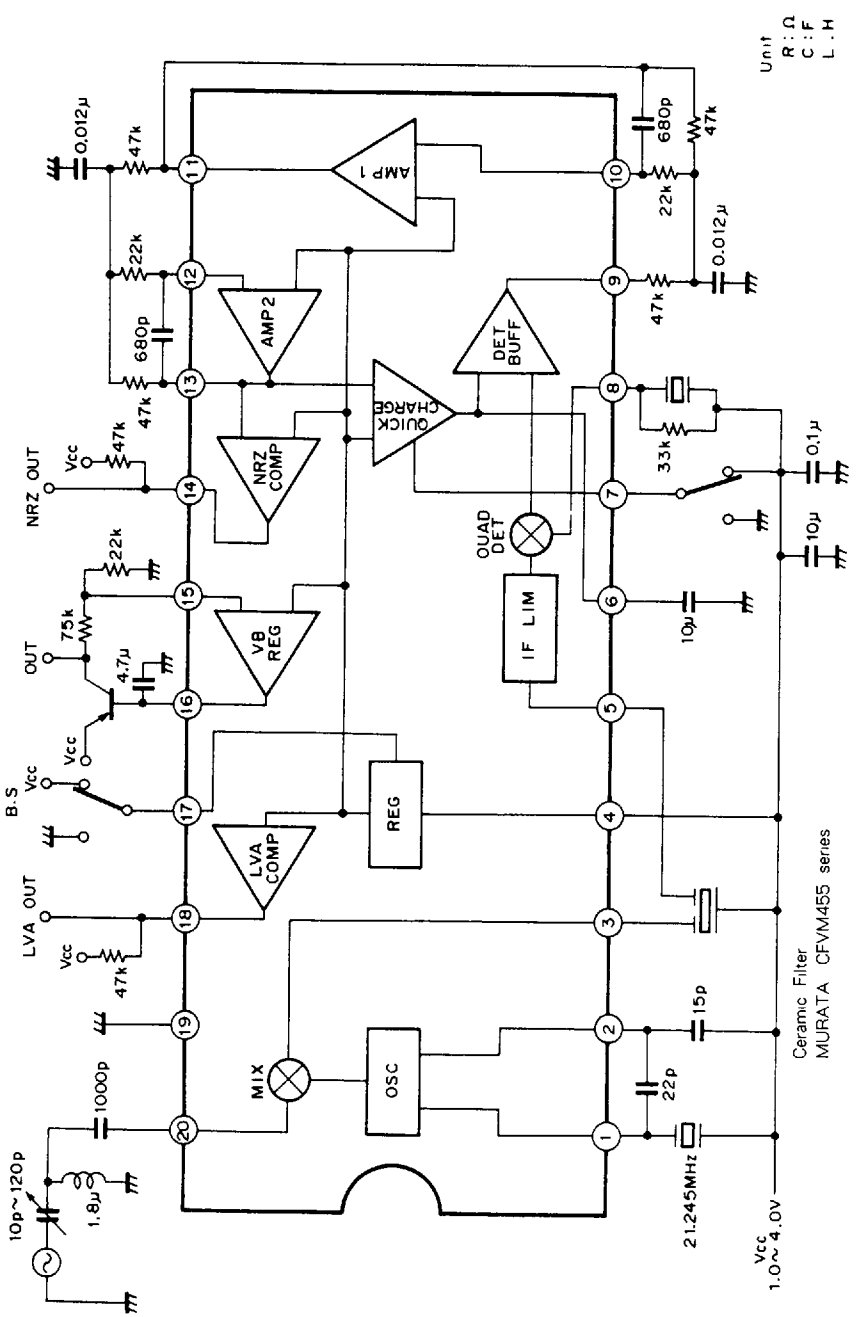


Fig. 8

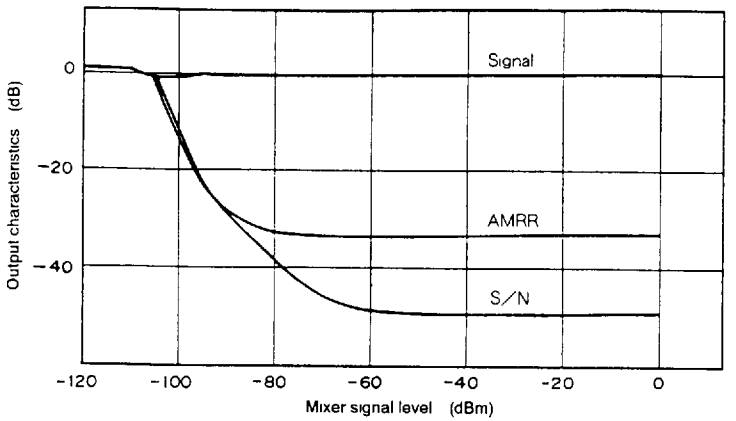
Application Circuit



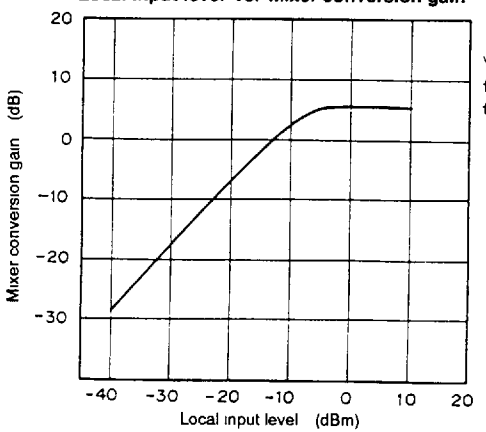
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Example of Representative Characteristics

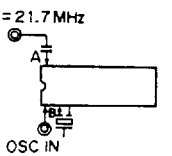
Mixer signal level vs. Output characteristics



Local input level vs. Mixer conversion gain

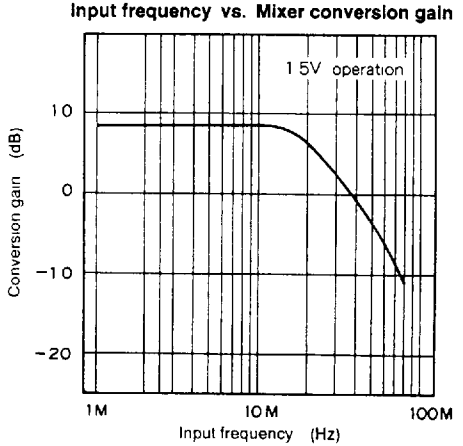


Vcc = 1.5V
fs = 21.7MHz
fLOCAL = 21.245MHz

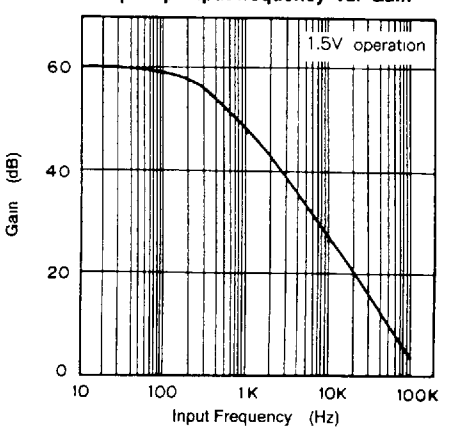


Tests the ratio of A and B

Input frequency vs. Mixer conversion gain

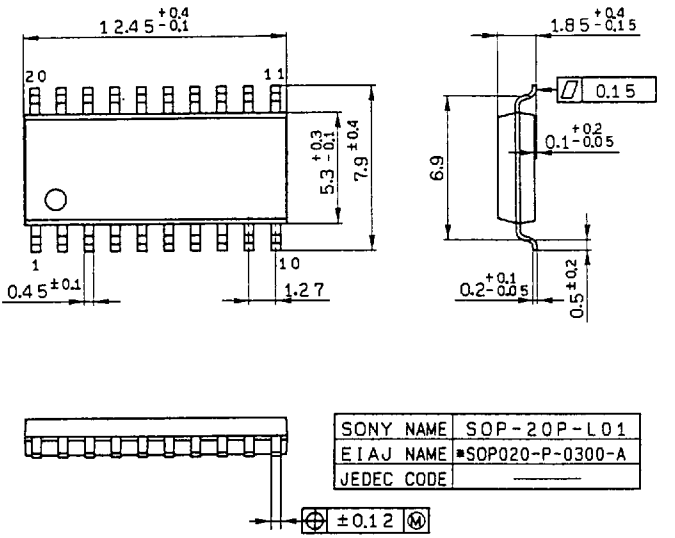


Op amp. input frequency vs. Gain



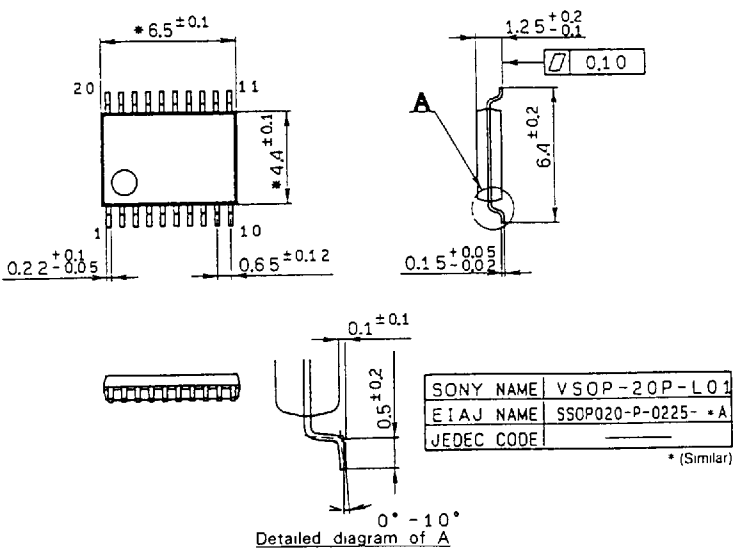
Package Outline Unit : mm

CXA1484M 20pin SOP (Plastic) 300mil 0.3g



SONY NAME	SOP-20P-L01
EIAJ NAME	*SOP020-P-0300-A
JEDEC CODE	———

CXA1484N 20pin VSOP (Plastic) 225mil



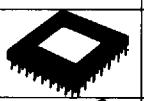
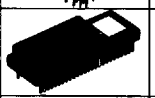
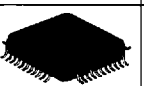
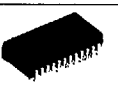
Detailed diagram of A

SONY NAME	VSOP-20P-L01
EIAJ NAME	SSOP020-P-0225- *A
JEDEC CODE	———

* (Similar)

Note) Dimensions marked with * does not include resin residue

Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C···Ceramic

2