ML6672*

ATM UTP Transceiver

GENERAL DESCRIPTION

The ML6672 is a complete monolithic transceiver for 155Mbps NRZ encoded data transmission over Category 5 Unshielded Twisted Pair and Shielded Twisted Pair cables. The ML6672 is compliant with the ATM Forum 155Mbps Twisted Pair Specification. The adaptive equalizer in the ML6672 will accurately compensate for line losses of up to 100m of UTP. The part requires only external 1% resistors for accurate equalization.

The ML6672 receive section consists of an equalizing filter with a feedback loop for controlling effective line compensation. The feedback loop contains a filter and detection block for determining the proper control signal. An ECL 100K compatible buffer at the output interfaces directly with ATM physical interface chips.

The ML6672 transmit section accepts ECL 100K compatible NRZ inputs.

Several additional functions are provided by the ML6672 to simplify applications. A common-mode reference is provided to set the input DC level for the equalizer and the near-end transformer winding. This terminal may be used as an AC ground for the transformer center-tap or termination resistors. A link status circuit monitors line integrity and provides a proper logic level output signal to interface with the host system.

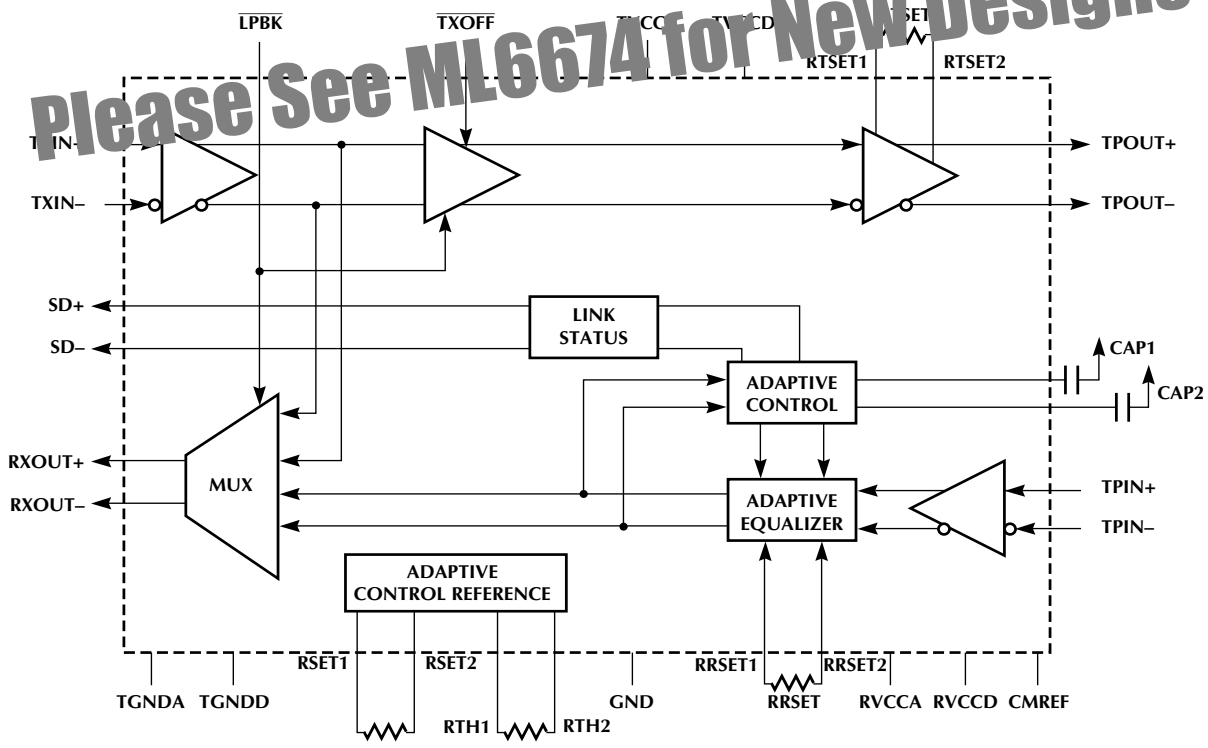
The ML6672 is implemented in a BiCMOS process. A differential signal path throughout minimizes the effects of power supply transients and noise.

FEATURES

- Complies with ATM Forum 155Mbps Twisted Pair Specification
- Transmitter can be externally turned off for true quiet line
- Receiver includes adaptive equalizer
- Operates over 100 meters of STP or category 5 UTP Twisted Pair Cable
- Semi-standard options available

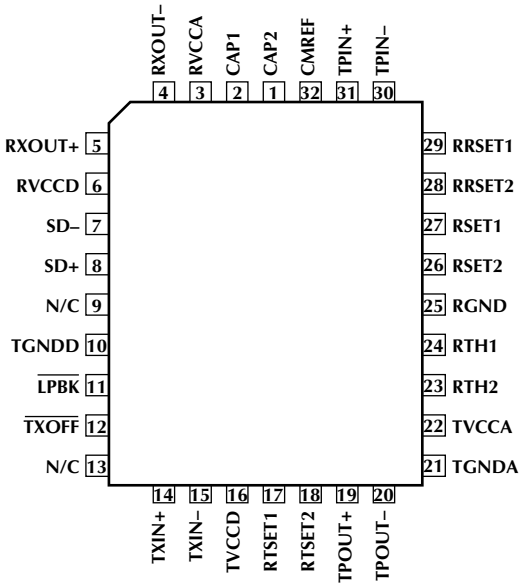
*** This Part Is End Of Life As Of August 1, 2000**

BLOCK DIAGRAM

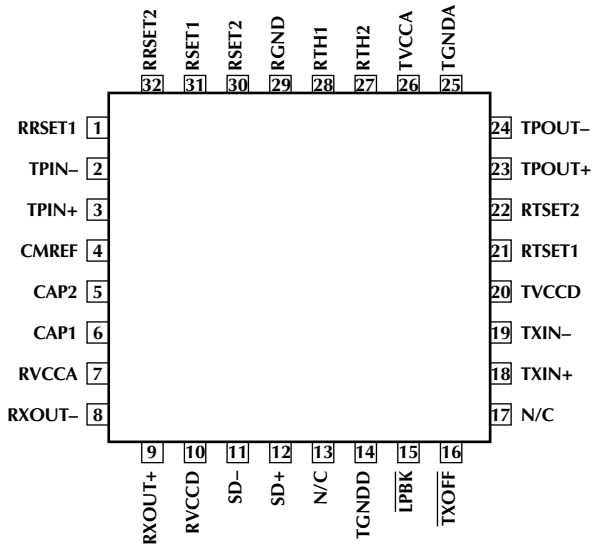


PIN CONFIGURATION

ML6672
32-Pin PLCC (Q32)



ML6672
32-Pin TQFP (H32-7)



PIN DESCRIPTION

NAME	FUNCTION
$TX_{IN}+$, $TX_{IN}-$	These differential ECL100K compatible inputs receive NRZ data from the PHY for transmission.
TPOUT+, TPOUT–	Outputs from the NRZ buffer drive these differential current outputs. The transmitter filter/transformer module connects the media to these pins.
$\overline{\text{LPBK}}$	This TTL input enables transmitter-Receiver loopback internally when asserted low.
$\overline{\text{TXOFF}}$	This TTL input forces the NRZ buffer to a quiet state when asserted low.
RTSET1, RTSET2	An external 1% resistor connected between these pins controls the transmitter output current amplitude. I_{OUT} = 64 x 1.25V/RTSET
TVCCA, TVCCD	Separate analog and digital transmitter power supply pins help to isolate sensitive circuitry from noise generating digital functions. Both supplies are nominally +5 volts.
TGNDA, TGNDD	Analog and digital transmitter grounds provide separate return paths for clean and noisy signals.
SD+, SD–	These differential ECL100K compatible outputs indicate the presence of a data signal with an amplitude exceeding a preset threshold.
TPIN+, TPIN–	NRZ encoded data from the receiver filter/ transformer module enters the Receiver through these pins.

NAME	FUNCTION
RXOUT+, RXOUT–	Differential ECL100K compatible outputs provide NRZ encoded data to the PHY.
CAP1, CAP2	Two external capacitors connected to these pins sets the time constant for the adaptation in the equalizer loop as well as for signal detect response.
RRSET1, RRSET2	Internal time constants controlling the equalizer's transfer function are set by an external resistor connected across these pins.
CMREF	This pin provides a DC common mode reference point for the receiver inputs.
RVCCA, RVCCD	Analog and digital supply pins are separated to isolate clean and noisy circuit functions. Both supplies are nominally +5 volts.
RGND	Receiver ground.
RSET1, RSET2	An external 5kΩ resistor across these pins sets up an internal reference current.
RTH1, RTH2	An external resistor connected across these pins sets the internal levels for equalization as well as signal detect. This resistor allows compensation for transmit and magnetics variations. RTH should be set to match the peak-to-peak transmit amplitude. V_{AMP} = 16 x 1.25 x RTH/RSET where V_{AMP} is the peak-to-peak amplitude of the transmit output with zero length cable.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VCC Supply Voltage Range ..... GND –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... GND –0.3V to VCC + 0.3
Output Current
  TPOUT+/TPOUT–, SD±, RXOUT± 50mA
  All other outputs 10mA
Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θJA)
  PLCC ..... 60°C/W
  TQFP ..... 80°CW

OPERATING CONDITIONS

VCC Supply Voltage ..... 5V ± 5%
T_A, Ambient Temperature ..... 0°C to +70°C
RTSET ..... 4KΩ ± 1%
RRSET ..... 9.53KΩ ± 1%
RSET ..... 5KΩ ± 1%
RTH ..... 250Ω ± 1%
CAP1, CAP2 ..... 1.0µF + 5%
Receive transformer insertion loss ..... < –0.5dB

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, VCC = 5V ±5%, RTSET = 4.0Ký, RTH = 250ý.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics					
Supply Current					
RVCCD			67		mA
RVCCA			52		mA
TVCCD			25		mA
TVCCA			6		mA
RVCCD + RVCCA + TVCCD + TVCCA				170	mA
TTL Inputs ($\overline{TXOFF}$, $\overline{LPBK}$)					
V_{IL} Input Low Voltage				0.8	V
V_{IH} Input High Voltage		2.0			V
Differential Inputs (TPIN±, TXIN±)					
TPIN+, TPIN– Common Mode Input Voltage		2.2		V_{CC}	V
TPIN+, TPIN– Differential Input Voltage				1.5	V
TPIN+, TPIN– Differential Input Resistance		10			κΩ
TPIN+, TPIN– Common Mode Input Current				+10	uA
TXIN+, TXIN– Input Voltage HIGH (V_{IH})		V_{CC}–1.165		V_{CC}–0.88	V
TXIN+, TXIN– Input Voltage LOW (V_{IL})		V_{CC}–1.810		V_{CC}–1.475	V
TXIN+, TXIN– Input Current LOW (I_{IL})		0.5			uA
TXIN+, TXIN– Input Current HIGH (I_{IH})				50	uA
Differential Outputs (SD±, RXOUT±, TPOUT±)					
SD+, SD–, RXOUT+, RXOUT– Output Voltage HIGH (V_{OH})	Note 5	V_{CC}–1.025		V_{CC}–0.88	V
SD+, SD–, RXOUT+, RXOUT– Output Voltage LOW (V_{OL})	Note 5	V_{CC}–1.81		V_{CC}–1.62	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Outputs (SD±, RXOUT±, TPOUT±) (Continued)					
TPOUT+, TPOUT– Differential Output Current HIGH	$V_{OUT} = V_{CC} \pm 0.5$, Note 4	19.0		21.0	mA
TPOUT+, TPOUT– DifferentialOutput Current LOW	$V_{OUT} = V_{CC} \pm 0.5$, Note 4	0		0.1	mA
TPOUT+, TPOUT– Output Current Offset	Note 3			0.5	mA
TPOUT+, TPOUT–$V_{OUT} = V_{CC}$ Output Amplitude Error	Note 3, 4	–5.0		5.0	%
TPOUT+, TPOUT–$V_{OUT} = V_{CC} \pm 1.1V$ Output Voltage Compliance		–2.0		+2.0	%
AC Characteristics					
TPOUT+, TPOUT– Rise/Fall Time	Note 2	1.5	2.0	2.5	ns
TPOUT+, TPOUT– Output Jitter	Note 2		0.5		ns
RXOUT+, RXOUT– Rise/Fall Time	Note 2			5	ns
RXOUT+, RXOUT– Output Jitter	Note 2		2.0		ns

Note 1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 3. Low Duty cycle pulse testing is performed at T_A.
Note 4. Output current amplitude is determined by $I_{OUT} = 64 \times 1.25V/RTSET$.
Note 5. Output voltage levels are specified when terminated by 50Ω to V_{CC}-2V or equivalent load.

FUNCTIONAL DESCRIPTION

The ML6672 transceiver is a physical media dependent transceiver that allows the transmission and reception of 155 Mbps data over shielded twisted pair cable or category 5 unshielded twisted pair cable.

The transmit section accepts NRZ data, sending the information on a two pin current driven transmitter. The transmitted output passes through an external low pass filter and transformer before entering the connectors to the STP or UTP cable. The output amplitude of the transmitted signal is programmable through the external RTSET resistor.

The receive section accepts NRZ coded data after it passes through an isolation transformer and band limiting filter. The adaptive equalizer is used to compensate for the amplitude and phase distortion incurred from the cable. The adaptive control section determines the cable length and adjusts the equalizer accordingly. As the input signal amplitude diminishes, the amount of equalization increases until it reaches its maximum of an equivalent 100 meters of category 5 cable. A parallel 10pF capacitor can be connected between TPIN+ and TPIN– to improve Bit Error Rate.

The adaptive control block governs both the equalization level as well as the link detection status. The link detection threshold has a fixed relationship to the overall equalization level which is currently 25% of the transmitted amplitude. For the link status to be true, a minimum level signal must be received. When the input signal is small, the equalization will be at its maximum.

After the signal has been equalized, it is fed through the loopback multiplexer onto the RXOUT± pins.

Figure 1 shows a typical gain vs frequency plot of the adaptive equalizer for 0, 25, 50, 75 and 100 meter category 5 cable lengths.

TRANSMISSION

PECL level scrambled NRZ data is received by the ML6672 and the current driven transmitter then sent the data to the filter/transformer module. The transmit amplitude is controlled by one external resistor, RTSET.

$$I_{OUT} = \frac{64 \times 1.25V}{RTSET}$$

For ATM UTP applications the transmit amplitude is 1V peak to peak. The termination at the transmitter output is 50Ω. Therefore the transmit current I_{OUT} = 1/50 = 20 mA.

Therefore, RTSET = (64 x 1.25/20)kΩ = 4kΩ

The transmitter may be disabled via the TXOFF pin. When this pin is pulled low, the transmitter's output goes to its center value (I_{OUT}/2) with no differential current flowing through the transformer.

ADAPTIVE EQUALIZATION

During transmission of data over UTP (unshielded twisted pair), distortion and ISI are caused by dispersion in the cable. Equalization is used to overcome this signal corruption. However, the distortion is frequency dependent and loop length dependent. Therefore, in most practical cases, the TP port characteristic is unknown and it is impractical to tune the equalizer specifically to each individual port. Hence, adaptive equalizer is used in the TP-PMD to ensue proper compensation of the received signal.

By using adaptive equalizer, the receiver automatically compensate different length of cable without over equalizing or under equalizing the line. The ML6672 monitors the energy of the received signal to determine the cable length and adjust the equalizer accordingly. The input signal level is inversely proportional to the cable length. Therefore, as the signal level decreases, the amount of equalization is increased to compensate for the line loss.

RECEIVE CIRCUIT

After the data is received and equalized, it is then sent to the clock recovery circuit via the RXOUT pins. A resistor RTH is used to control the internal level of equalization.

$$V_{AMP} = \frac{16 \times 1.25 \times RTH}{RSET}$$

VAMP is the transmit voltage amplitude and is equal to 1V and RSET = 5kΩ. Therefore, RTH = 1 x 5/(16 x 1.25) kΩ = 250Ω.

CAP1 and CAP2 are capacitors used to set the time constant for adaptation of the equalizer loop and should be 0.33µF.

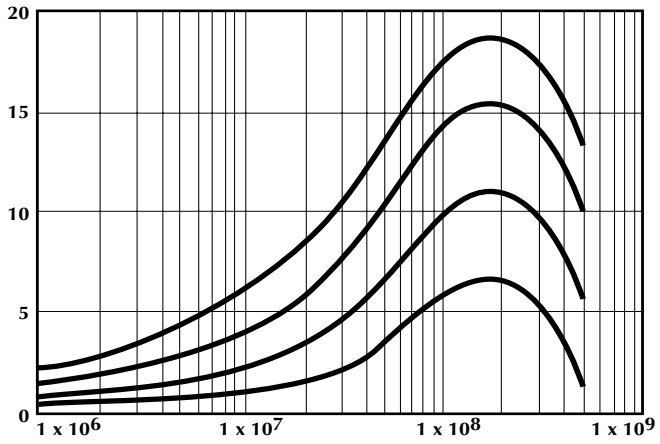


Figure 1. Equalization Range

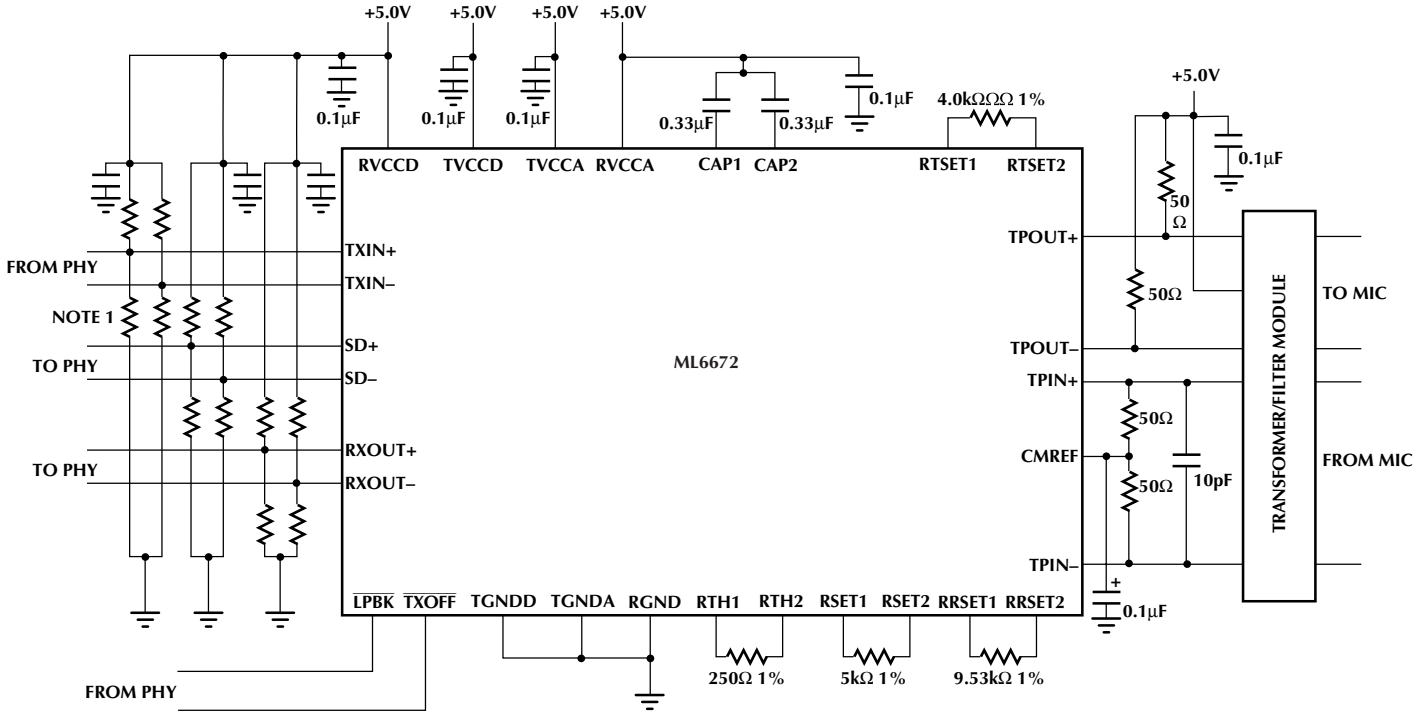
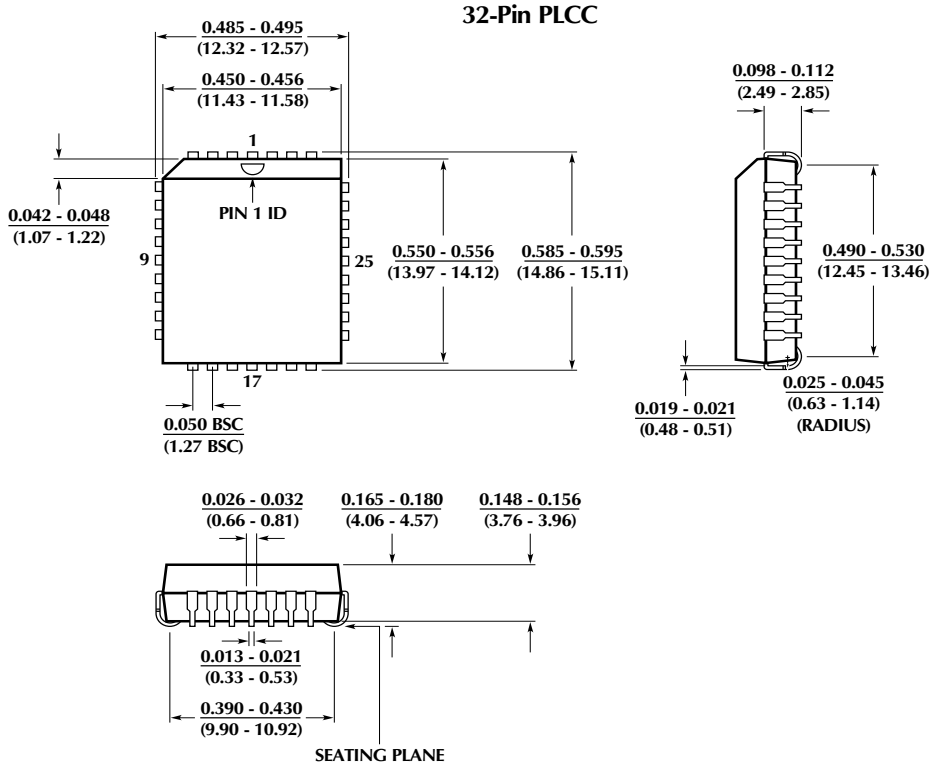


Figure 2. Application Example of ML6672 Configured for 1.0V_{P-P} Transmit Amplitude on C5 UTP.

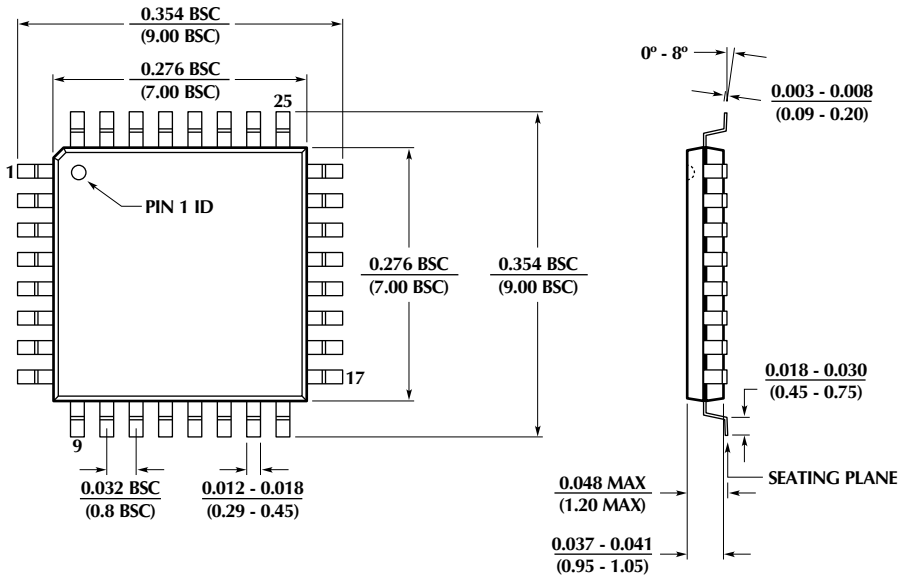
Note 1. Split 100K ECL terminations are 82Ω and 130Ω to VCC and GND respectively.
Note 2. Recommended power supply bypass capacitors are 0.1µF with optional 10µF tantalum in parallel.
Note 3. Transformer turns ratio is 1:1.
Note 4. LPBK and TXOFF inputs are active LOW.

PHYSICAL DIMENSIONS inches (millimeters)

Package: Q32
32-Pin PLCC



Package: H32-7
32-Pin (7 x 7 x 1mm) TQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6672CQ (EOL)	0°C to 70°C	32-Pin Leaded PLCC (Q32)
ML6672CH (EOL)	0°C to 70°C	32-Pin TQFP (H32-7)

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