January 29, 1998

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1650 is a high performance inverting DC-DC converter, designed to drive an external power switch to generate programmable negative voltages. In the particularly suitable LCD bias contrast application, maximum efficiency of 90% can be achieved with low cost PNP bipolar transistor drivers. The 4V to 24V input operation range allows the SC1650 to be powered directly by the battery pack in most battery-operated applications for greater efficiency. The output voltage can be scaled to -40V by two external resistors. A pulse frequency modulation scheme is employed to maintain high efficiency conversion under wide input voltage ranges. Quiescent current is about 100µA and can be reduced to 8µA in shutdown mode. With a switching frequency range of 100kHz to 320kHz, small size switching components may be used, which is ideal for battery powered portable equipment such as notebook and palmtop computers.

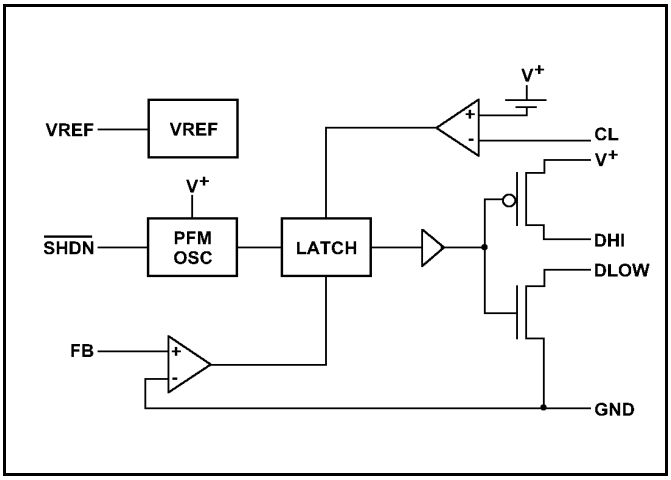
FEATURES

- 4V to 24V input voltage operation
- Adjustable output voltage up to -40V
- Low quiescent current at 100µA
- Pulse frequency modulation maintains high efficiency (max 90%)
- 100kHz to 320kHz switching frequency
- Power-Saving shutdown mode (8µA typical)
- High efficiency with low cost external PNP bipolar transistor

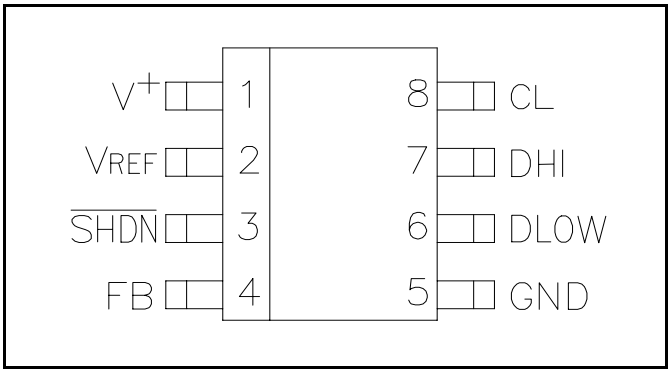
APPLICATIONS

- Negative LCD contrast bias for
  1. Notebook & palmtop computers
  2. Pen-based data systems
  3. Portable data collection terminals
  4. Personal digital assistants
- Negative voltage supplies

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE(1)	V_{OUT}	PACKAGE
SC1650CS	Adj	SO-8

Note:
(1) Add suffix 'TR' for tape and reel.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Supply Voltage	V^+	24	V
$\overline{SHDN}$ Voltage	$V_{\overline{SHDN}}$	15	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{STG}	-65 to 125	°C

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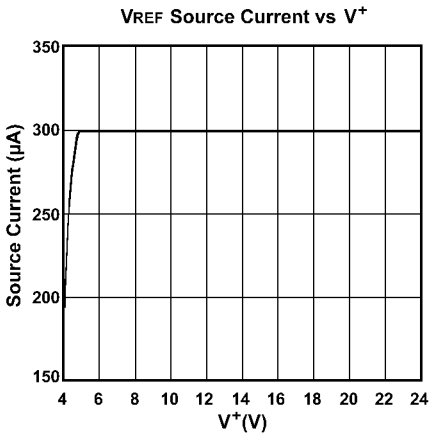
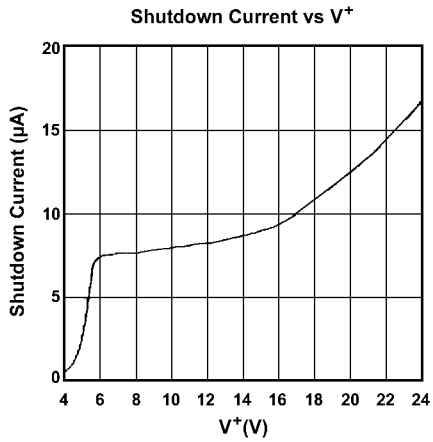
ELECTRICAL CHARACTERISTICS

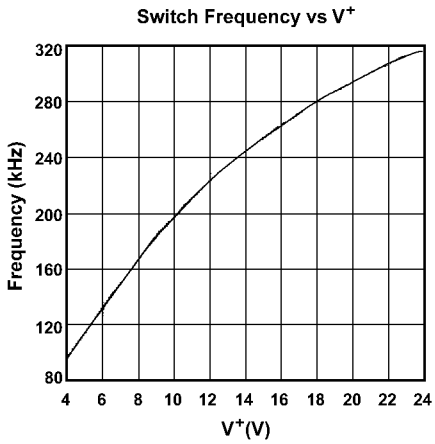
Unless otherwise specified, T_A = 25°C, V^+ = 13V

	Test Conditions	Test Limits			
Parameter		**Min**	**Typ**	**Max**	**Units**
Input Voltage		4		24	V
Switch Off Current	V_{FB} = -50mV		100	200	µA
Shutdown Mode Current			8	20	µA
V_{REF} Voltage	I_{SOURCE}=250µA	1.16	1.22	1.28	V
V_{REF} Source Current		250			µA
DLOW "ON Resistance"			15		Ω
DHI "ON Resisance"			10		Ω
CL Threshold		45	60	75	mV
Shutdown Threshold		0.8	1.5	2.4	V

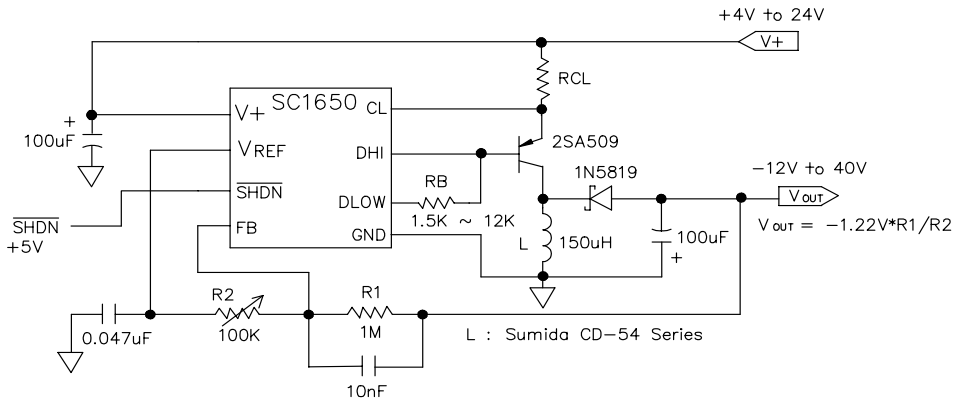
TYPICAL PERFORMANCE CHARACTERISTICS







TYPICAL APPLICATION CIRCUIT



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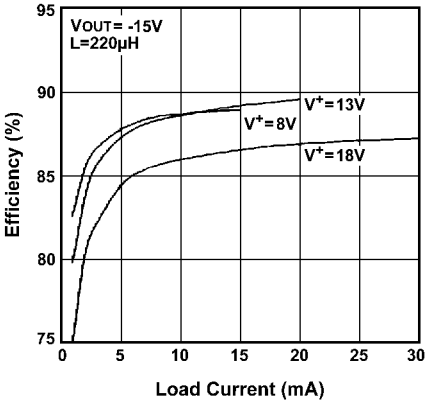
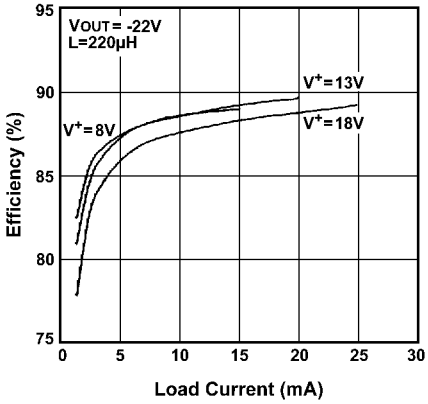
TYPICAL APPLICATION INFORMATION

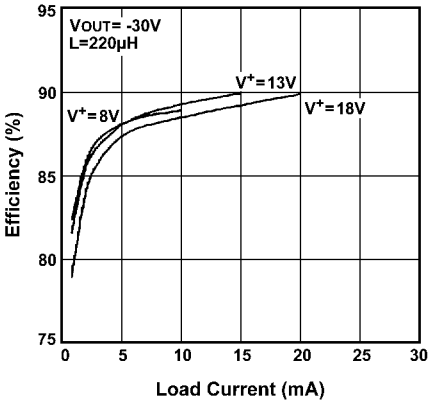
Efficiency vs Load Current



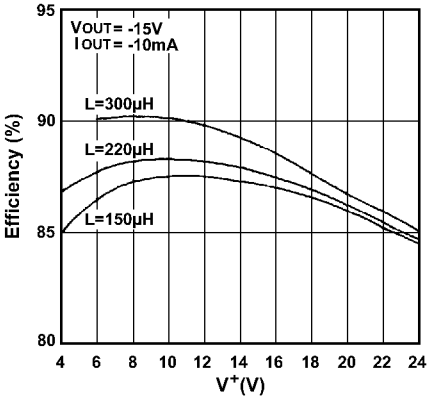
Efficiency vs Load Current



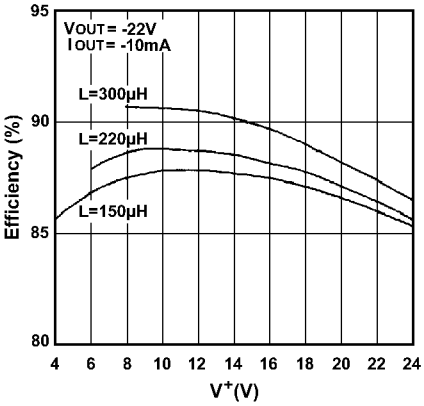
Efficiency vs Load Current



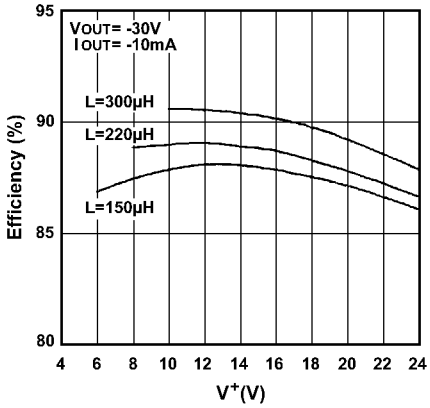
Efficiency vs V+



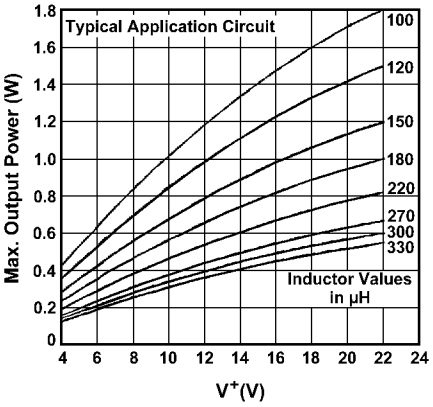
Efficiency vs V+



Efficiency vs V+



Max. Output Power vs V+



The typical application circuit generates an adjustable negative voltage for contrast bias of LCD displays. Efficiency and output power can be optimized by using the appropriate inductor and switch. The following formulas provide a guideline for determing the optimal component val-

$$L = \left(11.1 - 0.15 \times V^{+}\right) \times \frac{V^{+}}{\left|I_{OUT}\right| \times \left|V_{OUT}\right|}$$

PNP : $\left|V_{CEO}\right| > V^{+} + \left|V_{OUT}\right|$

$$\left|I_{C(MAX)}\right| \geq 200 \times \frac{\left|I_{OUT}\right|}{V^{+}}$$

$$\left|V_{CE(SAT)}\right| < 0.4V \text{ at } I_C = 200 \times \frac{I_{OUT}}{V^{+}} \text{ and } \beta = 10$$

$R_B \cong 3 \times L \times \left(V^{+} - 0.8\right)$, where units : V^{+} in Volt, V_{OUT} in Volt, I_{OUT} in Ampere, L in µH, R_B in Ohm.

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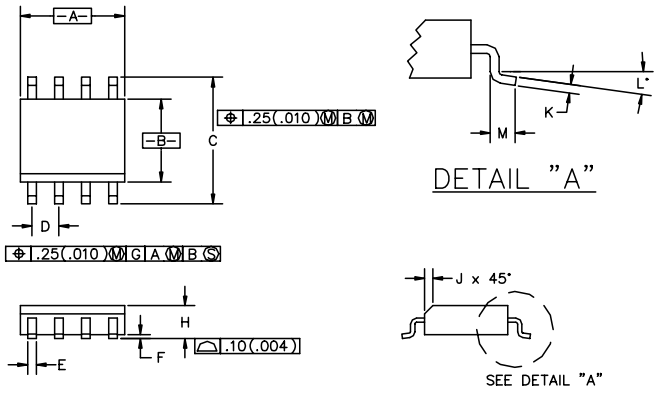
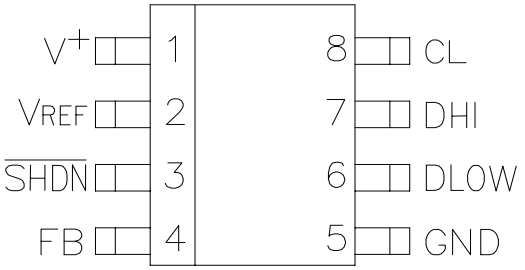
OUTLINE DRAWING - SO-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN 1: V^+ 4V to 24V input supply voltage.

PIN 2: V_{REF} 1.22V reference output. Bypass with a 0.047µF capacitor to GND. Sourcing capability is guaranteed to be greater than 250µA.

PIN 3: $\overline{SHDN}$ Logic input to shutdown the chip.
>1.5V = normal operation,
GND = shutdown
In shutdown mode DLOW and DHI pins are high.

PIN 4: FB Feedback signal input to comparator. Connecting a resistance R1 to V_{OUT} and a resistance R2 to V_{REF} yields the output voltage:

$$V_{OUT} = -\frac{R1}{R2} * V_{REF}$$

PIN 5: GND Power ground.

PIN 6: DLOW Driver sinking output. Connected to DHI when using an external P-channel MOSFET. When using an external PNP bipolar transistor, connect a resistor R_B from this pin to DHI. R_B value depends upon V^+, inductor value and the PNP bipolar transistor. By adjusting the R_B value, efficiency can be optimized.

PIN 7: DHI Driver sourcing output. Connect to the gate of the external P-channel MOSFET or base of the PNP bipolar transistor.

PIN 8: CL Current-limit input. This pin clamps the switch peak current under abnormal conditions.