MOTOROLA
Semiconductor Technical Data

Order Number: MC33989/D
Rev. 4.1, 08/2001

Advance Information

System Basis Chip With High Speed CAN Transceiver

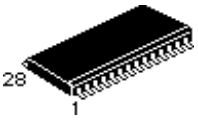
MC33989

SYSTEM BASIS CHIP WITH HIGH SPEED CAN

SEMICONDUCTOR TECHNICAL DATA

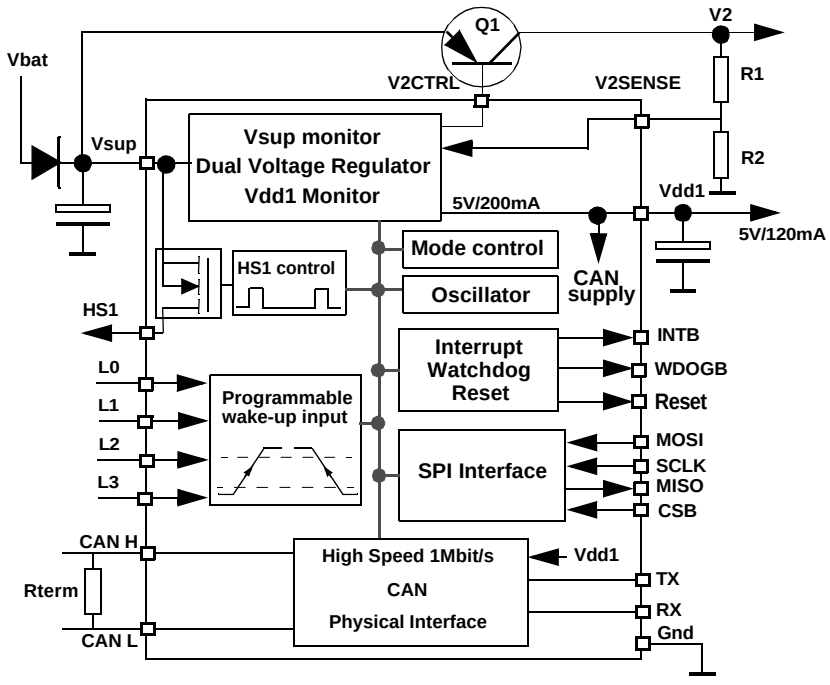
The MC33989 is a monolithic integrated circuit combining many functions frequently used by automotive ECUs. It incorporates:
- Two voltage regulators.
- Four high voltage inputs.
- 1Mbaud CAN physical interface.

• Vdd1: Low drop voltage regulator, current limitation, over temperature detection, monitoring and reset function
• Vdd1: Total current capability 200mA (including CAN current, 120mA for MCU and external peripheral components)
• V2: control circuitry for external bipolar ballast transistor for high flexibility in choice of peripheral voltage and current supply.
• Four operational modes (normal, stand-by, stop and sleep mode)
• Low stand-by current consumption in stop and sleep modes
• High speed 1MBaud CAN physical interface.
• Four external high voltage wake-up inputs, associated with HS1 Vbat switch
• 150mA output current capability for HS1 Vbat switch allowing drive of external switches pull up resistors or relays
• Vsup failure detection
• Nominal DC operating voltage from 5.5 to 27V, extended range down to 4.5V.
• 40V maximum transient voltage
• Programmable software time out and window watchdog
• Safe mode with separate outputs for Watchdog time out and Reset
• Wake up capabilities (four wake up inputs, programmable cyclic sense, forced wake up, CAN interface and SPI)
• Interface with MCU through SPI

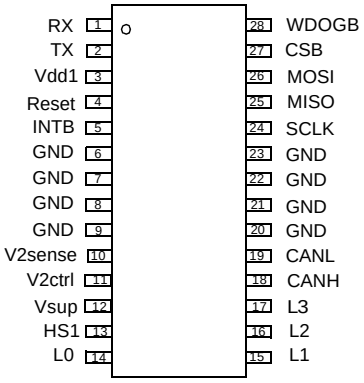


DW SUFFIX
PLASTIC PACKAGE
CASE
SO-28

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION		
Device	Operating Temperature Range	Package
None	T_A = -40 to 125°C	SO-28

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA digital dna™

1 MAXIMUM RATINGS

Ratings	Symbol	Min	Typ	Max	Unit
ELECTRICAL RATINGS					
Supply Voltage at Vsup - Continuous voltage - Transient voltage (Load dump)	 Vsup Vsup	 -0.3		 27 40	V
Logic Inputs (Rx, Tx, MOSI, MISO, CSB, SCLK, Reset, WDOGB, INTB)	Vlog	- 0.3		Vdd1+0.3	V
Output current Vdd1	I		Internally limited		A
HS1 - voltage - output current	 V I	 -0.3	 Internally limited	Vsup+0.3	 V A
ESD voltage (HBM 100pF, 1.5k) - CANL, CANH, HS1, L0, L1, L2, L3 - All other pins	Vesdh	 -4 -2		 4 2	kV
ESD voltage (Machine Model) All pins	Vesdm	200		200	V
L0, L1,L2, L3 - DC Input voltage - DC Input current - Transient input current (according to ISO7637 specification) and with external component tbd.	Vwu DC	 -0.3 -2 tbd		 40 2 tbd	 V mA mA
THERMAL RATINGS					
Junction Temperature	T_j	- 40		+150	°C
Storage Temperature	T_s	- 55		+165	°C
Ambient Temperature (for info only)	T_a	- 40		+125	°C
Thermal resistance junction pin	Rthj/p			20	°C/W

2 ELECTRICAL CHARACTERISTICS

(V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C)
For all pins except CANH, CANL, Tx and Rx which are described in the CAN module section

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Vsup pin (Device power supply)						
Nominal DC Voltage range	Vsup	5.5		18	V	
Extended DC Voltage range 1	Vsup-ex1	4.5		5.5	V	Reduced functionality (note 1)
Extended DC Voltage range 2	Vsup-ex2	18		27	V	(note 3)
Input Voltage during Load Dump	VsupLD			40	V	Load dump situation
Input Voltage during jump start	VsupJS			27	V	Jump start situation
Supply Current in Stand-by Mode (note 2,4)	Isup(stdby)			15	mA	Iout at Vdd1 =10mA, CAN recessive state or disabled
Supply Current in Normal Mode (note 2)	Isup(norm)			15	mA	Iout at Vdd1 =10mA, CAN recessive state or disabled
Supply Current in Sleep Mode (note 2,4)	Isup (sleep1)		45	65	µA	Vdd1 & V2 off, Vsup<12V, oscillator running (note5) CAN module disabled
Supply Current in Sleep Mode (note 2,4)	Isup (sleep2)		25	40	µA	Vdd1 & V2 off, Vsup<12V oscillator not running (5) CAN module disabled,
Supply current in sleep mode (note 2,4)	Isup (sleep3)			150	µA	Vdd1 & V2 off, Vsup>12V oscillator running (5) CAN module disabled
Supply Current in Stop mode (note 2,4) I out Vdd1 <2mA	Isup (stop1)			85	µA	Vdd1 on, Vsup<12V oscillator running (5) CAN module disabled,
Supply Current in Stop mode (note 2,4) Iout Vdd1 < 2mA	Isup (stop2)			60	µA	Vdd1 on, Vsup<12V oscillator not running (5) CAN module disabled
Supply Current in Stop mode (note 2,4) Iout Vdd1 < 2mA	Isup (stop3)			180	µA	Vdd on, Vsup>12 oscillator running (5) CAN module disabled
Supply Fail Flag internal threshold	Vthresh	1.5	3	4	V	
Supply Fail Flag hysteresis	Vdet hyst		1		V	

Note 1: Vdd1>4V, reset high, logic pin high level reduced, device is functional.

Note 2: current measured at Vsup pin.

Note 3: Device is fully functional. All functions are operating (All mode available and operating, Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0 to L3 inputs operating, SPI read write operation). Over temperature may occur.

Note 4: With CAN cell disabled. If CAN cell is enabled for wake up, an additional 100uA must be added to specified value.

Note 5: Oscillator running means “Forced Wake up” or “Cyclic Sense” or “Software Watchdog in stop mode” timer activated. Oscillator not running means that “Forced Wake up” and “cyclic Sense” and “Software Watchdog in stop mode” are not activated.

Vdd1 (external 5V output for MCU supply and internal CAN physical interface supply).
Idd1 is the total regulator output current. Iddcan is the internal CAN block supply current. Iout is Vdd1 external output current. Idd1 = Iddcan + Iout.
Vdd specification with external capacitor C>1uF and ESR<1O ohm. No tantalum capacitor required.

Vdd1 Output Voltage	Vdd1out	4,9	5	5,1	V	Idd1 from 2 to 200mA 5.5V< Vsup <27V
Vdd1 Output Voltage	Vdd1out	4			V	Idd1 from 2 to 200mA 4.5V< Vsup <5.5V
Drop Voltage Vsup>Vddout	Vdd1drop		0.2	0,5	V	Idd1 = 200mA
Idd1 Current (Idd1 = Iddcan + Iout)	Idd1	200	270	350	mA	Internally limited Included Internal CAN current consumption
Vdd1 Output Voltage in stop mode	Vddstop	4,75	5,00	5,25	V	Iout<=2mA
Thermal Shutdown	Tsd	160		190	°C	
Over temperature pre warning	Tpw	130		160	°C	VDDTEMP bit set

(V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C)
For all pins except CANH, CANL, Tx and Rx which are described in the CAN module section

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Temperature Threshold difference	Tsd-Tpw	20		40	°C	
Reset threshold 1	Rst-th1	4.3	4.5 V	4.7		Selectable by SPI. Default value after reset.
Reset threshold 2	Rst-th2	3.6	3.8	4		Selectable by SPI
Reset duration	reset-dur	1		2	ms	
Vdd1 range for Reset Active	Vdd_r	1			V	
Reset Delay Time	t_d	5		20	µs	
Line Regulation	LR1		5	25	mV	9V<V_{sup}<18, I_{dd}=10mA
Line Regulation	LR2		10	25	mV	5.5V<V_{sup}<27V, I_{dd}=10mA
Load Regulation	LD		20	50	mV	1mA<I_{Idd}<200mA
Thermal stability	ThermS		5		mV	Vsup=13.5V, I=100mA

V2 adjustable output voltage regulator

Note 3: V2 specification with external capacitor

- option 1: C>22uF and ESR<1O ohm, (no tantalum capacitor required)
- option2: C>1uF and ESR<10 ohm, (no tantalum capacitor required). In this case depending upon ballast transistor gain an additional resistor and capacitor network between emitter and base of PNP ballast transistor might be required (ex C=10nF).

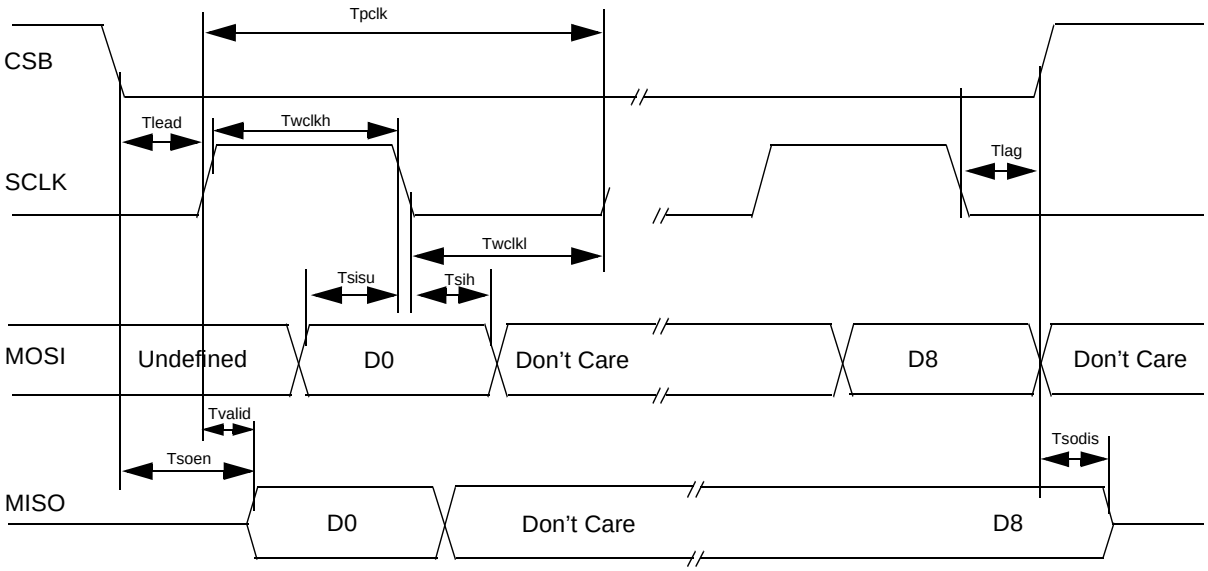
Note 4: Subject to external R1 and R2 resistors tolerances.

V2 Output Voltage (note 4)	V2	4,9	5	5,1	V	I2 from 2 to 200mA 5.5V< Vsup <27V
I2 output current (for information only)	I2	200			mA	Depending upon external ballast transistor
V2 sense reference voltage	V2sref		1.25		V	
V2 ctrl drive current	I2ctrl		10		mA	
V2 ctrl Output voltage range	V2ctrl	1.8		8	V	(Vsup>V2ctrl+1V)
Vdd2 to Vdd1 matching (note 4)	Vmatch	0.5		0.5	%	excluding external component matching
Logic output pins (MISO)						
Low Level Output Voltage	Vol			1.0	V	I out = 1.5mA
High Level Output Voltage	Voh	Vdd1-0.9			V	I out = -250uA
Tristated MISO Leakage Current		-2		+2	µA	0V<V_{miso}<Vdd
Logic input pins (MOSI, SCLK, CSB)						
High Level Input Voltage	Vih	0.7Vdd1		Vdd1+0.3		
Low Level Input Voltage	Vil	-0.3		0.3Vdd1	V	
High Level Input Current on CSB	Iih	-20		-100	µA	V_i=4V
Low Level Input Current CSB	Iil	-20		-100	µA	V_i=1V
MOSI, SCK Input Current	Iin	-10		10	µA	0<V_{IN}<Vdd
Reset Pin (output pin only)						
High Level Output current	Iol		-30		µA	0<V_{out}<0.7Vdd
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	1v<V_{sup}<27V
Reset pull down current	Ipdw	3		5	mA	
Reset Duration after Vdd1 High	reset-dur	1		2	ms	
Wdogb output pin						
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	1v<V_{sup}<27V
High Level Output Voltage (I_0=-250uA)	Voh	Vdd1-0.9				
INT Pin						
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	
High Level Output Voltage (I_0=-250uA)	Voh	Vdd1-0.9				
HS1: 150mA High side output pin						

(V_{sup} From 5.5V to 18V and T_j from -40°C to 150°C)
For all pins except CANH, CANL, Tx and Rx which are described in the CAN module section

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Rdson at Tj=25°C, and Iout -150mA	Ron25			2.5	Ohms	Vsup>9V
Rdson at Tj=150°C, and Iout -150mA	Ron150			5	Ohms	Vsup>9V
Rdson at Tj=150°C, and Iout -120mA	Ron150-2		4		Ohms	5.5<Vsup>9V
Output current limitation	Ilim	200		500	mA	
Over temperature Shutdown	Ovt	155		190	°C	
Leakage current	Ileak			10	uA	
Output Clamp Voltage at Iout= -10mA	Vcl	-0.5		-2	V	no inductive load drive capability
Cyclic sense period (refer to SPI)	Toff				ms	in sleep and stop modes
Cyclic sense On time (refer to SPI)	Ton		300		us	in sleep and stop modes
Timing accuracy	Tacc	-30		+30	%	in sleep and stop mode
L0, L1, L2, L3 inputs						
Negative Switching Threshold	Vthn	2.5 tbd	3 3	3.5 tbd	V	5.5V<Vsup<18V 18V<Vsup<27
Positive Switching Threshold	Vthp	3 tbd	3.7 3.7	4.5 tbd	V	5.5V<Vsup<18V 18V<Vsup<27
Hysteresis	Vhyst	0.7 tbd		1.3 tbd	V	5.5V<Vsup<18V 18V<Vsup<27
Input current	Iin	-10		10	uA	-0.3V < Vin < 40V
Wake up Filter Time		8	20	38	µs	
DIGITAL INTERFACE TIMING						
SPI operation frequency	Freq			4	MHz	
SCLK Clock Period	t_{pCLK}	250			ns	
SCLK Clock High Time	t_{wSCLKH}	125			ns	
SCLK Clock Low Time	t_{wSCLKL}	125			ns	
Falling Edge of CS to Rising Edge of SCLK	t_{lead}	100	50		ns	
Falling Edge of SCLK to Rising Edge of CS	t_{lag}	100	50		ns	
MOSI to Falling Edge of SCLK	t_{SISU}	40	25		ns	
Falling Edge of SCLK to MOSI	t_{SIH}	40	25		ns	
MISO Rise Time (CL = 220pF)	t_{rSO}		25	50	ns	
MISO Fall Time (CL = 220pF)	t_{fSO}		25	50	ns	
Time from Falling or Rising Edges of CS to: - MISO Low Impedance - MISO High Impedance	 t_{SOEN} t_{SODIS}			 50 50	ns	
Time from Rising Edge of SCLK to MISO Data Valid	t_{valid}			50		0.2 V1≤SO≥ 0.8V1, C_L=200pF

Figure 1. SPI Timing characteristics



3 CAN MODULE SPECIFICATION

MAXIMUM RATING

Ratings	Symbol	Min	Typ	Max	Unit
ELECTRICAL RATINGS					
CANL,CANH Continuous voltage	VcanH,L	-27		40	V
CANH, CANL Transient voltage (Load dump, note1)	VtrH,L			40	V
CANH, CANL Transient voltage (note2)	VtrH,L	-40		40	V
Logic Inputs (Tx, Rx)	U	- 0.5		6	V

ELECTRICAL CHARACTERISTICS V_{DD1} = 4,75 to 5,25; V_{sup}=5.5 to 27V; T_j = -40 to 150°C unless otherwise specified

Descriptions	Symbol	Min	Typ	Max	Unit	Conditions
Supply						
Supply current of CAN cell	Ires			15	mA	Recessive state
Supply current of CAN cell	Idom			75	mA	Dominant state
Supply current of CAN cell (CAN cell in Sleep state)	Isleep			100	uA	CAN cell in sleep state
CANH and CANL						
Bus pins common mode voltage		-2		7	V	
Differential input voltage	Vcanh-Vcanl			500	mV	Recessive state at Rx
Differential input voltage		900			mV	Dominant state at Rx
Differential input hysteresis (Rx)		100			mV	
Input resistance	Rin	5		100	Kohms	
Differential input resistance	Rind	10		100	Kohms	
Unpowered node input current				1.5	mA	
CANH output voltage		2.75		4.5	V	TX dominant state
CANL output voltage		0.5		2.25	V	Tx dominant state
Differential output voltage		1.5		3	V	Tx dominant state
CANH output voltage				3	V	Tx recessive state
CANL output voltage		2			V	Tx recessive state
Differential output voltage				100	mV	Tx recessive state
Output current at CANH	Icanh	-35		-100	mA	Dominant state
Output current at CANL	Icanl	35		150	mA	Dominant state
Over temperature shutdown	Tshut	160			°C	
TX and RX						
Tx Input High Voltage	Vih	0.7 Vdd		Vdd+0.4	V	
Tx Input Low Voltage	Vilp	-0.4		0.3 Vdd	V	

Descriptions	Symbol	Min	Typ	Max	Unit	Conditions
Tx High Level Input Current, Vtx=Vdd	Iih	-10		10	uA	
Tx Low Level Input Current, Vtx=0	Iil	-300		-100	uA	
Rx Output Voltage High, Irx=-250uA	Voh	Vdd-1			V	
Rx Output Voltage Low, Irx=+1mA	Vol			0.5	V	
Timing						
Dominant State Timeout	Tdout	140			us	
Propagation loop delay Tx to Rx	Tlrd			150	ns	
Propagation delay Tx to CAN	Ttrd			110	ns	
Propagation delay CAN to Rx	Trrd			60	ns	
Propagation loop delay Tx to Rx	Tldr			150	ns	
Propagation delay Tx to CAN	Ttdr			130	ns	
Propagation delay CAN to Rx	Trdr			60	ns	

note 1: Load dump test according to ISO7637 part 1
note 2: Transient test according to ISO7637 part 1, pulses 1,2,3a and 3b
note 3: Human Body Model; C=100pF, R=1.5Kohms
note 4: Machine Model; C=200pF, R=25ohms

Figure 2. Transceiver AC characteristics

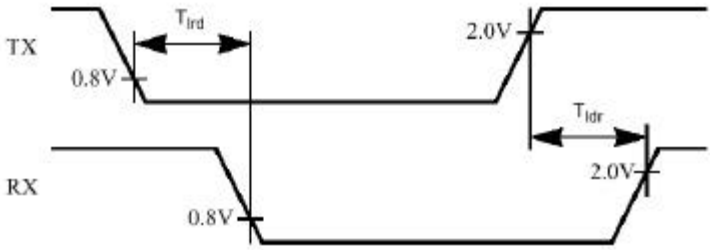
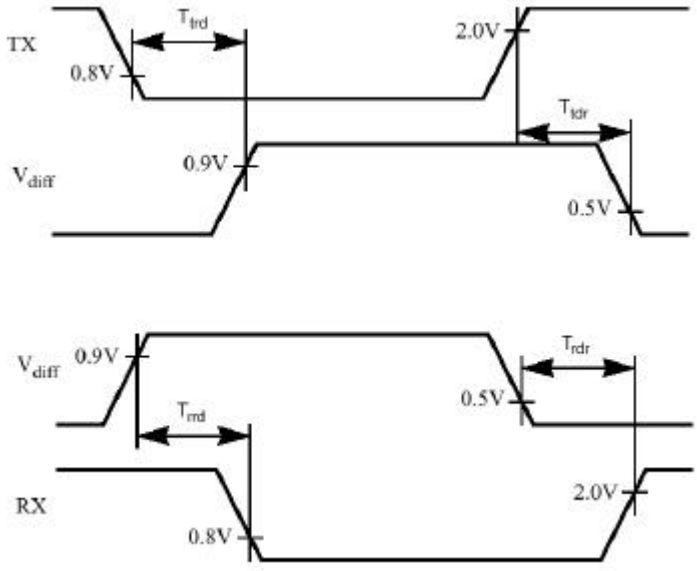


Figure 3. Transceiver AC characteristics



DEVICE DESCRIPTION

3.1 CAN error detection and wake up

3.1.1 Dominant State Time-out

This protection is based on the fact that all CAN signals can not have more than five bits in a row with the same state. In case of a condition the Tx pin is stuck at 0v, the transceiver would hold the bus in dominant state making it impossible to the others CAN modules to use the bus. The protection acts releasing the bus when a dominant signal with more than 140uS is present in the Tx signal. After entering the fault condition the driver is disabled. To clear this disabled state the CAN transceiver needs to have its input going to recessive state.

3.1.2 Internal Error output flags

There are internal error flags to signals when an error occurs. The flags are enabled when one of the below condition happens:

- Thermal protection activated.
- Over Current detection in CANL or CANH pins.
- Time-out condition for dominant state.

3.1.3 Standby mode & Wake-up via CAN bus feature

The HSCAN interface enters in a low consumption mode when the CAN standby mode s enable (stand-by mode). In this mode the HSCAN module will have a 100uA consumption via internal 5V.

When in stand-by mode the transmitter and the normal receiver are disable, the only part of circuit which remains working is the wake up module. This module has a receiver to check the bus lines and according to its activity generate a wake up output

signal. The conditions for the wake is meet when there are 3 valid pulses in a row. A valid signal must have a pulse width bigger than 0.5uS and no more than 0.5mS.

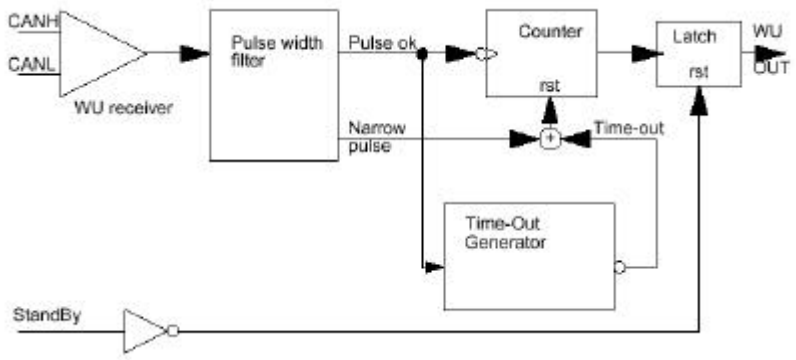


Figure 4. Wake up block diagram

The block diagram shows how the wake up signal is generated. First the CAN signal is detected by a low consumption receiver (WU receiver). The signal pass through a pulse width filter to validate the signal.

The signal pass through a pulse width filter in order to select or discard the input signal according to its width. If the pulse width is greater than 500uS the signal pass to the “pulse ok” node with 0.5uS of delay. If the width of pulse is less than 0.5uS no signal appears on “pulse ok” node and a pulse appears in “Narrow pulse” node. A narrow pulse will reset the counter.

The time-out generator block act as a retriggerable mono stable, when the first signal appears it causes a low signal output disabling the counter reset and beginning to count, if the next CAN signal do not occurs within 0.5mS the time out node will reset the counter. After the counter reach the number 3 the Wake up output is latched until the standby signal be disabled. The wake up output do not takes the CAN out of stand-by mode. In order to do this an external circuit should change the standby input signal.

4 GENERAL DESCRIPTION

The MC33989 is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 200mA total output current capability. Available output current is 120mA at Vdd1 external pin.
- Driver for external path transistor for V2 regulator function.
- Reset, programmable watchdog function, INT, 4 operational modes
- Programmable wake up input and cyclic sense wake up
- Can high speed physical interface

4.1 Device Supply

The device is supplied from the battery line through the Vsup pin. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5V and under the jump start condition at 27V DC. This pin sustains standard automotive voltage conditions such as load dump at 40V. When Vsup falls below 3V typical the MC33989 detects it and store the information into the SPI register, in a bit called “BATFAIL”. This detection is available in all operation modes.

4.2 Vdd1 Voltage Regulator

Vdd1 Regulator is a 5V output voltage with output current capability up to 200mA. As the V1 regulator supplies the CAN module, 120mA is available at the Vdd1 external outside the circuit. This Vdd1 regulator is normally used in the application for the main microcontroller supply. It includes a voltage monitoring circuitry associated with a reset function. The Vdd1 regulator is fully protected against over current, short-circuit and has over temperature detection warning flags and over temperature shutdown with hysteresis.

4.3 V2 regulator

V2 Regulator circuitry is designed to drive an external path transistor in order to increase output current flexibility. Two pins are used: V2 sense and V2 ctrl. Output voltage can be adjusted by an external resistor bridge, in a range from 1.8 to 8V. Vsup must be greater than V2 ctrl + 1V.

Target ballast transistor is PNP MJD32C. Other PNP transistor might be used, however depending upon PNP gain an external resistor capacitor network might be connected between emitter and base of PNP.

4.4 HS1 Vbat Switch Output

HS1 output is a 2 ohms typical switch from Vsup pin. It allows the supply of external switches and their associated pull up or pull down circuitry, in conjunction with the wake up input pins for example. Output current is limited to 200mA and HS1 is protected against short-circuit and over temperature. HS1 output is controlled from the internal register and SPI. It can be activated at regular intervals in sleep mode thanks to internal timer. It can also be permanently turned on in normal or stand-by modes to drive loads or supply peripheral components. No internal clamping protection circuit is implemented.

4.5 Functional Modes

The device has four modes of operation, the stand-by mode, normal mode, stop and sleep modes. All modes are controlled by the SPI. An additional temporary mode called “normal request mode” is automatically accessed by the device (refer to state machine) after wake up events. Two modes and configuration are possible for debug and program MCU flash memory.

4.5.1 Normal mode:

In this mode both regulators are ON and this corresponds to the normal application operation. All functions are available in this mode (watchdog, wake up input reading through SPI, HS1 activation, CAN communication). The software watchdog is running and must be periodically cleared though SPI.

4.5.2 Standby mode:

Only the regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2 ctrl pin. Same functions as in normal mode are available. The watchdog is running. In this mode, the device supply current from Vbat can be as low as 500uA, in the case where the MCU is in power save mode and the CAN interface disabled.

4.5.3 Sleep mode:

Regulators 1 and 2 are OFF. In this mode, the MCU is not powered. The sleep current from Vsup pin is less than 100uA (excluding CAN interface current). In this mode, the device can be awakened internally by cyclic sense via the wake up inputs pins and HS1 output, from the “forced wake up” function and from the CAN physical interface.

4.5.4 Stop mode

Regulator 2 is turned OFF by disabling the V2 ctrl pin. The regulator 1 is activated in a special low power mode which allow to deliver 2 mA. The objective is to maintain the MCU of the application supplied while it is turned into power saving condition (i.e stop or wait mode). In the stop mode, the device supply current from Vbat can be as low as 100uA (excluding CAN interface current), in the case where the MCU is in power save mode and CAN interface disabled. Stop mode is entered through SPI.

When the application is in stop mode (both MCU and SBC), the application can wake up from the SBC side (ex cyclic sense, forced wake up, CAN message, wake up inputs) or the MCU side (key wake up etc.).

When Stop mode is selected by SPI, stop mode becomes active 20us after end of SPI message. The “go to stop” instruction must be the last instruction executed by the MCU before going to low power mode.

In stop mode the Software watchdog can be “running” or “not running” depending upon selection by SPI. Refer to table 1 and SPI description.

In stop mode, SBC wake up capability are identical as in sleep mode. refer to table 1.

4.5.4.1 Application wake up from SBC side:

When application is in stop mode, it can wake up from the SBC side. When a wake up is detected by the SBC (ex CAN, Wake up input etc.) the SBC turns itself into Normal request mode. The wake up is signalled to the MCU through the INT pin. INT pin is pulled low for 10us and then returns high. Wake up event can be read through the SPI registers.

4.5.4.2 Application wake up from MCU side:

When application is in stop mode, the wake up event may come to the MCU. In this case the MCU has to signal to the SBC that it has to go into Normal mod in order for the Vdd1 regulator to be able to deliver full current capability. This is done by a low to high transisiton of the CSB pin. CSB pin low to high activation has to be done as soon as possible after the MCU.

Alternatively the L0 , L1, L2 and L3 inputs can also be used as wake up from stop mode.

4.5.4.3 Software watchdog in stop mode:

If watchdog is enabled, the MCU has to wake up independently of the SBC before the end of the SBC watchdog time. In order to do this the MCU has to signals the wake to the SBC through the SPI wake up (CSB activation). Then the SBC wakes up and jump into the normal request mode. MCU has to configured the SBC to go to either normal or standby mode. The MCU can then decide to go back again to stop mode.

If no MCU wakes up occurs within the watchdog timing, the SBC will activate the reset pin and jump into the normal request mode. The MCU can then be initialized.

4.5.5 Normal request mode:

This is a temporary mode automatically accessed by the device after a wake up event from sleep or stop mode or after device power up. In this mode the Vdd1 regulator is ON, V2 is off, the reset pin is high. As soon as the device enters the normal request mode an internal 400ms timer is started. During these 400ms the micro controller of the application must addressed the SBC via SPI and configure the watchdog register. This is the condition for the SBC to stop the 400ms timer and to go into the Normal mode and to set the watchdog timer according to configuration.

If no SPI configuration occurs within the 400ms, two cases must be considered:

- The “BATFAIL flag” has not been cleared: in this case the SBC goes to reset mode for 1ms, then return to normal request mode. If no W/D configuration is done within 400ms, the SBC goes to reset again, then normal request etc.
- If the “BATFAIL flag” has been reset, the SBC will goes back to previous low power mode. For instance If SBC was in sleep mode prior to the wake up it returns to sleep mode and keep the same wake up event configuration.

If SBC was in stop mode, it return to stop mode and keep the same wake up event configuration.

After an SBC power up (Vsup rising from zero to nominal), and if BATFAIL flag is cleared (MCR register read) the default low power mode is sleep mode.

“BATFAIL flag” is a bit which is triggered when Vsup is below 3V. This bit is set into the MCR register. It is reset by MCR register read.

4.5.6 Reset and watchdog: mode1 and mode 2 (safe mode):

The watchdog and reset functions have two modes of operation: mode 1 and mode 2 (mode 2 is also called safe mode). These modes are independent of the SBC modes (Normal, stand-by, sleep, stop). Mode 1 or mode 2 selection is done through SPI (register MCR, bit SAFE). Default mode after reset is mode 1.

4.6 Internal Clock

The device has an internal clock used to generate all timings (reset, watchdog, cyclic wake up, filtering time etc....).

4.7 Reset pin

A reset output is available in order to reset the microcontroller. Two operation modes for the reset pin are available, mode 1 and mode 2 (refer to table for reset pin operation).

The reset cause when SBC is in mode 1 are:

- Vdd1 falling out of range: if Vdd1 falls below the reset threshold (parameter Rst-th), the reset pin is pull low until Vdd1 return to nominal voltage.
- Power on reset: at device power on or at device wake up from sleep mode, the reset is maintained low until Vdd1 is within its operation range.
- Watchdog time out: if the watchdog is not cleared the SBC will pull the reset pin low for the duration of the reset duration time (parameter: reset-dur).

In mode 2, the reset pin is not activated in case of watchdog time out. Refer to” table for reset pin operation“for mode detail.

For debug purposes at 25°C, reset pin can be shorted to 5V.

4.8 Software watchdog (selectable window or time out watchdog)

Software watchdog is used in the SBC normal and stand-by modes for the MCU monitoring. The watchdog can be either window or time out. This is selectable by SPI (register TIM1, bit WDW). Default is window watchdog. The period for the watchdog is selectable from SPI from 5 to 400ms (register TIM1, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first half of the selected period, and the open window is the second half of the period. The

watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. Watchdog is cleared through SPI by addressing the TIM1 register.

4.9 Wake Up capabilities

Several wake-up capabilities are available for the device when it is in sleep or stop mode. When a wake up has occurred, the wake up event is stored into the WUR or CAN registers. The MCU can then access to the wake up source. The wake up options are selectable trough SPI while the device is in normal or standby mode and prior to go to enter low power mode (sleep or stop mode).

4.9.1 Wake up from wake up inputs (L0, L1, L2, L3) without cyclic sense:

The wake up lines are dedicated to sense external switches state and if changes occur to wake up the MCU (In sleep or stop modes). The wake up pins are able to handle 40V DC. The internal threshold is 3V typical and these inputs can be used as input port expander. The wake up inputs state can be read through SPI (register WUR).

4.9.2 Cyclic sense wake up (Cyclic sense timer and wake up inputs L0, L1, L2, L3)

The SBC can wake up upon state change of one of the four wake up input lines (L0, L1, L2 and L3) while the external pull up or pull down resistor of the switches associated to the wake up input lines are biased with HS1 Vsup switch. The HS1 switch is activated in sleep or stop mode from an internal timer. Cyclic sense and Forced wake up are exclusive. If Cyclic Sense is enabled the forced up can not be enabled.

4.9.3 Forced wake up

SBC can wake up automatically after a pre determined time spent in sleep or stop mode. Cyclic sense and Forced wake up are exclusive. If Forced wake up is enabled the Cyclic Sense can not be enabled.

4.9.4 CAN wake up

The device can wake up from a CAN message if CAN wake up has been enabled. Refer to CAN module description for detail of wake up detection.

4.9.5 SPI wake up

The device can wake up by the CSB pin in sleep or stop mode. Wake up is detetced by CSB pin transition from low to high level. In stop mode this correspond to the condition where MCU and SBC are in Stop mode and when the application wake up event comes through the MCU.

4.9.6 System power up

At power up the device automatically wakes up.

4.10 SPI

The complete device control as well as the status report is done through a 8 bits SPI interface. Refer to SPI paragraph.

4.11 CAN

The device incorporates a high speed 1MBaud CAN physical interface. Its electrical parameters for the CANL, CANH, Rx and Tx pins are compatible to ISO11898 specification (IS0 11898: 1993(E)). The control of the CAN physical interface operation is done through the SPI interface. CAN modes are independant of the SBC operation modes.

4.12 Device power up

After device or system power up the SBC enter into “normal request mode”.

4.13 Package and thermal consideration

The device is proposed in a standard surface mount SO28 package. In order to improve the thermal performances of the SO28 package, 8 pins are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

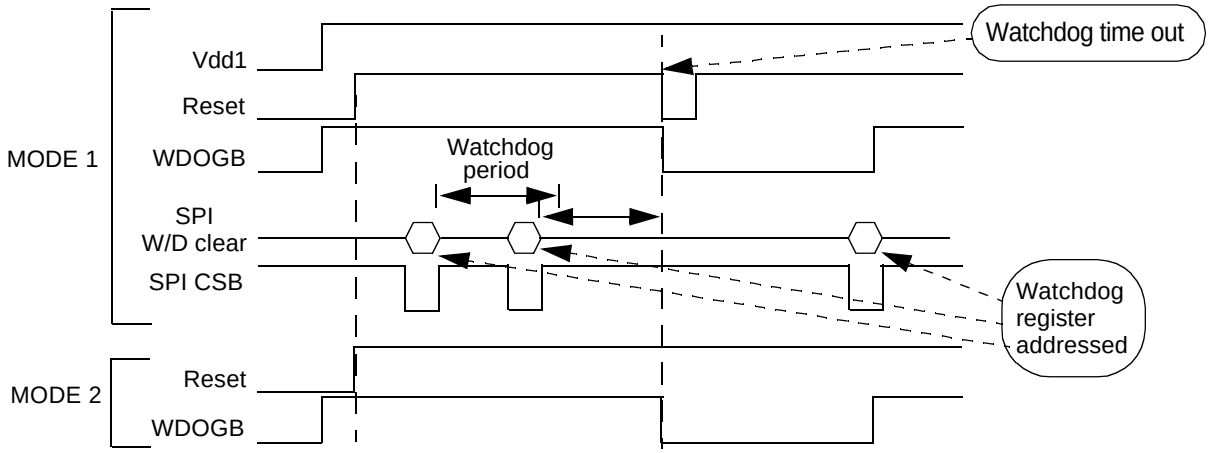
4.14 Table 1: Reset and Wdogb operation. Mode1 and Mode2.

Table below is the reset and watchdog output mode of operation. Two modes (mode 1 and mode 2) are available and are selectable through the SPI, safe bit. Default operation after reset or power up is mode 1.
In both modes reset is active at device power up and wake up.
In mode 1: Reset is activated in case of Vdd1 fall or watchdog not triggered. Wdogb output is active low as soon as reset goes low and stays low as long as the watchdog is not properly re-activated by SPI.
In mode 2, safe mode: Reset in not activated in case of Watchdog failure. WDOGB output has same behavior as in mode 1.
The Wdogb output pin is a push pull structure than can drive external component of the application in order for instance to signal MCU wrong operation.
Even if it is internally turned on (low sate) the reset pins can be forced to 5V at 25°C only, thanks to its internal limited current drive capability (capability used in Flash programming modes).

Events	Mode	WDOGB output	Reset output
Device power up	1 or 2 (safe mode)	low	low to high
- Vdd1 normal - Watchdog properly triggered	1	high	high
Vdd1 < Rst-th	1	high	low
Watchdog time out reached	1	low (note1)	low
- Vdd1 normal - Watchdog properly triggered	2 (safe mode)	high	high
Vdd1 < Rst-th	2 (safe mode)	high	low
Watchdog time out reached	2 (safe mode)	low (note1)	high

note1: Wdogb stays low until the Watchdog register is properly addressed through SPI.

Figure 5. Reset and Wdogb functions diagram in mode 1 and 2



4.15 Application hardware and software debug with the SBC

When the SBC is mounted on the same printed circuit board as the mico contoller it supplies, both application software and SBC dedicated rouitne must be debugged. Following features allow the user to debug the software by allowing the possiblity to disable the SBC internal software watchdog timer.

4.15.1 First SBC power up, reset pin connected to Vdd1

At SBC power up, the Vdd1 voltage is provided, but if no SPI communication occurs to configure the device in normal mode, a reset occurs every 400ms. In order to allow software debug and avoid MCU reset the Reset pin can be connected directly to Vdd1 by a jumper.

4.15.2 Debug modes with sowftare watchdog disabled though SPI (Debug Normal and Debug Standby)

The software watchdog can be disabled through SPI. But in order to avoid unwanted watchdog disable and to limit the risk of disabling the watchdog during SBC normal operation the watchdog disable has to be done when the “bat fail flag” is set. The bat fail flag is set when the SBC supply voltage (Vsup) has been lower than 3V. This is the case at SBC power up.

When this is done, the watchdog of the SBC is disabled, SBC can be used without having to clear the W/D on a regular basis to facilitate software and hardware debug.

4.15.3 MCU flash programming configuration

In order to allow the possibility to download software into the application memory (MCU EEPROM or Flash) the SBC allows the following capabilities: The Vdd1 can be forced by an external power supply to 5V and the reset and Wdogb outputs by external signal sources to zero or 5V and this without damage. This allow for instance to supply the complete application board by external power supply and to apply the correct signal to reset pins.

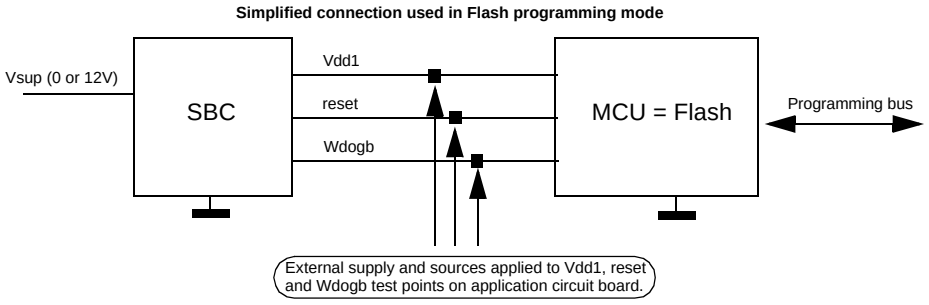
5 TABLE OF OPERATION

The table below describe the SBC operation modes.

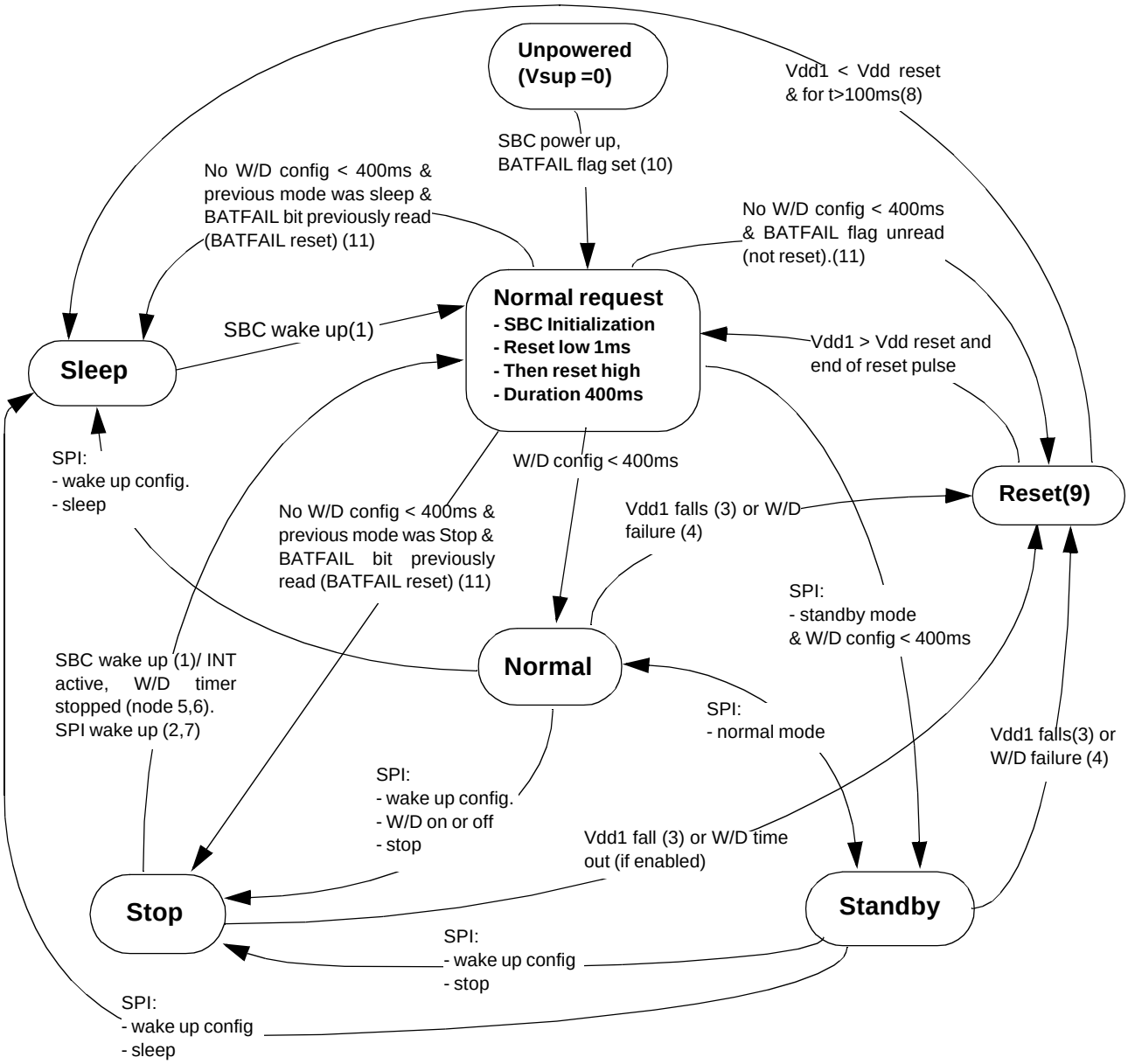
mode	Voltage Regulator HS1 switch	Wake up capabilities (if enabled)	Reset pin	INT	Software Watchdog	CAN cell
Normal Request	Vdd1: ON V2: OFF HS1: OFF		Low for 1ms, then high			
Normal	Vdd1: ON V2: ON HS1 controllable		- Normally high. - Active low if W/D or Vdd1 under voltage occurs (and mode 1 selected)	If enabled, signal failure (Vdd pre warning temp, CAN, HS1)	Running	Tx/Rx
Standby	Vdd1: ON V2: OFF HS1 controllable		same as Normal Mode	same as Normal Mode	Running	Tx/Rx
Stop	Vdd1: ON (2mA capability) V2: OFF HS1: OFF or cyclic	- CAN - SPI - L0,L1,L2,L3 - Cyclic sense - Forced Wake up	- Normally high. - Active low if W/D (*) or Vdd1 under voltage occurs (*): if enabled	Signal SBC wake up (not maskable)	- Running if enabled - Not Running if disabled	- Low Power - Wake up capability if enabled
Sleep	Vdd1: OFF V2: OFF HS1 OFF or cyclic	- CAN - SPI - L0,L1,L2,L3 - Cyclic sense - Forced Wake up	Low	Not active	No Running	- Low Power - Wake up capability if enabled
Debug Normal	Vdd1: ON V2: ON HS1 controllable		- Normally high. - Active low if Vdd1 under voltage occur	Same as Normal	Not running	same as Normal
Debug Standby	Vdd1: ON V2: OFF HS1 controllable		- Normally high. - Active low if Vdd1 under voltage occur	Same as Standby	Not running	same as Standby
Flash programming	Forced externally		not operating	not operating	not operating	not operating

Tableau 1 : table of operation

“Debug Normal” and “Debug Standby” are entered vai SPI, register MCR. Bit BATFAIL must be set.
Flash programming mode is a mode ,where the SBC outputs Vdd1, V2 and reset can be powered externaly to provide power to MCU and peripheral components. No function of the SBC are operating.



6 SIMPLIFIED STATE MACHINE

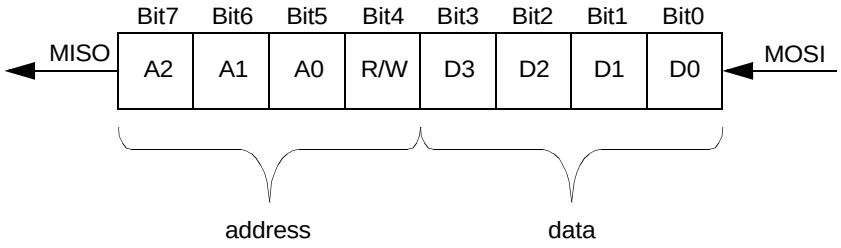


Comments:

(1): SBC wake up: wake up from CAN, Lx, Cyclic sense or forced wake up.
(2): SPI wake up: wake up from CSB pin (Wake up through MCU activity).
(3): Vdd1 falls: Vdd1 falls below Vdd1 reset threshold
(4): W/D failure: Watchdog not triggered before time out, or Watchdog trigger in the closed window.
(5): In stop mode when SBC wakes up, wake up is transmitted to MCU through INT pin activation. INT stays low until INT register is read (cleared).
(6): In stop mode, if W/D is enabled, when SBC goes out of stop mode before W/D time out, W/D timer is stopped. Then the normal request mode 400ms timer starts. If no SPI configuration occurs within the 400ms SBC goes back to Stop mode with same conditions (wake up, W/D enable etc.).
(7): In stop mode when MCU goes out of its low power mode, this event is transmitted to SBC through an SPI wake up (CSB pin activation).
(8): In case of short circuit or over load condition at Vdd. SBC goes to Sleep mode after 100ms.
(9): In reset mode Vdd1 is ON and can deliver full current capability (120mA). Reset pulse occurs at reset pin.
(10): BATFAIL bit is set to 1 when Vsup fall below 3V typical.
(11): BATFAIL is reset when MCR register is read.

7 SPI INTERFACE AND REGISTER DESCRIPTION

7.1 Data format description



Read operation: R/W bit = 0

Write operation: R/W bit = 1

The SPI is a 8 bit SPI. First 3 bits are used to identify the internal SBC register adress, bit 4 is a read/write bit. The last 4 bits are data send from MCU to SBC or read back from SBC to MCU.

Following tables describe the SPI register list, and register bit meaning. Register containt at reset is also described.

7.2 List of Registers:

Name	Adress	Description	Comment and usage
MCR	$ 0 0 0	Mode control register	Write: Control of normal, standby, sleep, stop, debug modes Read: BATFAIL flag and other status bits and flags
RCR	$ 0 0 1	Reset control register	Write: Configuration of reset voltage level and safe bit
CAN	$ 0 1 0	CAN control register	Write: CAN module control: Tx/Rx & sleep modes, slope control, wake enable/disable. Read: CAN wake up and CAN failure status bits
IOR	$ 0 1 1	I/O control register	Write: HS1 (high side switch) control in normal and standby mode Read: HS1 over temp bit
WUR	$ 1 0 0	Wake up input register	Write: Control of wake up input polarity Read: Wake up input, and real time Lx input state
TIM	$ 1 0 1	Timing register	Write: TIM1, Watchdog timing control, window or Timeout mode. Write: TIM2, Cyclic sense and force wake up timing selection
LPC	$ 1 1 0	Low power mode control register	Wrtite: HS1 periodic activation in sleep and stop modes, force wake up control.
INTR	$ 1 1 1	Interrupt register	Write: Interrupt source configuration Read: INT source

Table 7-1.

7.2.1 MCR register

MCR		D3	D2	D1	D0
$000b	W	WDSTOP	MCTR2	MCTR1	MCTR0
	R	BATFAIL	VDDTEMP	GFAIL	WDRST
Reset		0	0	0	0

Table 7-2.

Control bits:

BATFAIL	MCTR2	MCTR1	MCTR0	SBC mode	Description
X	automatically entered after reset			Normal Request	
0	0	0	1	Normal	
0	0	1	0	Standby	
X	0	1	1	Stop	

Table 7-3.

BATFAIL	MCTR2	MCTR1	MCTR0	SBC mode	Description
0	1	0	0	Sleep	
1 (*)	1	0	1	Normal	For debugging only, **watchdog is disabled**
1 (*)	1	1	0	Standby	

Table 7-3.

(*) : Bit BATFAIL cannot be set by SPI. BATFAIL is set when Vsup falls below 3V.

WDSTOP	Watchdog in Stop mode
0	OFF, watchdog not running once SBC is in Stop mode
1	ON, watchdog running when SBC is in Stop mode

Status bits:

Status bit	Description
GFAIL	Logic OR of CAN or HS1 failure
BATFAIL	Battery fail flag (set when Vsup < 3V)
VDDTEMP	Temperature pre-warning on VDD (latched)
WDRST	Watchdog reset occurred

7.2.2 RCR register

RCR		D3	D2	D1	D0
$001b	W			SAFE	RSTTH
	R				
Reset				0	0

Table 7-4.

Control bits:

Condition	SAFE	WDOGB pin	Reset pin
Device power up	0 1	0	0→1
V1 normal, WD is properly triggered	0 1	1	1 1
V1 drops below 4.5 volt	0 1	1 1	0 0
WD time out	0 1	0	0 1

Table 7-5.

RSTTH	Reset threshold voltage [V]
0	4.5
1	3.7

7.2.3 CAN register

Description : control of the high speed CAN module, mode, slew rate and wake up

CAN		D3	D2	D1	D0
$010b	W		SC1	SC0	MODE
	R	CANWU	TXF	CUR	THERM
Reset			0	0	0

Table 7-6.

7.2.3.1 High speed CAN transceiver modes

Description: Mode bit (D0) controls the state of the CAN module, Normal or Sleep mode. SCO bit (D1) defines the slew rate when the CAN module is in normal, and controls the wake up option (wake up enable or disable) when the CAN module is in sleep mode. CAN module modes (Normal and Sleep) are independant of the SBC modes.

SC1	SC0	MODE	CAN Mode
0	0	0	CAN normal, slew rate 0
0	1	0	CAN normal, slew rate 0
1	0	0	Can normal, slew rate 0
1	1	0	Can normal, slew rate 0
X	1	1	Can sleep, wake up disable
X	0	1	Can sleep, wake up enable

Status bits:

Status bit	Description
CANWU	CAN wake-up occurred
TXF	Permanent dominant TX
CUR	CAN transceiver in current limitation
THERM	CAN transceiver in thermal shut down

7.2.4 IOR register

Description.: control of HS1 in normal and standby modes

IOR		D3	D2	D1	D0
$011b	W		HS1ON		
	R		HS1OT		
Reset			0		

Table 7-1.

Control bits:

HS1ON	HS1 state
0	HS1 OFF, in normal and standby mode
1	HS1 ON, in normal and standby mode

Table 7-2.

Status bits:

Status bit	Description
HS1OT	High side 1 over temperature

Once the switch has been turned off because of over temperature, it can be turned on again by setting the appropriate control bit to “1”.

7.2.5 WUR register

The local wake-up inputs L0, L1, L2, and L3 can be used in both normal and standby mode as port expander and for waking up the SBC in sleep or stop mode.

WUR		D3	D2	D1	D0
$100b	W	LCTR3	LCTR2	LCTR1	LCTR0
	R	L3WU	L2WU	L1WU	L0WU
Reset		0	0	0	0

Table 7-3.

The wake-up inputs can be configured almost separetly, where L0 and L1 are configured toghether and L2 and L3 are configured toghether.

Control bits:.

LCTR3	LCTR2	LCTR1	LCTR0	L0/L1 configuration	L2/L3 configuration
X	X	0	0	inputs disabled	
X	X	0	1	high level sensitive	
X	X	1	0	low level sensitive	
X	X	1	1	both level sensitive	
0	0	X	X		inputs disabled
0	1	X	X		high level sensitive
1	0	X	X		low level sensitive
1	1	X	X		both level sensitive

Table 7-4.

Status bits:

Status bit	Description
L3WU	Wake-up occurred (sleep/ stop mode), logic state on Lx (standby/ normal mode)
L2WU	
L1WU	
L0WU	

note : Status bits have two functions. After SBC wake up, they indicate the wake up source (LxWU set at 1 if wake up source is Lx). After SBC wake and once the WUR has been read, status bits indicates the real time state of the Lx inputs (1 mean Lx is above threshold, 0 means that Lx input is below threhold).

7.2.6 TIM registers

Description : This register is splitted into 2 sub registers, TIM1 and TIM2.
TIM1 controls the watchdog timing selection as well as the window or time out option. TIM1 is selected when bit D3 is 0.
TIM2 is used to define the timing for the cyclic sense and forced wake up function. TIM2 is selected when bit D3 is 1.
No read operation is allowed for registers TIM1 and TIM2

7.2.7 TIM1 register.

TIM1		D3	D2	D1	D0
$101b	W	0	WDW	WDT1	WDT0
	R				
Reset			0	0	0

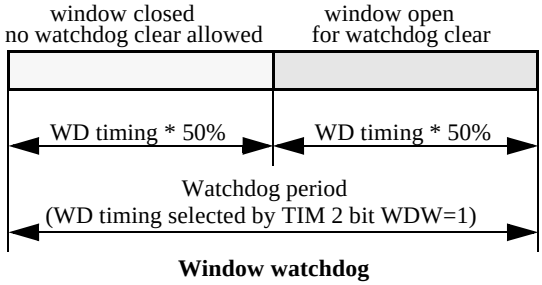
Table 7-5.

Description

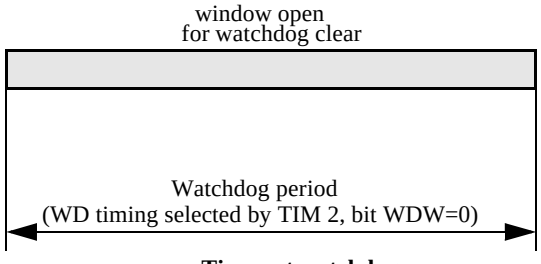
WDW	WDT1	WDT0	Watchdog timing [ms]	
0	0	0	10	no window watchdog
0	0	1	50	
0	1	0	100	
0	1	1	400	
1	0	0	10	window watchdog enabled (window lenght is half the watchdog timing)
1	0	1	50	
1	1	0	100	
1	1	1	400	

Table 7-6.

Watchdog operation (window and time out)



Window watchdog



Time out watchdog

7.2.8 TIM2 register

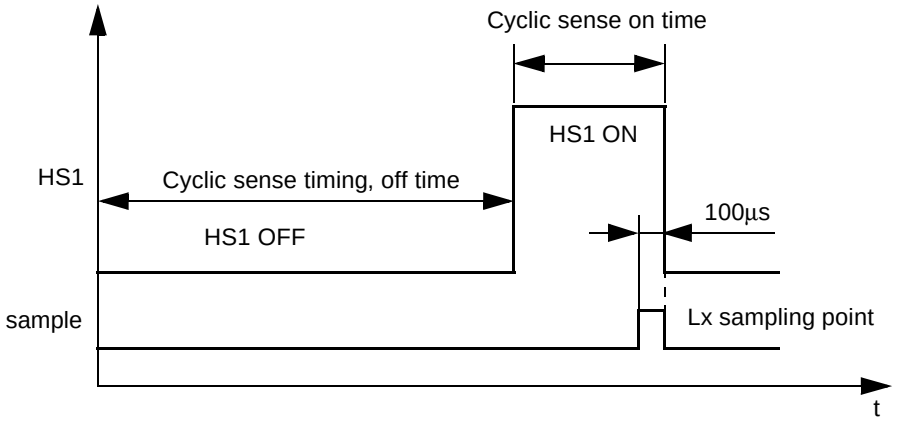
The purpose of TIM2 register is to select an appropriate timing for sensing the wake-up circuitry or cyclically supplying devices by switching on or off HS1.

TIM2		D3	D2	D1	D0
$101b	W	1	CSP2	CSP1	CSP0
	R				
Reset			0	0	0

Table 7-7.

CSP2	CSP1	CSP0	Cyclic sense timing [ms]
0	0	0	5
0	0	1	10
0	1	0	20
0	1	1	40
1	0	0	75
1	0	1	100
1	1	0	200
1	1	1	400

Table 7-8.



7.2.9 LPC register

Description: This register controls:

- The state of HS1 in stop and sleep mode (HS1 permanently off or HS1 cyclic)
- Enable or Disable the forced wake up function (SBC automatic wake up after time spend in sleep or stop mode, time defined by TIM2 register)
- Enable of disable the sense of the wake up inputs (Lx) at sampling point of the cyclic sense period (LX2HS1 bit).

LPC		D3	D2	D1	D0
$110b	W	LX2HS1	FWU		HS1AUTO
	R				
Reset		1	0	0	0

Table 7-9.

LX2HS1	HS1AUTO	Wake-up inputs supplied by HS1	Autotiming HS1 in sleep and stop modes
X	0		off
X	1		on, HS1 cyclic, perdio defined in TIM2 register
0	X	no	
1	X	yes, Lx inputs sensed at sampling point	

Table 7-10.

7.2.10 INTR register

Description: This register allows to mask or enable the INT source. A read operation informs about the interrupt source.

INTR		D3	D2	D1	D0
$111b	W		HS1OT	VDDTEMP	CANF
	R		HS1OT	VDDTEMP	CANF
Reset			0	0	0

Table 7-11.

Control bits:

Control bit	Description
CANF	Mask bit for CAN failures
VDDTEMP	Mask bit for VDD medium temperature
HS1OT	Mask bit for HS1 over temperature

When the mask bit has been set, INTB pin goes low if the appropriate condition occurs.

Status bits:

Status bit	Description
CANF	CAN failure
VDDTEMP	VDD medium temperature (pre warning)
HS1OT	HS1 over temperature

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