Integrated Circuit Systems, Inc.

ICS950813
Advance Information

Frequency Generator with 200MHz Differential CPU Clocks

Recommended Application:

CK-408 clock for Brookdale/Odem/Montara-GM for P4/Banias processor.

Output Features:

- 3 Differential CPU Clock Pairs @ 3.3V
- 7 PCI (3.3V) @ 33.3MHz including 2 early PCI clocks
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz, 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

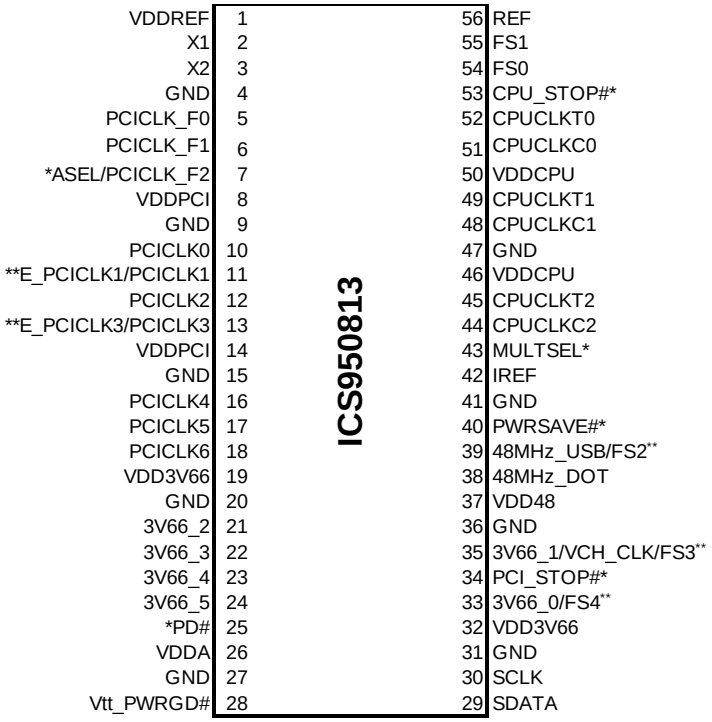
Features:

- Provides standard frequencies and additional 3%, 5% and 10% over-clocked frequencies
- Supports spread spectrum modulation: No spread, Center Spread (±0.3%, ±0.55%), or Down Spread (-0.5%, -0.75%)
- Offers adjustable PCI early clock via latch inputs
- Selectable 1X or 2X strength for REF via I^2C interface
- Programmable group to group skew
- Linear programmable frequency and spreading %
- Efficient power management scheme through PD#, CPU_STOP# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through I^2C interface.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

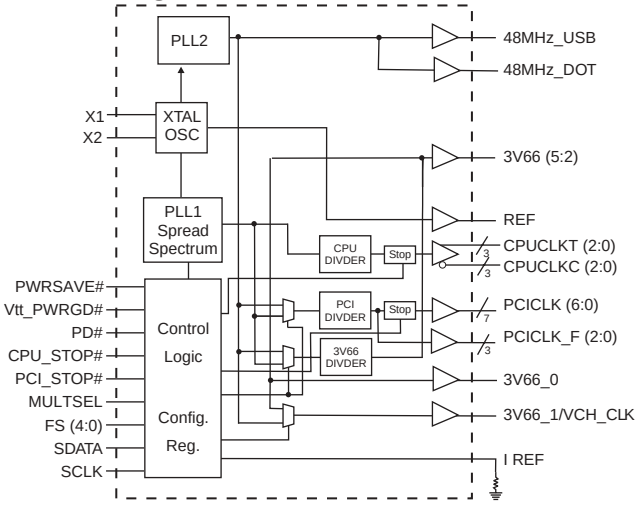
Pin Configuration



56-Pin 300mil SSOP
56-Pin 240mil TSSOP

*These inputs have 120K internal pull-up resistors to VDD.
**Internal pull-down resistors to ground.

Block Diagram



0708—10/10/02

Functionality Table

FS1	FS0	CPU	AGP	PCI
		MHz	MHz	MHz
0	0	100.00	66.67	33.33
0	1	133.33	66.67	33.33
1	0	200.00	66.67	33.33
1	1	166.66	66.66	33.33

Asynchronous AGP/PCI Frequency Selection Table

Byte7 Bit5	Byte7 Bit4	AGP Frequency	PCI Frequency
0	0	66.00	33.00
0	1	75.43	37.72
1	0	88.00	44.00
1	1	--	--

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	X1	IN	Crystal input,nominally 14.318MHz.
3	X2	OUT	Crystal output, Nominally 14.318MHz
4	GND	PWR	Ground pin.
5	PCICLK_F0	OUT	Free running PCI clock not affected by PCI_STOP# .
6	PCICLK_F1	OUT	Free running PCI clock not affected by PCI_STOP# .
7	*ASEL/PCICLK_F2	I/O	Asynchronous AGP/PCI frequency latch input pin / 3.3V PCI free running clock put. Pull-Up = Main PLL / Pull-Down = Async Fix PLL
8	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
9	GND	PWR	Ground pin.
10	PCICLK0	OUT	PCI clock output.
11	**E_PCICLK1/PCICLK1	I/O	Early/Normal PCI clock output latched at power up.
12	PCICLK2	OUT	PCI clock output.
13	**E_PCICLK3/PCICLK3	I/O	Early/Normal PCI clock output latched at power up.
14	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
15	GND	PWR	Ground pin.
16	PCICLK4	OUT	PCI clock output.
17	PCICLK5	OUT	PCI clock output.
18	PCICLK6	OUT	PCI clock output.
19	VDD3V66	PWR	Power pin for the 3V66 clocks.
20	GND	PWR	Ground pin.
21	3V66_2	OUT	3.3V 66.66MHz clock output
22	3V66_3	OUT	3.3V 66.66MHz clock output
23	3V66_4	OUT	3.3V 66.66MHz clock output
24	3V66_5	OUT	3.3V 66.66MHz clock output
25	*PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
26	VDDA	PWR	3.3V power for the PLL core.
27	GND	PWR	Ground pin.
28	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input.

Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
29	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
31	GND	PWR	Ground pin.
32	VDD3V66	PWR	Power pin for the 3V66 clocks.
33	3V66_0/FS4**	I/O	Frequency select latch input pin / 3.3V 66.66MHz clock output.
34	PCI_STOP#*	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
35	3V66_1/VCH_CLK/FS3**	I/O	Frequency select latch input pin / 3.3V 66.66MHz clock output / 48MHz VCH clock output.
36	GND	PWR	Ground pin.
37	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
38	48MHz_DOT	OUT	48MHz clock output.
39	48MHz_USB/FS2**	I/O	Frequency select latch input pin / 3.3V 48MHz clock output.
40	PWRSAVE#*	IN	Real Time input pin to change frequency to under-clock entries located in FS 4:2 = '100'. Clock groups gear ratio will not be change during this operation.
41	GND	PWR	Ground pin.
42	IREF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL*	IN	3.3V LVTTL input for selection the current multiplier for CPU outputs
44	CPUCLKC2	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	CPUCLKT2	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
46	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
47	GND	PWR	Ground pin.
48	CPUCLKC1	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
49	CPUCLKT1	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
50	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
51	CPUCLKC0	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
53	CPU_STOP#*	IN	Stops all CPUCLK besides the free running clocks
54	FS0	IN	Frequency select pin.
55	FS1	IN	Frequency select pin.
56	REF	OUT	14.318 MHz reference clock.

Power Supply

Pin Number		Description
VDD	GND	
1	4	Xtal, Ref, CPU PLL, digital
37	36	48MHz, Fix Digital, Fix Analog
46	47	Master clock, CPU Analog

Frequency Select Table 1

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
0	0	0	0	0	100.00	66.67	33.33	0.3% Center
0	0	0	0	1	133.33	66.67	33.33	0.3% Center
0	0	0	1	0	200.00	66.67	33.33	0.3% Center
0	0	0	1	1	166.66	66.66	33.33	0.3% Center
0	0	1	0	0	100.00	66.67	33.33	0 - 0.5% down
0	0	1	0	1	133.33	66.67	33.33	0 - 0.5% down
0	0	1	1	0	200.00	66.67	33.33	0 - 0.5% down
0	0	1	1	1	166.66	66.66	33.33	0 - 0.5% down
0	1	1	0	0	100.00	66.67	33.33	0.55% Center
0	1	1	0	1	133.33	66.67	33.33	0.55% Center
0	1	1	1	0	200.00	66.67	33.33	0.55% Center
0	1	1	1	1	166.66	66.66	33.33	0.55% Center
0	1	0	0	0	100.00	66.67	33.33	0 - 0.75% down
0	1	0	0	1	133.33	66.67	33.33	0 - 0.75% down
0	1	0	1	0	200.00	66.67	33.33	0 - 0.75% down
0	1	0	1	1	166.66	66.66	33.33	0 - 0.75% down
1	0	0	0	0	80.00	53.33	26.67	Spread Off
1	0	0	0	1	106.66	53.33	26.67	Spread Off
1	0	0	1	0	160.00	53.33	26.67	Spread Off
1	0	0	1	1	133.33	53.33	26.67	Spread Off
1	0	1	0	0	103.00	68.67	34.33	0.3% Center
1	0	1	0	1	137.33	68.66	34.33	0.3% Center
1	0	1	1	0	206.00	68.67	34.33	0.3% Center
1	0	1	1	1	171.66	68.66	34.33	0.3% Center
1	1	0	0	0	105.00	70.00	35.00	0.3% Center
1	1	0	0	1	140.00	70.00	35.00	0.3% Center
1	1	0	1	0	Tristate	Tristate	Tristate	N/A
1	1	0	1	1	174.99	70.00	35.00	0.3% Center
1	1	1	0	0	110.00	73.33	36.67	0.3% Center
1	1	1	0	1	146.66	73.33	36.67	0.3% Center
1	1	1	1	0	Test/2	Test/4	Test/8	N/A
1	1	1	1	1	183.33	73.33	36.67	0.3% Center

Host Swing Select Functions

MULTSEL	Board Target	Reference R,	Output	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4 * I REF	1.0V @ 50 ohm
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6 * I REF	0.7V @ 50 ohm

PCI Select Functions

E_PCICLK1	E_PCICLK3	E_PCICLK(3,1)*
0	0	0ns
0	1	0.5ns
1	0	1.0ns
1	1	1.5ns

Note:

E_PCICLK1 = 10Kohm resistor.
E_PCICLK3 = 10Kohm resistor.
0 = No resistor
1 = 10Kohm pull-up to V_{DD}.
* Approximate values

Frequency Select Table 2

Freqency Select			CPU, 3V66, PCI	Clocking Mode
FS4	FS3	FS2		
0	0	0	Standard Clocking	0.3% Center Spread
0	0	1	Standard Clocking	0 to -0.5%, Down Spread
0	1	0	Standard Clocking	0.3% Center Spread
0	1	1	Standard Clocking	0 to - 0.75%, Down
1	0	0	Pwr Save Clocking	Spread Off
1	0	1	3% Overclocking	0.3% Center Spread
1	1	0	5% Overclocking	0.3% Center Spread
1	1	1	10% Overclocking	0.3% Center Spread

PWRSAVE# = '1'. as PWRSAVE# is driven back to high '1'. The output frequencies will be driven back to the original programmed frequencies smoothly. Notice that this operation will only happen after the PWRSAVE# has been driven to '0'. This will not affect power up or I2C programmed frequencies if the PWRSAFE# has been tied to a '1'.

PWRSAVE# Usage Illustration

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz
X	X	X	0	0	XXX	XXX	XXX
X	X	X	0	1	XXX	XXX	XXX
X	X	X	1	0	XXX	XXX	XXX
X	X	X	1	1	XXX	XXX	XXX
1	0	0	0	0	80.00	53.33	26.67
1	0	0	0	1	106.66	53.33	26.67
1	0	0	1	0	160.00	53.33	26.67
1	0	0	1	1	133.33	53.33	26.67

PWRSAVE# = '0'. as PWRSAVE# is driven to low '0'. The output frequencies of the CPU, AGP and PCI clock will smoothly switch to frequencies indicated by FS (4:2) = 100. The frequencies gear ratio will be kept the same. Notice that the 48MHz & REF frequencies will not be changed. This function can be used with asynchronous AGP/PCI frequencies.

BYTE 0	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	Spread Enabled	Spread Spectrum Control	RW	OFF	ON	0
Bit 6	-	CPUCLKT(2:0)	Power down mode output level 0= CPU driven in power down 1= undriven	RW	HIGH	LOW	0
Bit 5	35	3V66_1/VCH_CLK/FS3**	VCH/66.66 Select	RW	66.66	48.00	0
Bit 4	53	CPU_STOP#*	Reflects value of pin	R	Stop	Active	X
Bit 3	34	PCI_STOP#*	Reflects value of pin at power up. Also can be set.	RW	Stop	Active	X
Bit 2	39	FS3	Frequency Selection	RW	-	-	X
Bit 1	55	FS1	Frequency Selection	R	-	-	X
Bit 0	54	FS0	Frequency Selection	R	-	-	X

Note: For PCI_STOP# function, refer to table 3.

BYTE 1	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	43	MULTSEL*	Reflects value of pin	R	-	-	x
Bit 6	-	CPUCLKT(2:0)	CPU_Stop mode output level 0= CPU driven when stopped 1 = undriven	RW	HIGH	LOW	0
Bit 5	45, 44	CPUCLKT2, CPUCLKC2 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 4	49, 48	CPUCLKT1, CPUCLKC1 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 3	52, 51	CPUCLKT0, CPUCLKC0 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 2	45, 44	CPUCLKT2, CPUCLKC2	Output control	RW	Disable	Enable	1
Bit 1	49, 48	CPUCLKT1, CPUCLKC1	Output control	RW	Disable	Enable	1
Bit 0	52, 51	CPUCLKT0, CPUCLKC0	Output control	RW	Disable	Enable	1

Note: CPUCLK(2:0) can be turned on/off by CPU_STOP#. Refer to table 4.

BYTE 2	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	56	REF	1X or 2X Strength control	RW	1X	2X	0
Bit 6	18	PCICLK6	Output control	RW	Disable	Enable	1
Bit 5	17	PCICLK5	Output control	RW	Disable	Enable	1
Bit 4	16	PCICLK4	Output control	RW	Disable	Enable	1
Bit 3	13	**E_PCICLK3/PCICLK3	Output control	RW	Disable	Enable	1
Bit 2	12	PCICLK2	Output control	RW	Disable	Enable	1
Bit 1	11	**E_PCICLK1/PCICLK1	Output control	RW	Disable	Enable	1
Bit 0	10	PCICLK0	Output control	RW	Disable	Enable	1

Note: PCICLK(6:0) can be turned on/off by PCI_STOP#. Refer to table 3.

BYTE 3	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	38	48MHz_DOT	Output control	RW	Disable	Enable	1
Bit 6	39	48MHz_USB/FS2**	Output control	RW	Disable	Enable	1
Bit 5	7	*ASEL/PCICLK_F2 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 4	6	PCICLK_F1 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 3	5	PCICLK_F0 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 2	7	*ASEL/PCICLK_F2	Output control	RW	Disable	Enable	1
Bit 1	6	PCICLK_F1	Output control	RW	Disable	Enable	1
Bit 0	5	PCICLK_F0	Output control	RW	Disable	Enable	1

Note: PCICLK_F(2:0) can be turned on/off by PCI_STOP#. Refer to table 5.

BYTE 4	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	35	FS3	Frequency Selection	RW	-	-	X
Bit 6	33	FS4	Frequency Selection	RW	-	-	X
Bit 5	33	3V66_0/FS4**	Output control	RW	Disable	Enable	1
Bit 4	35	3V66_1/VCH_CLK/FS3**	Output control	RW	Disable	Enable	1
Bit 3	24	3V66_5	Output control	RW	Disable	Enable	1
Bit 2	23	3V66_4	Output control	RW	Disable	Enable	1
Bit 1	22	3V66_3	Output control	RW	Disable	Enable	1
Bit 0	21	3V66_2	Output control	RW	Disable	Enable	1

BYTE 5	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	PD Mode Iref Mirror Enable	Allow Iref Mirror to be ON during Power Down Mode	RW	OFF	ON	0
Bit 6	X	Reserved	Reserved	X	-	-	0
Bit 5	X	3V66(5:2) (See table 6)	Allow control of output with assertion of CPU_STOP#.	X	Freerun	Not Freerun	0
Bit 4	X	3V66(1:0) (See table 7)	Allow control of output with assertion of CPU_STOP#.	X	Freerun	Not Freerun	0
Bit 3	38	48MHz_DOT Slew Control	00 = Medium (default), 01 = Low, 11,10 =High	RW	-	-	0
Bit 2				RW	-	-	0
Bit 1	39	48MHz_USB Slew Control	00 = Medium (default), 01 = Low, 11,10 =High	RW	-	-	0
Bit 0				RW	-	-	0

Note: Functions in Byte 5 of CK408 were intended as a test and debug byte only.

BYTE 6	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	Revision ID Bit 3	Revision ID Value Based on Device Revision	R	-	-	0
Bit 6	X	Revision ID Bit 2		R	-	-	0
Bit 5	X	Revision ID Bit 1		R	-	-	0
Bit 4	X	Revision ID Bit 0		R	-	-	0
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	0
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	0
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	0
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

BYTE 7	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	AEN	3V66/PCI Freq Source Select	RW	Fix_PLL Async	CPU_PLL Sync	1
Bit 5	X	AFS1	Async Freq select bit 1	RW	See Async Freq Selection Table		0
Bit 4	X	AFS0	Async Freq select bit 0	RW			0
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

BYTE 8	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	X	-	-	0
Bit 6	X	-	(Reserved)	X	-	-	0
Bit 5	X	-	(Reserved)	X	-	-	0
Bit 4	X	-	(Reserved)	X	-	-	0
Bit 3	X	-	Readback Byte Count	R	-	-	1
Bit 2	X	-		R	-	-	1
Bit 1	X	-		R	-	-	1
Bit 0	X	-		R	-	-	1

Note: Byte 8 is for ICS test only. Do not write as system damage may occur. Bit(2:0) contain the readback Byte count.

BYTE 9	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	35	VCHCLK Slew Control	00 = High(default), 01 = Low, 11,10 = Medium	RW	-	-	0
Bit 6				RW	-	-	0
Bit 5	7, 6, 5	PCICLK_F (2:0) Slew Contol	00 (default), 11 = Medium 01 = Low, 10 =High	RW	-	-	0
Bit 4				RW	-	-	0
Bit 3	13, 12, 11, 10	PCICLK (3:0) Slew Contol	00 (default), 11 = Medium 10 = Low, 01 =High	RW	-	-	0
Bit 2				RW	-	-	0
Bit 1	18, 17, 16	PCICLK (6:4) Slew Contol	00 (default), 11 = Medium 10 = Low, 01 =High	RW	-	-	0
Bit 0				RW	-	-	0

BYTE 10	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	M/N Enable (Enable access to Byte 11 - 14)	RW	HW/B0	Byte (11-14)	0
Bit 6	X	-	Unused	-	-	-	0
Bit 5	X	3V66 (5:2) Skew	Approx 250ps per bit (Ref to PCI)	RW	-	-	0
Bit 4	X			RW	-	-	0
Bit 3	X	-	Unused	-	-	-	1
Bit 2	X	-	Unused	-	-	-	0
Bit 1	X	-	Unused	-	-	-	1
Bit 0	X	-	Unused	-	-	-	0

Note: See table 8 for Byte 11-14 default information

BYTE 11	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	VCO Divider Bit8	RW	-	-	X
Bit 6	X	-	REF Divider Bit6	RW	-	-	X
Bit 5	X	-	REF Divider Bit5	RW	-	-	X
Bit 4	X	-	REF Divider Bit4	RW	-	-	X
Bit 3	X	-	REF Divider Bit3	RW	-	-	X
Bit 2	X	-	REF Divider Bit2	RW	-	-	X
Bit 1	X	-	REF Divider Bit1	RW	-	-	X
Bit 0	X	-	REF Divider Bit0	RW	-	-	X

Note: The decimal representation of these 7 bits (Byte 11 bit[6:0]) + 2 is equal to the REF divider value.

BYTE 12	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	VCO Divider Bit7	RW	-	-	X
Bit 6	X	-	VCO Divider Bit6	RW	-	-	X
Bit 5	X	-	VCO Divider Bit5	RW	-	-	X
Bit 4	X	-	VCO Divider Bit4	RW	-	-	X
Bit 3	X	-	VCO Divider Bit3	RW	-	-	X
Bit 2	X	-	VCO Divider Bit2	RW	-	-	X
Bit 1	X	-	VCO Divider Bit1	RW	-	-	X
Bit 0	X	-	VCO Divider Bit0	RW	-	-	X

Note: The decimal representation of these 9 bits (Byte 12 bit[7:0]) and Byte 11 bit [7]) + 8 is equal to the VCO divider value.

BYTE 13	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	Spread Spectrum Bit7	RW	-	-	X
Bit 6	X	-	Spread Spectrum Bit6	RW	-	-	X
Bit 5	X	-	Spread Spectrum Bit5	RW	-	-	X
Bit 4	X	-	Spread Spectrum Bit4	RW	-	-	X
Bit 3	X	-	Spread Spectrum Bit3	RW	-	-	X
Bit 2	X	-	Spread Spectrum Bit2	RW	-	-	X
Bit 1	X	-	Spread Spectrum Bit1	RW	-	-	X
Bit 0	X	-	Spread Spectrum Bit0	RW	-	-	X

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

BYTE 14	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	RW	-	-	X
Bit 6	X	-	(Reserved)	RW	-	-	X
Bit 5	X	-	Spread Spectrum Bit13	RW	-	-	X
Bit 4	X	-	Spread Spectrum Bit12	RW	-	-	X
Bit 3	X	-	Spread Spectrum Bit11	RW	-	-	X
Bit 2	X	-	Spread Spectrum Bit10	RW	-	-	X
Bit 1	X	-	Spread Spectrum Bit9	RW	-	-	X
Bit 0	X	-	Spread Spectrum Bit8	RW	-	-	X

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Table 3

PCI_STOP# I²C Control Table

PCI_STOP# (Pin 34)	Byte 0 Bit 3 Write Bit	Byte 0, Bit 3 Read Bit (Internal Status)
0	0	0
0	1	0
1	0	0
1	1	1`

Note: When this Byte 0, Bit 3 is low (0), all PCI clocks are stopped.

Table 4

CPUCLKT/C (2:0) Outputs I²C Control Table

CPU_STOP# (Pin 53)	Byte 1 Bit 3, 4, 5	CPUCLKT/C (2:0) Outputs
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Note: Individual CPUCLK outputs are controlled by Byte 1, Bit 3, 4, and 5.

Table 5

PCICLK_F (2:0) Outputs I²C Control Table

PCI_STOP# (Pin 34)	Byte 3 Bit 3, 4, 5	PCICLK (2:0) Outputs
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Note: Individual PCICLK outputs are controlled by Byte 3, Bit 3, 4, and 5.

Table 6

3V66 (5:2) I²C Control Table

CPU_STOP# (Pin 53)	Byte 5 Bit 5	3V66 (5:2)
0	0	Running
0	1	Stopped
1	0	Running
1	1	Running

Note: Activating Byte 5, Bit 5 will allow CPU_STOP# to control stop of pins 21, 22, 23, and 24.

Table 7

3V66 (1:0) I²C Control Table

CPU_STOP# (Pin 53)	Byte 5 Bit 4	3V66 (1:0)
0	0	Running
0	1	Stopped
1	0	Running
1	1	Running

Note: Activating Byte 5, Bit 4 will allow CPU_STOP# to control stop of pins 33 and 35.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +90°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz	229		280	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz	220		280	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=5 mA			45	mA
Input Frequency	F_i	V_{DD} = 3.3 V				MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	30	33	pF
PWRSAVE Stabilization[1,2]	T_{PWRSV}	From Assertion of PWRSAVE# to 1st clock.			1.8	ms
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.			1.8	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

Electrical Characteristics - CPUCLKT/C

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Voltage High	VHigh	Statistical measurement on single ended	660		850	mV
Voltage Low	VLow	signal using oscilloscope math function.	-150		150	
Max Voltage	Vovs	Measurement on single ended signal			1150	mV
Min Voltage	Vuds	using absolute value.	-450			
Crossing Voltage (abs)	Vcross(abs)		250		550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps
Rise Time Variation	d-t_r				125	ps
Fall Time Variation	d-t_f				125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%
Skew	t_{sk3}	V_T = 50%			100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%			150	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66			250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps
USB to DOT Skew	t_{sk1}[1]	V_T = 1.5 V (0 OR 180 degrees)			1	ns
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			1000	ps

[1]Guaranteed by design, not 100% tested in production.

General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

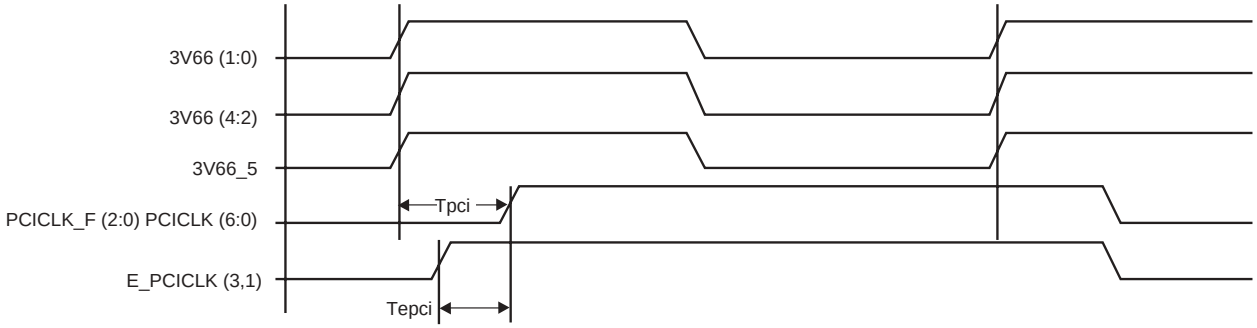
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
	X Byte	Beginning Byte N
ACK		
		O
O		O
O		O
O		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Un-Buffered Mode 3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1_VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group to Group Skews at Common Transition Edges: Unbuffered Mode

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66 to PCI[1,2]	$S_{3V66-PCI}$	3V66 (5:0) leads 33MHz PCI	1.5	2.55	3.5	ns

[1]Guarenteed by design, not 100% tested in production.

[2]500ps Tolerance

E_PCICLK to PCICLK Skews

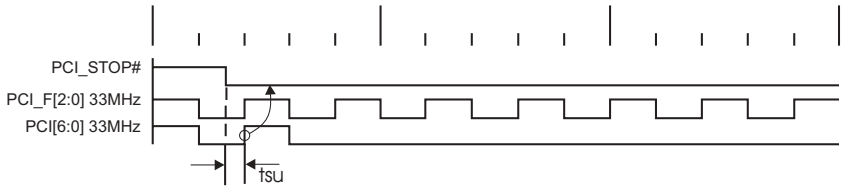
GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
E_PCICLK to PCICLK[1]	$T_{E\_PCI-PCI1}$	E_PCICLK1 (pin 11)=0 E_PCICLK3 (pin 13)=1	0.3	0.5	0.7	ns
	$T_{E\_PCI-PCI2}$	E_PCICLK1 (pin 11)=1 E_PCICLK3 (pin 13)=0	0.8	1.0	1.2	ns
	$T_{E\_PCI-PCI3}$	E_PCICLK1 (pin 11)=1 E_PCICLK3 (pin 13)=1	1.3	1.5	1.7	ns

[1]Guaranteed by design, not 100% tested in production.

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

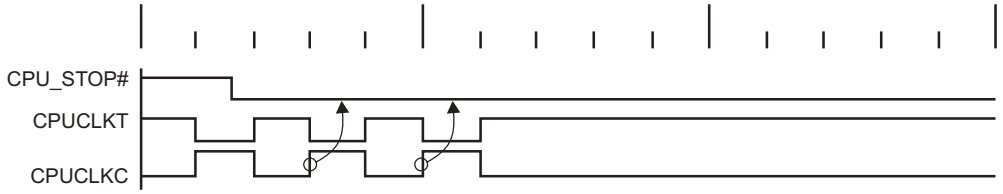
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition. When the I^2C Bit 6 of Byte 1 is programmed to '0' the final state of the stopped CPU signals is CPU = High and CPU# = Low. There is to be no change to the output drive current values. The CPU will be driven high with a current value equal to (Mult 0 'select') x (Iref), the CPU# signal will not be driven . When the I^2C Bit 6 of Byte 1 is programmed to '1' then final state of the stopped CPU signals is Low, both CPU and CPU# outputs will not be driven.

Assertion of CPU_STOP# Waveforms



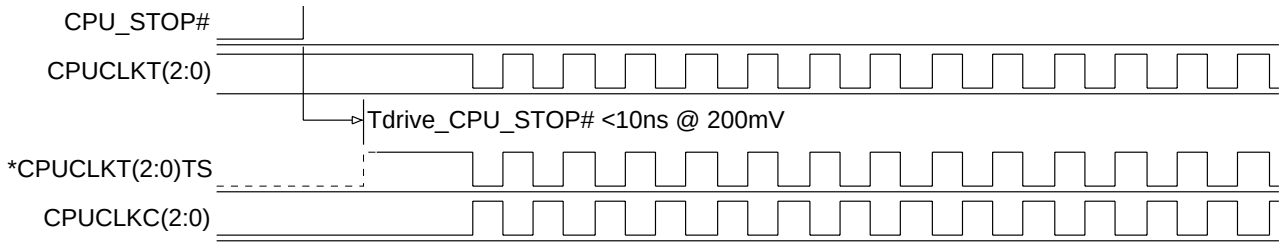
CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float

CPU_STOP# - De-assertion (transition from logic "0" to logic "1")

All CPU outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is to be defined to be between 2 - 6 CPU clock periods (2 clocks are shown). If the I2C Bit 6 of Byte 1 is programmed to "1" then the stopped CPU outputs will be driven High within 10 nS of CPU_Stop# de-assertion.

De-assertion of CPU_STOP# Waveforms

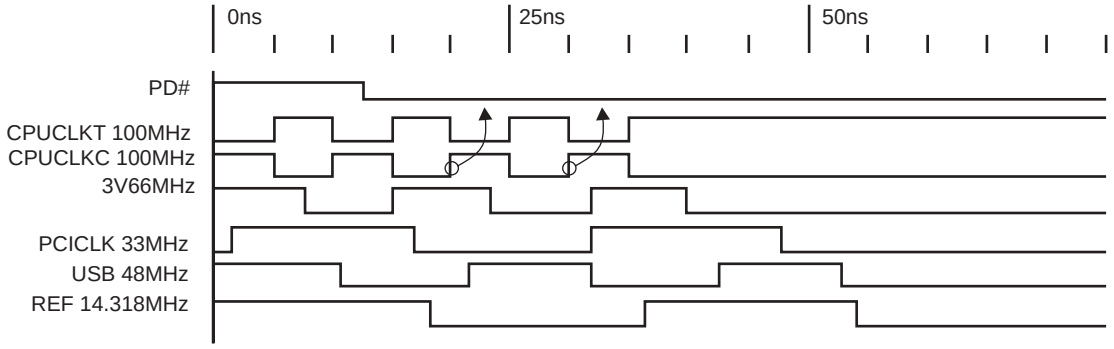


*Signal TS is CPUCLKT in Tri-State mode

PD# - Assertion (transition from logic "1" to logic "0")

When PWRDWN# is sampled low by two consecutive rising edges of CPU clock, then all clock outputs except CPU clocks must be held low on their next high to low transitions. When the I2C Bit 6 of Byte 0 is programmed to '0' CPU clocks must be held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# undriven. If Bit 6 of Byte 0 is '1' then both CPU and CPU# are undriven. Note the example below shows CPU = 133 MHz and Bit 6 of Byte 0 = '0', this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200 MHz.
Due to the state if the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms

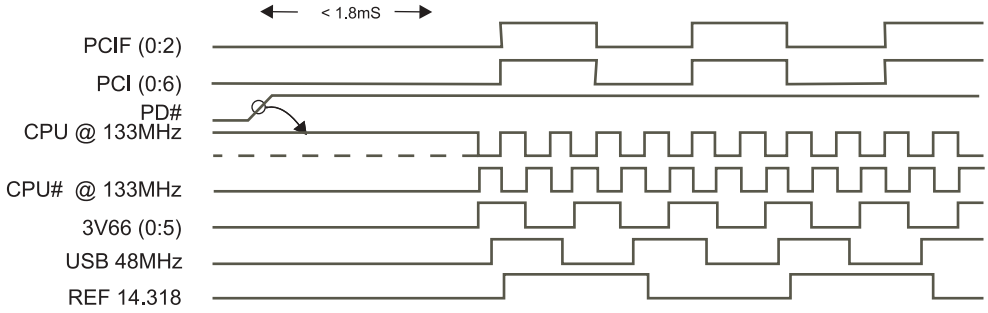


PD# Functionality

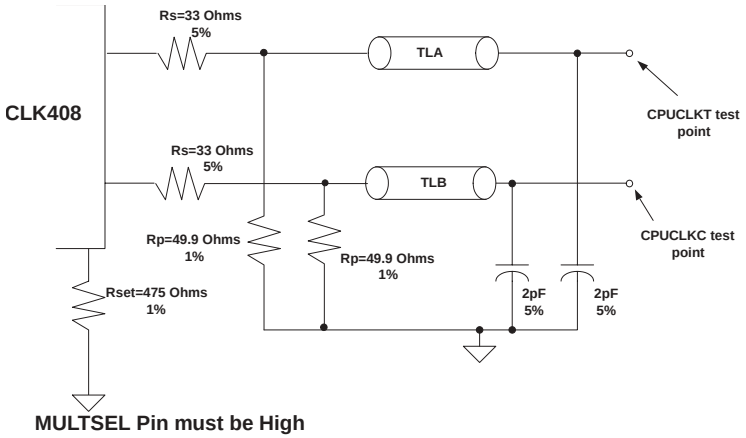
PD#	CPUCLKT	CPUCLKC	3V66	PCICLK_F PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	33MHz	48MHz
0	iref * Mult	Float	Low	Low	Low

Power Down De-Assertion Mode

The power-up latency needs to be less than 1.8mS. this is the time from the de-asseration of the powerdown of the ramping of the power supply until the time that stable clocks are output from the clock chip. If the I^2C Bit 6 of Byte 0 is programmed to "1" then the stopped CPU outputs will be driven high within 3 nS of PD# de-asseration.



Test Configuration Diagram



MULTSEL Pin must be High

CPU 0.7V Configuration test load board termination

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

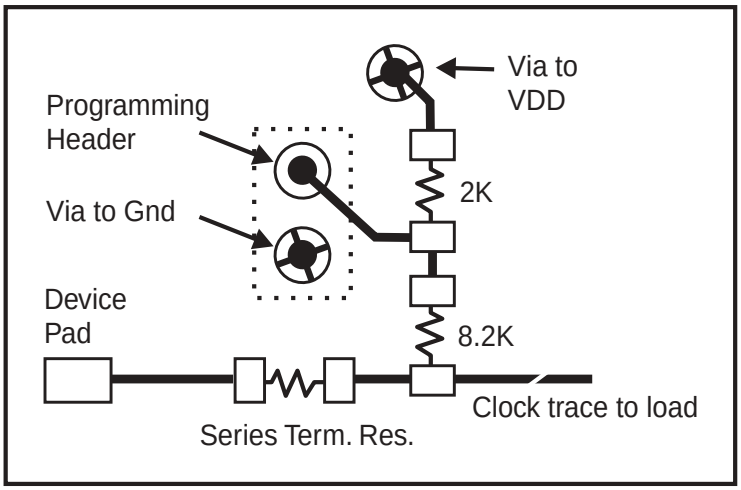
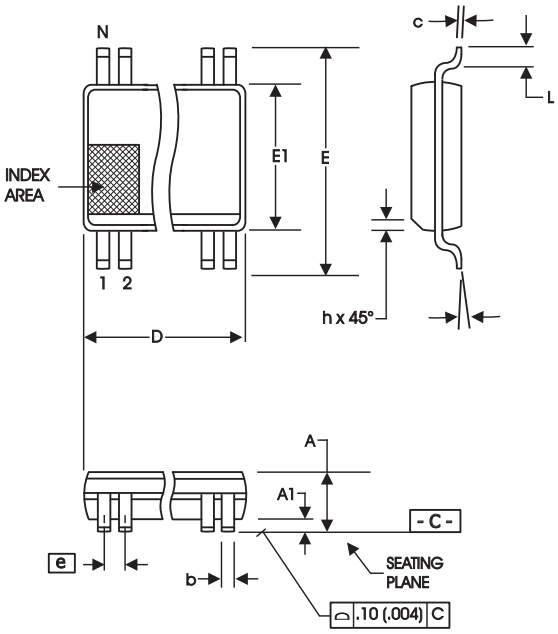


Fig. 1



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

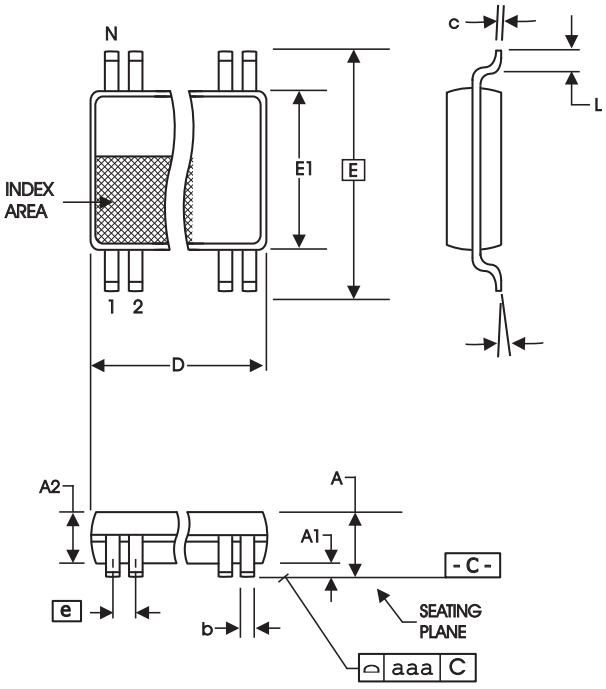
ICS950813yFT

Example:

ICS95 XXXX y F - T

- **Designation for tape and reel packaging**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

0708—10/10/02



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

Ordering Information

ICS950813yGT

Example:

ICS95 XXXX y G - T

- **Designation for tape and reel packaging**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

0708—10/10/02