PM7351

S/UNI™-VORTEX

S/UNI-VORTEX

OCTAL SERIAL LINK MULTIPLEXER

DATA SHEET

RELEASED

ISSUE 5: MARCH 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
Issue 5	March 2000	Changes marked with side bars. Incorporated errata items and updated data sheet for Production Release. Updated A.C. Timing Characteristics tH_{RCLK} and tH_{TCLK}. Updated D.C. Characteristics R_{IN} and V_{ODM} in.
Issue 4	January 2000	Changes marked with side bars. Matches functionality of PM7351 Rev B
Issue 3	June 1999	Changed the confidentiality notices for the document's public release.
Issue 2	April 1999	Changes in all areas from Issue 1. Matches functionality of product PM7351-BI, Rev A
Issue 1	May ,1998	Preliminary Document

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1 FEATURES

- Integrated analog/digital device that interfaces a high speed parallel bus to 8 bidirectional data streams, each transported over a high speed Low Voltage Differential Signal (LVDS) serial link.
- Works with its sister device, the S/UNI-DUPLEX, to satisfy a full set of system level requirements for backplane interconnect:
    - Transports user data by providing the inter-card data-path.
    - Inter-processor communication by providing an integrated inter-card control channel.
    - Exchanges flow control information (back-pressure) to prevent data loss.
    - Provides embedded command and control signals across the backplane: system reset, error indications, protection switching commands, etc.
    - Clock/timing distribution (system clocks as well as reference clocks such as 8 kHz timing references).
    - Fault detection, redundancy, protection switching, and inserting/removing cards while the system is running (hot swap).
- Each S/UNI-VORTEX Interfaces to 8 S/UNI-DUPLEX devices (via the LVDS links) to create a point-to-multipoint serial backplane architecture.
- Up to 16 S/UNI-VORTEX devices (interfacing to a maximum of 128 S/UNI-DUPLEXs) can reside on a single system bus.
- In the LVDS receive direction: accepts cell streams from the 8 LVDS links, multiplexing them into a single cell stream which is presented to the system bus as a single Utopia L2 compatible PHY.
- In the LVDS transmit direction: receives cell streams from the bus master, and routes the cells to the appropriate serial link.
- Cell read/write to the 8 LVDS links is available via the microprocessor port. Provides optional hardware assisted CRC32 calculation across cells to create an embedded inter-processor communication channel across the LVDS links.
- Optionally routes the embedded control channels from the 8 link's to/ from the system bus.

- Under software control, the 8 LVDS links can be individually marked active or standby. This is used by the far end S/UNI-DUPLEXs to implement 1:1 protected systems.
- Error monitoring and cell counting on all links.
- Requires no external memories.
- Low power 3.3V CMOS technology.
- Standard 5 pin P1149 JTAG port.
- 304 ball SBGA, 31mm x 31mm.

2 APPLICATIONS

- Single shelf or multi-shelf Digital Subscriber Loop Access Multiplexer (DSLAM).
- ATM, frame relay, IP switch.
- Multiservice access multiplexer.
- Universal Mobile Telecommunication System (UMTS) wireless base stations.
- UMTS wireless base station controllers.
- Multi-shelf access concentrators.

3 REFERENCES

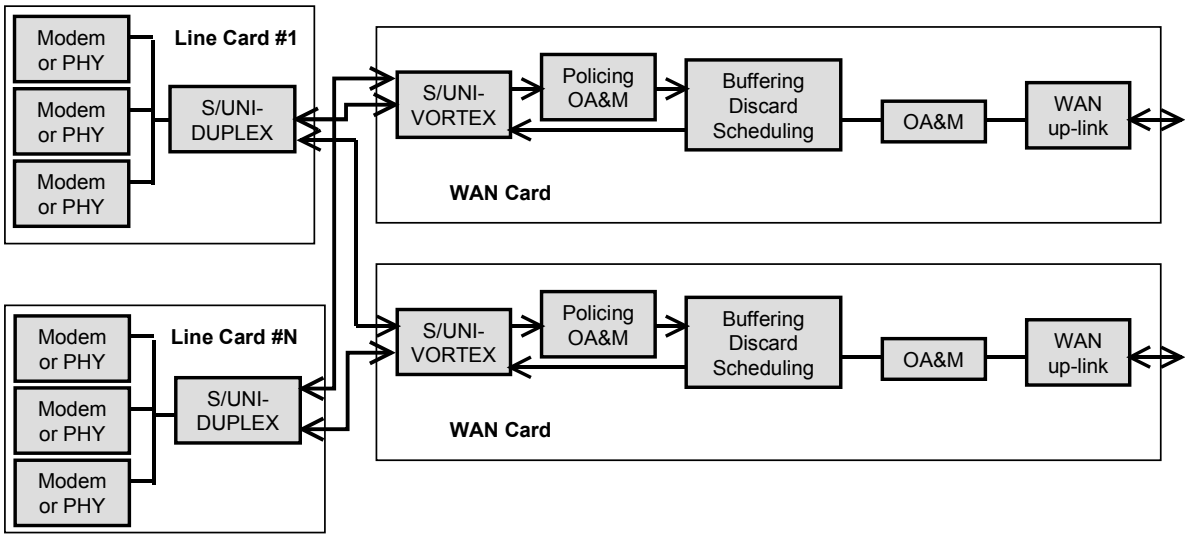
- PMC-Sierra; “Saturn Compatible Interface For ATM PHY Layer And ATM Layer Devices, Level 2”; PMC-940212; Dec. 8, 1995
- PMC-Sierra; “Saturn Interface Specification And Interoperability Framework For Packet And Cell Transfer Between Physical Layer And Link Layer Devices”, PMC-980902, Draft
- ATM Forum, “Universal Test & Operations PHY Interface for ATM (UTOPIA), Level 2”, Version 1.0, af-phy-0039.000, June 1995
- ITU-T Recommendation I.432.1, “B-ISDN user-network interface – Physical layer specification: General characteristics”, 08/96
- American National Standard for Telecommunications, “Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface”, ANSI T1.413-1998, November, 1998

4 APPLICATION EXAMPLES

When designing communication equipment such as access switches, multiplexers, wireless base stations, and base station controllers the equipment architect is faced with a common problem: how do I efficiently connect a large number of lower speed ports to a small number of high speed ports? Typically, a number of line-side ports (analog modems, xDSL modems ATM PHYs, or RF modems) are terminated on each line card. Numerous line cards are then slotted into one or more shelves and backplane traces or inter-shelf cables are used to connect the line cards to a centralized (often 1:1 protected) common card, hereafter referred to as the core card. The core card normally includes one or more high speed WAN up-link ports that transport traffic to and from a high speed broadband network.

A block diagram of a 1:1 redundant system is shown in Fig. 1.

Fig. 1 Typical Target Application



In this type of equipment the majority (perhaps all) user traffic goes from WAN port to line port, or from line port to WAN port. Although the individual ports on the line cards are often relatively low speed interfaces such as T1, E1, or xDSL, there may be many ports per line card and many line cards per system, resulting in hundreds or even thousands of lines terminating on a single WAN up-link. In the upstream direction (from line card to WAN up-link), the equipment must have capacity to buffer and intelligently manage bursts of upstream traffic simultaneously from numerous line cards.

In the downstream direction the equipment must handle a similar issue, the “big pipe feeding little pipe” problem. When a large burst of traffic destined for a single line port is received at the high speed WAN port it must be buffered and managed as it queues up waiting for the much lower speed line port to clear.

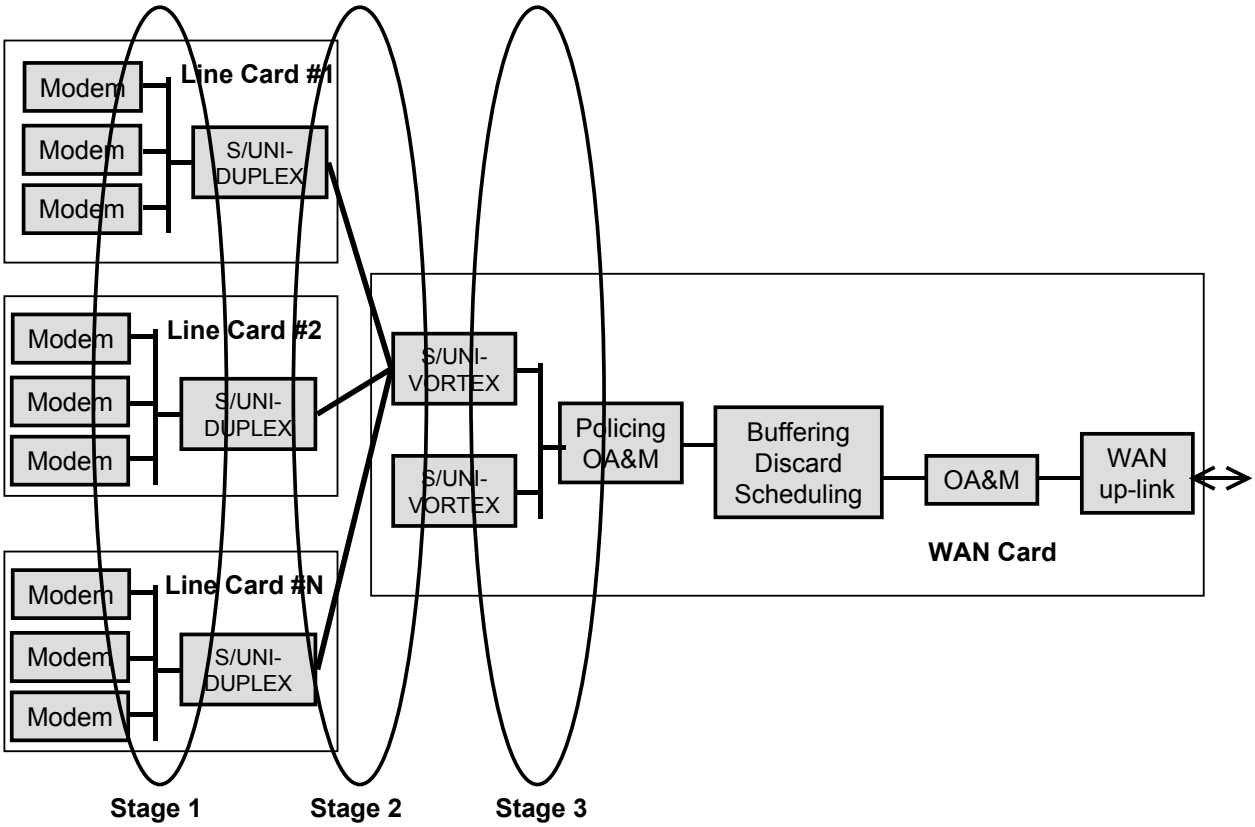
The line cards are always the most numerous cards in this type of equipment. An individual line card, even if it terminates a few dozen low speed ports, does not generate or receive enough traffic to justify putting complex buffering and traffic management devices on it. The ideal architecture has low cost “dumb” line cards and a feature rich, “smart” core card. In order to enhance fault tolerance, the architecture should also inherently support 1:1 protection using a redundant core card and WAN up-link without significantly increasing line card complexity.

A system architecture that keeps buffering and traffic management off the line card will typically exhibit the following features:

1. Connection setup is simpler both in terms of programming and during execution because there is minimal or no requirement for line card intervention during the connection setup process.
2. In-service feature upgrades are simpler because feature complexity is limited to the common equipment.
3. Component costs are reduced, while system reliability increases due to reduced component count.

In this type of architecture there are often three stages of signal concentration or multiplexing, as shown in Fig. 2.

Fig. 2 Three Stage Multiplex Architecture



The first stage resides on the line card and spans only those ports physically terminated by that card. Since it is confined to a single card, this first stage of multiplexing readily lends itself to a simple parallel bus based multiplex topology. The second stage of concentration occurs between the core card(s) and the line cards, including line cards that are on a separate shelf. This second stage is best served by a redundant serial point-to-point technology. The third stage of multiplexing is optional and resides on the core card. This third stage is used in systems with a large number of line cards that require several S/UNI-VORTEX devices to terminate the second stage of aggregation. Since the third stage of aggregation is confined to the core card, it lends itself readily to a parallel bus implementation. This three stage approach is implemented directly by the S/UNI-VORTEX and its sister device, the S/UNI-DUPLEX.

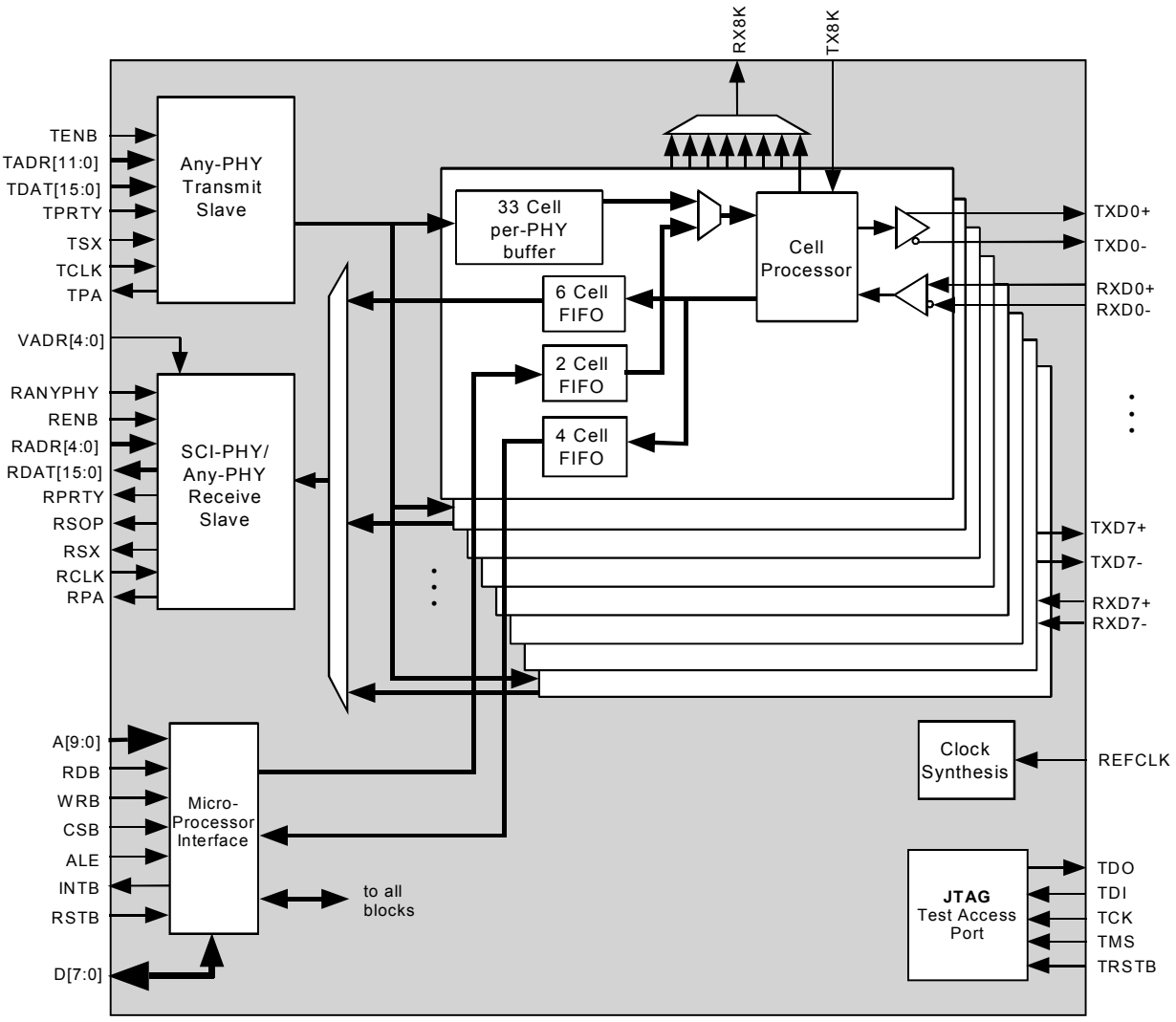
The S/UNI-DUPLEX acts as the line card's bus master. It implements the first stage of multiplexing by routing traffic from the PHYs and transmitting the traffic simultaneously over two high speed (up to 200 Mbps) serial 4-wire LVDS links. One serial link attaches to the active core card, the other to the standby core

card.[1] In the downstream direction the S/UNI-DUPLEX demultiplexes traffic from the active core card's LVDS serial link and routes this traffic to the appropriate PHYs. If the active core card (or its LVDS link) should fail, protection switching commands embedded in the spare LVDS link will direct the S/UNI-DUPLEX to start receiving its traffic from this spare link.

The S/UNI-VORTEX resides on the core card and terminates up to 8 LVDS links connected to 8 S/UNI-DUPLEX devices. The S/UNI-VORTEX implements the second stage of multiplexing. More than one S/UNI-VORTEX will be required if more than 8 links are required – as will be the case for a system with more than 8 line cards. The S/UNI-VORTEX device(s) share a high speed parallel bus with the core card's traffic management and OA&M layers, as implemented by devices such as PMC-Sierra's S/UNI-APEX and the S/UNI-ATLAS. This is the third stage of multiplexing.

[1] A single core card implementation is also supported, of course.

5 BLOCK DIAGRAM



6 DESCRIPTION

The PM7351 S/UNI-VORTEX is a monolithic integrated circuit typically used with its sister device, the S/UNI-DUPLEX, to implement a point-to-point serial backplane interconnect architecture.

Up to sixteen S/UNI-VORTEX devices can reside on a common cell processing card along side a traffic management device. The traffic management device exchanges cells with the S/UNI-VORTEX via 16-bit SCI-PHY or Any-PHY interfaces. Flow control is effected across this interface via cell available signals generated by the S/UNI-VORTEX. In the downstream direction, the availability of a buffer for each logical channel can be polled by the traffic management device. In the upstream direction, an indication is provided whether there is one or more cells queued in the S/UNI-VORTEX for transfer.

Each S/UNI-VORTEX can be connected to eight line cards via 100 to 200 Mb/s serial links. Each upstream link has its own queue. If a queue becomes nearly full, a flow control indication is sent downstream. In the downstream direction, each logical channel has a dedicated cell buffer to avoid head of line blocking. The serialization of cells from the cell buffers is throttled by flow control information sent from the line card via the upstream high-speed link.

A microprocessor port provides access to internal configuration and monitoring registers. The port may also be used to insert and extract cells in support of a control channel.

LVDS INTERFACES, BOTH DIRECTIONS

- 8 independent 4-wire LVDS serial transceivers each operating at up to 200 Mbps across PCB or backplane traces, or across up to 10 meters of 4-wire twisted pair cabling for inter-shelf communications.

- Usable bandwidth (excludes system overhead) of 186 Mbps per direction per LVDS link.

- Full integrated LVDS clock synthesis and recovery. No external analog components are required.

LVDS RECEIVE DIRECTION

- Weighted round robin multiplex of cell streams from the 8 LVDS links into a single cell stream which is transferred to the parallel bus under control of the bus master.

- LVDS link and S/UNI-VORTEX identifiers are added to each cell (along with the PHY identifier already added by S/UNI-DUPLEX) for use by ATM layer to identify the cell source.

- Back-pressure sent to far end to prevent overflow of receiver FIFO.

LVDS TRANSMIT DIRECTION

- Per PHY and microprocessor port back-pressure used on each of the 8 links to prevent overflow of downstream buffers.

- Device polling: provides Utopia-like TCA status for 264 PHYs (includes 8 control channels) based on back-pressure from the LVDS links.

- Cell transfer: Bus master adds a PHY address to each cell via a 12 bit identifier. S/UNI-Vortex decodes and accepts cells for its links based on software configured base addresses.

PARALLEL BUS INTERFACE:

- Both directions: 16 bit wide, 50 MHz max clock rate, bus slave.

- Cells transferred to the bus: Utopia L2 compatible with optional expanded length cells. Appears as single PHY, with a cell prepend identifying the source PHY ID of each cell. Alternatively, Utopia L2 compliance is supported by placing the PHY ID inside the UDF/HEC fields of a standard ATM cell.

- Cells received from the bus: The Any-PHY bus is similar to Utopia L2 but with optional expanded length cells and expanded addressing capabilities. The S/UNI-VORTEX appears to the bus master as a 264 port multi-PHY device (8 links, each with 32 PHYs & communication channel). PHY address is added as cell prepend or optionally in HEC/UDF field when standard length cells are desired.

MICROPROCESSOR INTERFACE

- 8 bit data bus, 8 bit address bus.
- Provides read/write access to all configuration and status registers.
- Provides CRC32 calculation and cell transfer registers to support an embedded microprocessor to microprocessor communication channel over the LVDS link.

7 PIN DIAGRAM

The S/UNI-VORTEX is packaged in a 304-ball enhanced ball grid array (BGA) package having a body size of 31 mm by 31 mm and a ball pitch of 1.27 mm.

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VDD	VSS	nc	RDAT15	RENB	VSS	RADR2	VSS	VADR2	RX8K	TDI	VSS	nc	nc	nc	VSS	nc	VSS	nc	nc	nc	VSS	VDD	A
B	VSS	VDD	VSS	nc	RPRTY	RSOP	RADR1	RADR4	VADR0	VADR4	TMS	nc	nc	nc	nc	nc	nc	nc	nc	nc	VSS	VDD	VSS	B
C	RDAT11	VSS	VDD	nc	RDAT14	RPA	RSX	RADR3	RANYPHY	VADR3	TRSTB	TDO	nc	nc	nc	nc	QAVS	nc	nc	TAVS	VDD	VSS	TXDP0	C
D	RDAT8	RDAT10	RDAT12	VDD	RDAT13	VDD	RCLK	RADR0	VDD	VADR1	TCK	VDD	nc	nc	VDD	QAVD	nc	VDD	TAVD	VDD	RXDP0	TXDN0	TXDP1	D
E	RDAT4	RDAT7	RDAT9	BIAS																RXDN0	TAVS	TXDN1	TXDP2	E
F	VSS	RDAT3	RDAT6	VDD																VDD	RXDP1	TXDN2	VSS	F
G	RDAT0	nc	RDAT2	RDAT5																RXDN1	RXDP2	TAVD	TAVS	G
H	VSS	nc	nc	RDAT1																RXDN2	TAVD	RAVD	VSS	H
J	TX8K	nc	nc	VDD							PM7351									VDD	RAVS	TAVD	TAVS	J
K	TDAT15	nc	nc	nc																ATP1	ATP0	TXDN3	TXDP3	K
L	TDAT12	TDAT13	nc	TDAT14							S/UNI-VORTEX									RAVD	CAVS	RXDN3	RXDP3	L
M	VSS	TDAT11	TDAT10	VDD																VDD	CAVD	CAVS	VSS	M
N	TDAT9	TDAT8	TDAT7	TDAT6							BOTTOM VIEW									RAVS	CAVD	TXDN4	TXDP4	N
P	TDAT5	TDAT4	TDAT3	TDAT1																RES	RESK	RXDN4	RXDP4	P
R	TDAT2	TDAT0	TCLK	VDD																VDD	RAVS	TAVS	TAVD	R
T	VSS	TPRTY	TSX	TADR11																RXDN5	TAVS	RAVD	VSS	T
U	TPA	TENB	TADR10	TADR7																RXDN6	RXDP5	TAVD	TAVD	U
V	VSS	TADR9	TADR6	VDD																VDD	RXDP6	TXDN5	VSS	V
W	TADR8	TADR5	TADR3	BIAS																RXDN7	TAVS	TXDN6	TXDP5	W
Y	TADR4	TADR2	TADR0	VDD	A0	VDD	A7	RDB	VDD	D3	INTB	VDD	nc	nc	VDD	QAVD	nc	VDD	TAVD	VDD	RXDP7	TXDN7	TXDP6	Y
AA	TADR1	VSS	VDD	nc	A3	A6	CSB	RSTB	D1	D5	nc	nc	nc	nc	nc	nc	QAVS	nc	nc	TAVS	VDD	VSS	TXDP7	AA
AB	VSS	VDD	VSS	A2	A5	A9	ALE	D0	D2	D6	REFCLK	nc	nc	nc	nc	nc	nc	nc	nc	nc	VSS	VDD	VSS	AB
AC	VDD	VSS	A1	A4	A8	VSS	WRB	VSS	D4	D7	nc	VSS	nc	nc	nc	VSS	nc	VSS	nc	nc	nc	VSS	VDD	AC
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8 PIN DESCRIPTION

Ball Name	Type	Ball No.	Function
			High Speed LVDS Links
RXD0+ RXD0- RXD1+ RXD1- RXD2+ RXD2- RXD3+ RXD3- RXD4+ RXD4- RXD5+ RXD5- RXD6+ RXD6- RXD7+ RXD7-	Diff. LVDS Input	D3 E4 F3 G4 G3 H4 L1 L2 P1 P2 U3 T4 V3 U4 Y3 W4	The high-speed receive data (RXD0+/- - RXD7+/-) inputs present NRZ data from a serial backplane. These are truly differential inputs offering superior common-mode noise rejection. They have sufficient sensitivity and common-mode range to support LVDS signals. These inputs are high-impedance. An external resistor must be connected between the two pins of a signal pair to terminate the transmission line. D.C. or A.C. coupling may be used depending on the application.
TXD0+ TXD0- TXD1+ TXD1- TXD2+ TXD2- TXD3+ TXD3- TXD4+ TXD4- TXD5+ TXD5- TXD6+ TXD6- TXD7+ TXD7-	Diff. LVDS Output	C1 D2 D1 E2 E1 F2 K1 K2 N1 N2 W1 V2 Y1 W2 AA1 Y2	The transmit differential data (TXD0+/- -TXD7+/-) outputs present NRZ encoded data to a serial backplane. These outputs are open drain current sinks which interface directly with twisted-pair cabling or board interconnect. D.C. or A.C. coupling may be used depending on the application. As current sinks, these outputs must see a 100Ω reflected impedance between the pins in a signal pair to produce correct LVDS signal levels.

Ball Name	Type	Ball No.	Function
REFCLK	Input	AB13	The reference clock input (REFCLK) must provide a jitter-free reference clock. It is used as the reference clock by both clock recovery and clock synthesis circuits. Any jitter below 1 MHz is transferred directly to the TXDn+/- outputs. The high speed serial interface bit rate is eight times the REFCLK frequency.
RES RESK	Analog	P4 P3	A 4.75kΩ ±1% resistor must be connected between these two balls to achieve the correct LVDS output signal levels.
ATP0 ATP1	Analog	K3 K4	The Analog Test Points (ATP) are provided for production test purposes. In mission mode they are high impedance and should be connected to ground.
TX8K	Input	J23	The transmit 8 kHz timing reference (TX8K) input allows a traceable signal to be transmitted to the far end of the high-speed serial links via TXD0+/- through TXD7+/-. A rising edge on TX8K is encoded in the next cell transmitted. Although TX8K is targeted at a typical need of transporting an 8 kHz signal, its frequency is not constrained to 8 kHz. Any frequency less than the cell rate is permissible.
RX8K	Output	A14	The receive 8 kHz timing reference (RX8K) output presents the timing extracted from one of the receive high-speed serial links. The rising edge of RX8K is accurate to the nearest byte boundary of the high-speed serial link; therefore, a small amount of jitter is present. At a link rate of 155.52 Mb/s, the jitter is 63ns peak-to-peak. Pulses on RX8K are always 16 high-speed serial link bit periods wide (two REFCLK periods).

Ball Name	Type	Ball No.	Function
			Upstream (Receive) Bus
RANYPHY	Input	C15	The Receive Any-PHY configuration input determines the protocol of the upstream cell interface. If RANYPHY is logic low, the interface complies to the SCI-PHY specification. As such, all outputs have a single cycle latency. If RANYPHY is logic high, the interface complies to the Any-PHY specification. Relative to SCI-PHY, all outputs have an additional cycle of latency. RANYPHY is an asynchronous input and is expected to be held static.
RCLK	Input	D17	The Receive FIFO clock (RCLK) is used to read words from the S/UNI-VORTEX upstream cell buffer. RCLK must cycle at a 52 MHz or lower instantaneous rate. RSOP, RPA, RPRTY and RDAT[15:0] are updated on the rising edge of RCLK. RENB and RADR[4:0] are sampled on the rising edge of RCLK.
RPA	Output	C18	The RPA signal indicates whether at least one cell is queued for transfer. Upon sampling a RADR[4:0] value that equals the value on VADR[4:0], the S/UNI-VORTEX drives the RPA with the cell availability status immediately if RANYPHY is logic low. If RANYPHY is logic high, RPA has an additional cycle of latency. RPA will be a one if at least one entire cell is available. RPA is high-impedance when not polled. RPA is updated on the rising edge of RCLK.

Ball Name	Type	Ball No.	Function
RENB	Input	A19	The active low read enable (RENB) output is used to initiate the transfer of cells from the S/UNI-VORTEX to a traffic management device. When RENB is sampled low and the S/UNI-VORTEX has been selected, a word is output on bus RDAT[15:0]. Selection occurs when RENB is last sampled high if the RADR[4:0] value equals the state of VADR[4:0]. RENB must be low for between 27 and 29 cycles to transfer an entire cell depending on whether the cell contains prepended words or the H5/UDF word. If RANYPHY is logic low, valid data is driven immediately upon sampling RENB low. If RANYPHY is logic high, the RSX, RSOP, RDAT[15:0] and RPRTY outputs have an additional cycle of latency. It is permissible to pause a cell transfer by deasserting RENB high. If RANYPHY is logic low, the S/UNI-VORTEX's address must be presented on RADR[4:0] the last cycle RENB is high to reselect the device. If RANYPHY is logic high, the cell transfer resumes unconditionally when RENB is asserted low again. In either case, a cell transfer must be completed before another device on the bus is selected. The Any-PHY protocol supports autonomous deselection. If RANYPHY is logic high, the outputs become high impedance after the last word of a cell is transferred until the S/UNI-VORTEX is reselected. If RANYPHY is logic low, a subsequent cell is transferred (provided one is available) if RENB is held low beyond the end of a cell. When RENB is sampled high or the S/UNI-VORTEX is not selected, no read is performed and outputs RDAT[15:0], RPRTY, RSX and RSOP become high impedance. The RENB input is sampled on the rising edge of RCLK.

Ball Name	Type	Ball No.	Function
RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	Input	B16 C16 A17 B17 D16	The RADR[4:0] signals are used to address up to sixteen S/UNI-VORTEX devices for the purposes of polling and selection for cell transfer. When a RADR[4:0] value is sampled that equals the state of VADR[4:0], the RPA output is driven to indicate whether a cell is available for transfer. If RANYPHY is logic high, RPA has an additional cycle of latency. If the RADR[4:0] value equals the state of VADR[4:0] when the RENB is last sampled high, the S/UNI-VORTEX will initiate a cell transfer. If RANYPHY is logic low, the device must be reselected to resume a cell transferred that has been halted by deasserting RENB high. The RADR[4:0] bus is sampled on the rising edge of RCLK.
VADR[4] VADR[3] VADR[2] VADR[1] VADR[0]	Input	B14 C14 A15 D14 B15	The device identification address (VADR[4:0]) inputs are the most-significant bits of the upstream polling address space which this S/UNI-VORTEX occupies. When the VADR[4:0] inputs match the value sampled on RADR[4:0] inputs, the S/UNI-VORTEX drives RPA to indicate the existence of queued cells. Otherwise, RPA is high impedance. VADR[4:0] are expected to be held static.

Ball Name	Type	Ball No.	Function
RSOP	Output	B18	The Receive Start of Packet (RSOP) marks either the first or second word of the cell on the RDAT[15:0] bus. When RSOP is high and RANYPHY is low, the first word of the cell structure is present on the RDAT[15:0] stream. When RSOP and RANYPHY are both high, the second word of the cell structure is present on the RDAT[15:0] stream. RSOP is updated on the rising edge of RCLK and considered valid only when the S/UNI-VORTEX device was selected after the polling process and the RENB signal is sampled low. If RANYPHY is logic low RSOP is driven immediately upon sampling RENB low, but it has an additional cycle latency when RANYPHY is logic high. RSOP becomes high impedance upon sampling RENB high or if the S/UNI-VORTEX device is not selected for transfer. When RANYPHY is high, autonomous deselection occurs after the last word of a cell resulting in setting RSOP high-impedance until reselection.
RSX	Output	C17	The Receive Start of Transfer (RSX) is only active when the RANYPHY input is logic high. When RANYPHY is logic low, RSX is low during cell transfers or high-impedance otherwise. RSX marks the start of the cell on the RDAT[15:0] bus. When RSX is high, the first word of the cell structure is present on the RDAT[15:0] stream. RSX is updated on the rising edge of RCLK and considered valid only when the RENB signal was sampled low in the previous cycle and the S/UNI-VORTEX device was selected after the polling process. RSX becomes high impedance (with a cycle latency) upon sampling RENB high or if the S/UNI-VORTEX device is not selected for transfer. When RANYPHY is high, autonomous deselection occurs after the last word of a cell resulting in setting RSX high-impedance until reselection.

Ball Name	Type	Ball No.	Function
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	A20 C19 D19 D21 C23 D22 E21 D23 E22 F21 G20 E23 F22 G21 H20 G23	The receive cell data bus (RDAT[15:0]) carries the ATM cell words that have been read from the S/UNI-VORTEX internal cell buffers. The RDAT[15:0] bus is updated on the rising edge of RCLK and considered valid only when the S/UNI-VORTEX device was selected after the polling process and the RENB signal is sampled low. If RANYPHY is logic low RDAT[15:0] is driven immediately upon sampling RENB low, but it has an additional cycle latency when RANYPHY is logic high. RDAT[15:0] becomes high impedance upon sampling RENB high or if the S/UNI-VORTEX device is not selected for transfer. When RANYPHY is high, autonomous deselection occurs after the last word of a cell resulting in setting RDAT[15:0] high-impedance until reselection.
RPRTY	Output	B19	The Receive Parity (RPRTY) signal completes the parity (programmable for odd or even parity) of the RDAT[15:0] bus. The RPRTY signal is updated on the rising edge of RCLK and is considered valid only when the S/UNI-VORTEX device was selected after the polling process and the RENB signal is sampled low. If RANYPHY is logic low RPRTY is driven immediately upon sampling RENB low, but it has an additional cycle latency when RANYPHY is logic high. RPRTY becomes high impedance upon sampling RENB high or if the S/UNI-VORTEX device is not selected for transfer. When RANYPHY is high, autonomous deselection occurs after the last word of a cell resulting in setting RPRTY high-impedance until reselection.

Ball Name	Type	Ball No.	Function
Downstream (Transmit) Bus			
TCLK	Input	R21	The transmit FIFO clock (TCLK) is used to transfer cells from a traffic scheduler device to the internal downstream cell buffers. TCLK must cycle at a 52 MHz or lower instantaneous rate. TSX, TENB, TADR[11:0], TPRTY and TDAT[15:0] are sampled on the rising edge of TCLK. TPA is updated on the rising edge of TCLK.
TPA	Output	U23	The S/UNI-VORTEX indicates the availability of space in the FIFO associated with a logical channel when polled using the TADR[11:0] signals. The S/UNI-VORTEX will drive the TPA signal to the appropriate value during the second clock cycle following that in which a particular logical channel is addressed. When high, TPA indicates that the corresponding buffer segment is empty and a complete cell may be written. The buffer status for the particular logical channel involved in the transfer is updated immediately upon sampling the first word of the cell when the INADDUDF bit of the Downstream Cell Interface Configuration register is logic 0. When the INADDUDF bit is logic 1, the buffer status is stale until nine cycles after the cell transfer is completed; therefore, the master should refrain from polling that logical channel in the interim. TPA becomes high impedance when an address not matching the address space set by the Control Channel Base Address, Logical Channel Base Address and Logical Channel Address Range / Logical Channel Base Address MSB registers is sampled from the TADR[11:3] inputs. TPA is updated on the rising edge of TCLK.

Ball Name	Type	Ball No.	Function
TENB	Input	U22	The active low write enable (TENB) signal is used to indicate cell transfers to the internal cell buffers. The segment of the buffer associated with a particular logical channel is determined by the inband address in the prepended cell bytes. TENB is ignored if TSX is high. Upon the completion of a cell transfer, TENB may be held low because a cell transfer is only initiated by assertion of TSX. TENB must be low for 26 to 28 (depending on the inclusion of optional words) cycles to transfer an entire cell. TENB may be deasserted high at any time to pause a cell transfer. TENB is updated on the rising edge of TCLK.
TADR[11] TADR[10] TADR[9] TADR[8] TADR[7] TADR[6] TADR[5] TADR[4] TADR[3] TADR[2] TADR[1] TADR[0]	Input	T20 U21 V22 W23 U20 V21 W22 Y23 W21 Y22 AA23 Y21	The TADR[11:0] signals are used to address logical channels for the purposes of polling. Upon sampling a TADR[11:3] value within one of the address ranges set by the Control Channel Base Address, Logical Channel Base Address and Logical Channel Address Range / Logical Channel Base Address MSB registers, TPA will be driven to indicate the availability of the buffer segment addressed by TADR[4:0]. When TADR[11:3] does not match a programmed address range, TPA becomes high impedance. The TADR[11:0] bus is sampled on the rising edge of TCLK.
TSX	Input	T21	The transmit start of cell (TSX) indication signal marks the start of cell on the TDAT[15:0] data bus. When TSX is high, the first word of the cell structure is present on the TDAT[15:0] stream. TSX must be asserted for each cell. An interrupt may be generated if TSX is high during any word other than the expected first word of the cell structure. TSX is sampled on the rising edge of TCLK.

Ball Name	Type	Ball No.	Function
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	K23 L20 L22 L23 M22 M21 N23 N22 N21 N20 P23 P22 P21 R23 P20 R22	The transmit cell data bus (TDAT[15:0]) carries the ATM cell octets that are transferred to the internal cell buffer. The TDAT[15:0] bus is sampled on the rising edge of TCLK and is considered valid only when the TENB signal is asserted low or the TSX signal is asserted high.
TPRTY	Input	T22	The transmit parity (TPRTY) signal completes the parity (programmable for odd or even parity) of the TDAT[15:0] bus. A parity error is indicated by a status bit and a maskable interrupt. The TPRTY signal is sampled on the rising edge of TCLK and is considered valid only when the TENB signal is asserted or the TSX signal is asserted high.
Microprocessor Bus			
CSB	Input	AA17	The active-low chip select (CSB) signal is low during S/UNI-VORTEX register accesses. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	Y16	The active-low read enable (RDB) signal is low during S/UNI-VORTEX register read accesses. The S/UNI-VORTEX drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.

Ball Name	Type	Ball No.	Function
WRB	Input	AC17	The active-low write strobe (WRB) signal is low during S/UNI-VORTEX register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AC14 AB14 AA14 AC15 Y14 AB15 AA15 AB16	The bi-directional data bus D[7:0] is used during S/UNI-VORTEX register read and write accesses.
A[9]/TRS A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	AB18 AC19 Y17 AA18 AB19 AC20 AA19 AB20 AC21 Y19	The address bus A[9:0] selects specific registers during S/UNI-VORTEX register accesses. The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
RSTB	Input	AA16	The active-low reset (RSTB) signal provides an asynchronous S/UNI-VORTEX reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.
ALE	Input	AB17	The address latch enable (ALE) is active-high and latches the address bus A[9:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-VORTEX to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	OD Output	Y13	The active-low interrupt (INTB) signal goes low when a S/UNI-VORTEX interrupt source is active and that source is unmasked. The S/UNI-VORTEX may be enabled to report many alarms or events via interrupts. INTB becomes high impedance when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
JTAG Boundary Scan Port			

Ball Name	Type	Ball No.	Function
TCK	Input	D13	The test clock (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port. TCK has an integral pull-up resistor.
TMS	Input	B13	The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	A13	The test data input (TDI) signal carries test data into the S/UNI-VORTEX via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	C12	The test data output (TDO) signal carries test data out of the S/UNI-VORTEX via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.
TRSTB	Input	C13	The active-low test reset (TRSTB) signal provides an asynchronous S/UNI-VORTEX test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB must be connected to the RSTB input.
Power and Ground			
BIAS	Power	E20 W20	When tied to +5V, the BIAS inputs are used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When tied to +3.3V, the inputs and bi-directional inputs will only tolerate 3.3V level inputs.

Ball Name	Type	Ball No.	Function
VDD	Power	A1 B2 C3 D4 F4 J4 M4 R4 V4 AC1 AB2 AA3 Y4 Y6 Y9 Y12 Y15 Y18 AC23 AB22 AA21 Y20 V20 R20 M20 J20 F20 A23 B22 C21 D20 D18 D15 D12 D9 D6	The pad ring power (VDD) pins should be connected to a well-decoupled +3.3 V DC supply.

Ball Name	Type	Ball No.	Function
VSS	Ground	B1 C2 F1 H1 M1 T1 V1 AA2 AB1 AC2 AB3 AC6 AC8 AC12 AC16 AC18 AC22 AB21 AB23 AA22 V23 T23 M23 H23 F23 B23 C22 B21 A22 A18 A16 A12 A8 A6 A2 B3	The pad ring ground (VSS) pins should be connected to GND.
QAVD1 QAVD0	Analog Power	Y8 D8	Quiet Analog Power (QAVD1, QAVD0). QAVD1 and QAVD0 should be connected to analog +3.3 V.
QAVS1 QAVS0	Analog Power	AA7 C7	Quiet Analog Ground (QAVS1, QAVS0). QAVS1 and QAVS0 should be connected to analog GND.

Ball Name	Type	Ball No.	Function
CAVD	Analog Power	M3 N3	The power (CAVD) pins for the analog clock synthesis unit. These pins should be connected to analog +3.3V.
CAVS	Analog Ground	L3 M2	The ground (CAVS) pins for the analog clock synthesis unit. These pins should be connected to analog GND.
RAVD	Analog Power	H2 L4 T2	The power (RAVD) pins for the LVDS receivers. These pins should be connected to analog +3.3V.
RAVS	Analog Ground	J3 N4 R3	The ground (RAVS) pins for the LVDS receivers. These pins should be connected to analog GND.
TAVD	Analog Power	D5 G2 H3 J2 R1 U1 U2 Y5	The power (TAVD) pins for the LVDS transmitters. These pins should be connected to analog +3.3V.
TAVS	Analog Ground	C4 E3 G1 J1 R2 T3 W3 AA4	The ground (TAVS) pins for the LVDS transmitters. These pins should be connected to analog GND.

Notes on Pin Description:

1. All S/UNI-VORTEX inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels, except RXD0+/- through RXD7+/-.

2. Inputs RSTB, ALE, RANYPHY, TMS, TDI, TCK and TRSTB have internal pull-up resistors. To improve noise immunity, in designs where these inputs are no-connects it is still recommend that they be tied to VDD.

3. The recommended power supply sequencing is as follows:

3.1 During power-up, the voltage on the BIAS pins must be kept equal to or greater than the voltage on the VDD pins, to avoid damage to the device.

3.2 The VDD power must be applied before input pins are driven or the input current per pin be limited to less than the maximum DC input current specification. (20 mA)

3.3 Analog power supplies (QAVD, CAVD, RAVD, TAVD) must have their current per pin limited to the maximum latch-up current specification (100 mA). In operation, the differential voltage measured between AVD supplies and VDD must be less than 0.5 V. The relative power sequencing of the multiple AVD power supplies is not important.

3.4 Power down the device in the reverse sequence.

9 FUNCTIONAL DESCRIPTION

First, a brief note on terminology. Throughout this document the use of the term "downstream" implies data read in from the parallel bus (or microprocessor port) and sent out the LVDS links. However, since the S/UNI-VORTEX is a slave device and bus direction (transmit or receive) is normally defined with respect to the bus master, the downstream bus is called the Transmit bus. Conversely, "upstream" is used to describe the data path from the LVDS to the parallel bus, which is called the Receive bus.

9.1 Cell Interface

Cell transfer from the S/UNI-VORTEX (bus slave) to a traffic management device (bus master) in the upstream direction is configurable as either SCI-PHY or Any-PHY. SCI-PHY is very similar to UTOPIA, but it supports the appended bytes used by the S/UNI-VORTEX for carrying PHY address information. If the option to place PHY addressing information in the H5/UDF field is enabled, the SCI-PHY bus is compatible to a 16 bit Utopia Level 2. Any-PHY defines inband selection and polling techniques to support a large number of logical channels, where SCI-PHY is limited to 32 and UTOPIA is limited to 31.

The downstream interface only provides an Any-PHY bus slave interface. While the downstream cell transfer mechanism is compatible with existing SCI-PHY devices (or UTOPIA devices supporting extended cells), the channel status polling is a new extension.

16-bit wide busses plus parity are supported; 8 bit wide is not supported.

9.1.1 Downstream

Conceptually, the Any-PHY protocol can be divided into two processes: polling and cell transfer.

Polling in the downstream direction is used by the bus master – typically a traffic buffering and management device – to determine when a buffered data cell can be safely sent to a downstream PHY. The S/UNI-VORTEX provides an independent cell buffer for each logical downstream channel on each LVDS link. In total there are 256 data path cell buffers (maximum 32 channels per LVDS link times 8 links) plus 8 microprocessor communication channel buffers (one per link). This arrangement ensures there is no head of line blocking while eliminating the risk of buffer overflow.

The traffic manager need only poll those logical channels for which it has downstream cells queued. A cell transfer can be initiated after a polled logical

channel asserts the TPA output. Each channel's cell buffer availability status (i.e. the status that will be driven onto the TPA output when the channel is polled) is deasserted when the first byte of a cell is written into the buffer. It is re-asserted only after the number of bytes programmed by the associated Downstream Logical Channel FIFO Ready Level register have been serialized onto a high-speed link. Determining what value to set the FIFO ready level is discussed in Section 12.1.

Polling is performed using the TADR[11:0] bus, which supports a 4096 logical channel address space. Up to 32 logical channels associated with each high-speed link can be mapped to anywhere within this address space with a granularity of eight locations through the Logical Channel Base Address registers. To provide an optimal address map regardless of the number logical channels per high-speed link, each high-speed link can be programmed to use 8, 16, 24 or 32 address locations through the Logical Channel Address Range registers. The eight control channels of each S/UNI-VORTEX are mapped to eight contiguous address locations starting at the address set by the Control Channel Base Address register. The control channels are associated with the addresses numerical, i.e. the control channel for TXD0+/- belongs to the lowest order address and TXD7+/- belongs to the highest order address.

With respect to cell transfers, the Any-PHY port appears like a single PHY entity. No out of band addressing is required. Instead, the first word of the transferred cell identifies the destination logical channel. The format of the cell data structure is illustrated in Fig. 3. As programmed through register bits, a User Prepend word may be prepended to a basic ATM cell to support applications where context information is carried inband. By default, only the logical channel index (Word 0) is prepended.

The cell will be transferred to a S/UNI-VORTEX if the ADDR[11:0] (ADDR[13:12] is unused in the downstream direction.) field value matches the logical channel mapping programmed through the Control Channel Base Address, Logical Channel Base Address and Logical Channel Address Range / Logical Channel Base Address MSB registers.

Normally, ADDR[11:0] is contained within Word 0 of the Any-PHY data structure, but can be mapped to the H5/UDF fields. The H5/UDF (User Defined Field) and User Prepend fields can be handled in four ways:

1. They are excluded from the Any-PHY data structure.

2. They exist in the Any-PHY data structure, but are not passed across the high-speed serial interfaces. The contents are ignored.

3. They are passed transparently across the high-speed serial interfaces.

4. The H5/UDF fields contain the ADDR[11:0] value and are used to route transferred cells. In this case Word 0 is not used and should not generated by the bus master.

The treatment of the H5/UDF field, the address prepend(word 0), and their corresponding fields on the LVDS link are independent of that of the User Prepend. See Section 12.2 Interaction Between Bus and LVDS Configurations on page 130 for further details.

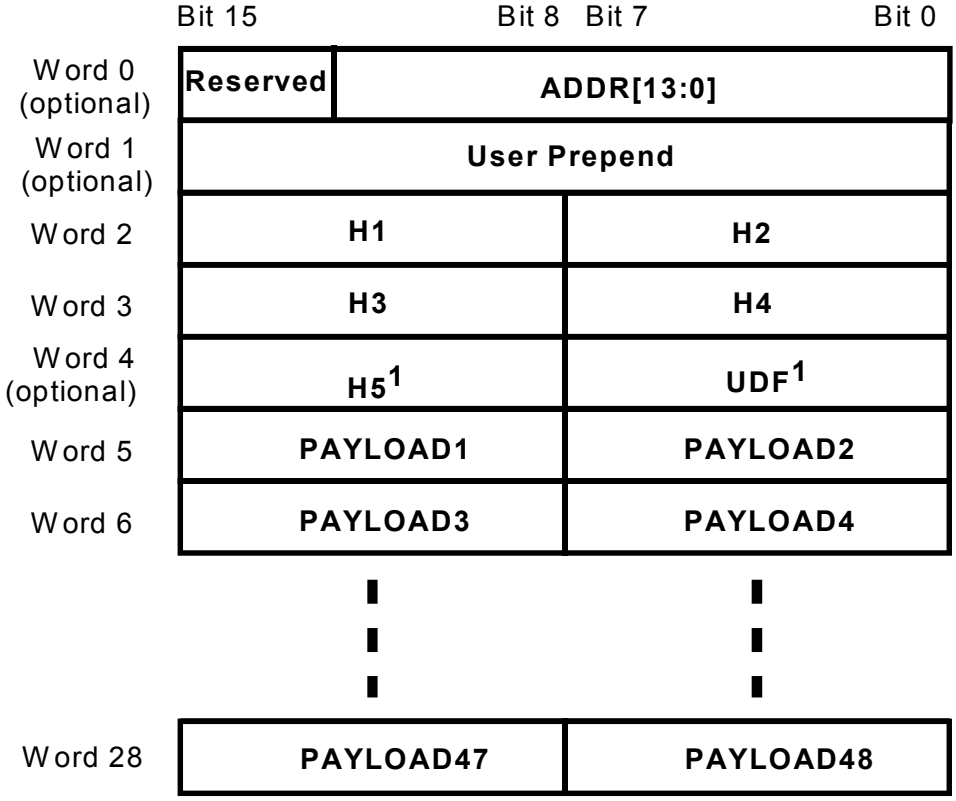
Although the ability to carry the inband address in the H5/UDF fields is provided for compatibility with devices that cannot generate an address prepend, there are two constraints that must be respected in this configuration:

1. Recall that in the default case (i.e. Word 0 provides the address) the logical channel participating in a cell transfer will deassert TPA upon the first word of the cell transfer. However, when the H5/UDF provides the address, the channel's TPA status will not return deasserted until nine TCLK periods after the last word of the cell transfer is complete. This implies that once a cell transfer to a channel has begun that channel should not be polled again until at least nine bus cycles after the transfer is complete.

2. Once the cell transfer is started, the TENB input must remain low until after the H5/UDF word has been transferred. After that, it is permissible for TENB to toggle high to momentarily halt the cell transfer.

Be aware that the Any-PHY data structures are transported transparently. There are no constraints on the contents. Therefore, data streams other than ATM cells can be transferred across the Any-PHY interface; only the bus timing and protocols need be respected.

Fig. 3 SCI-PHY/Any-PHY Cell



Format Note 1: Optionally, the H5/UDF fields can be overwritten by ADDR[13:0].

9.1.2 Upstream

In the upstream direction, each S/UNI-VORTEX appears as a single SCI-PHY or Any-PHY slave. The traffic from each high-speed serial link (RXD0+/- through RXD7+/) is queued independently to support per logical channel flow control without head of line blocking. Weighted round robin servicing determines the order of cells presented on RDAT[15:0]. Weights are strictly linear. For example, compared to a link with a weight of one, a LVDS link with a weight of four will on average have four times the number of opportunities to place a cell from its receive buffer onto the upstream bus. Each high speed serial link can be assigned a weight between 1 and 4. When the state of the RADR[4:0] inputs equals the state of the VADR[4:0] pins, the RPA output indicates whether there is at least one cell available for transfer from any link.

To support current and future devices, the interface is configurable as either an Any-PHY or SCI-PHY interface. Table 1 summarizes the distinctions between the two protocols.

Table 1 SCI-PHY and Any-PHY Comparison

Attribute	SCI-PHY	Any-PHY
Latency	RDAT[15:0], RPRTY, RSOP and RSX are driven or become high impedance immediately upon sampling RENB low or high, respectively. RPA is driven immediately upon sampling a RADR[4:0] value that matches VADR[4:0].	RDAT[15:0], RPRTY, RSOP and RSX are driven or become high impedance on the RCLK rising edge following the one that samples RENB low or high, respectively. RPA is driven on the RCLK rising edge following the one that samples a RADR[4:0] value that matches VADR[4:0].
RSX	Undefined. It is low when not high impedance.	High coincident with the first word of the cell data structure.
RSOP	High coincident with the first word of the cell data structure.	High coincident with the second word of the cell data structure.
Paused transfers	Permitted by deasserting RENB high, but the S/UNI-VORTEX's address must be presented on RADR[4:0] the last cycle RENB is high.	Permitted by deasserting RENB high. The cell transfer resumes unconditionally when RENB is asserted low again.
Autonomous deselection	Not supported. A subsequent cell is output (provided one is available) if RENB is held low beyond the end of a cell.	The outputs become high impedance after the last word of a cell is transferred until the S/UNI-VORTEX is reselected.

The cell format is the same as the downstream interface (Fig. 3). No address map manipulation is performed in the upstream direction; ADDR[13:0] field encoding has a fixed relationship to the physical ports. ADDR[13:9] will always equal the VADR[4:0] input pins' state. ADDR[8:6] corresponds to the index of the high speed serial link (RXD0+/- through RXD7+/-) over which the cell was received. ADDR[5:0] presents the logical channel index that had been encoded in the cell received on the high-speed serial link. An encoding of "111110" in ADDR[5:0] indicates the cell is a control channel cell.

9.2 High-Speed Serial Interfaces

The S/UNI-VORTEX provides backplane interconnection via 100 to 200 Mb/s serial links. All data destined to and coming from the line cards are concentrated on these high-speed links. The transceivers support UTP-5 cable lengths up to 10m. To avoid clock skew issues, no clock is transmitted and the receivers recover a local clock from the incoming data.

The serial links typically carry ATM cells with prepended bytes. The cell format is illustrated in Fig. 4. The S/UNI-VORTEX appends the first four bytes and the Header Check Sequence (HCS) byte in the downstream direction and strips them off and parses them in the upstream direction. The remainder of the bytes in the data structure is transferred transparently. The bytes are serialized most significant bit first.

The bit stream is a simple concatenation of the extended cells. Cell rate decoupling is accomplished through introduction of stuff cells.

The transmitter inserts a correct CRC-8 that protects both the ATM cell header and prepended bytes in the HCS byte. The receiver uses the HCS byte for delineation. Failure to establish cell alignment results in a loss of cell delineation (LCD) alarm. The entire bit stream is scrambled with a $x^{43} + 1$ self-synchronous scrambler.

Table 2 summarizes the contents of the system prepended bytes.

Fig. 4 High-Speed Serial Link Data Structure

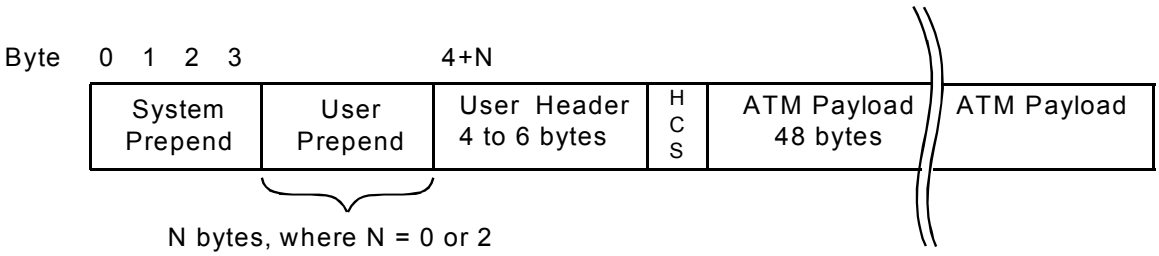


Table 2 Prepended Fields

Byte	Bits	Mnemonic	Description
0 1	7:0 7:0	CA[15:8] CA[7:0]	The CA[15:0] bits carry logical channel flow control information in the upstream direction. To support 32 logical channels, the status for each logical channel is sent every other cell; the CASEL indicates

Byte	Bits	Mnemonic	Description
			which half is represented. If CASEL is logic 0, CA[15:0] corresponds to those logical channels with UTOPIA addresses 0 through 15. If CASEL is logic 1, CA[15:0] corresponds to those logical channels with UTOPIA addresses 16 through 31. In the downstream direction, CA[0] is the only relevant bit and it flow controls the aggregate. A logic 0 indicates the far end can accept no more cells, and the S/UNI-DUPLEX will immediately start sending idle cells. If this bit is a logic 1, the S/UNI-DUPLEX is free to send all queued traffic. To allow inter-operability with a device that may be flow controlled on a logical channel basic, CA[15:1] are set to the same state as CA[0]. In the event of an errored header (as detected by an incorrect HCS), the CA bits will be assumed to be all zero. This ensures cells are not transmitted for which there is no buffer space.
2	7	CASEL	The state of the CA select bit determines which half of the modems the CA[15:0] bits correspond to. CASEL toggles with each cell transmitted.
2	6	UPCA	The UPCA bit carries flow control information for the microprocessor control channel. If this bit is one, control channel cells may be transferred. In the event of an errored header, the UPCA bit will be assumed to be zero. This ensures cells are not transmitted for which there is no buffer space.
2	5:0	PHYID	The PHY identifier determines to which PHY a cell is destined in the downstream direction and from which PHY it came in the upstream direction. It also indicates whether the cell is a stuff or control channel cell. The field is encoded as

Byte	Bits	Mnemonic	Description
			follows: "111111" – Stuff cell provided for cell rate decoupling. The payload carries no useful data and the cell shall be discarded. "111110" – Control channel cell. On the transmit serial link, PHYID shall equal this value for all cells inserted via the Microprocessor Cell Buffer and for all cells received from the Any-PHY interface whose inband address matches that programmed by the Control Channel Base Address register. All cells received on the serial link with this encoding will be routed to the local microprocessor if the ROUTECC register bit is a logic 1. Otherwise, the cells are routed to the SCI-PHY/Any-PHY interface. "100000" to "111101" – Reserved "000000" to "011111" – Logical channel index for PHY device.
3	7	BOC	The Bit Oriented Code (BOC) bit position carries a repeating 16 pattern that encodes one of 63 possible code words used for remote control and status reporting. Three codes are predefined to represent a remote defect, a loopback activate request and a loopback deactivate request. The remaining codes are either reserved or user defined. The receiver ensures the pattern is the same for 8 of 10 (default) or 4 of 5 repetitions before validating a new code word. Refer to the Bit Oriented Codes section for more details.
3	6	ACTIVE	The link active bit indicates which of the redundant links is currently chosen. The S/UNI-DUPLEX will switch to the link which contains a one in this location for at least 3 consecutive cells. The line card microprocessor can override this selection.

Byte	Bits	Mnemonic	Description
			The transmitted ACTIVE bit is set by the per-link ACTIVE register bits. To confirm which link is active, the received ACTIVE bit will be a one if the associated link is selected by the S/UNI-DUPLEX. In the event of an errored header or out of cell delineation state, the previous ACTIVE value is retained.
3	5:0	TREF[5:0]	The timing reference encodes an 8 kHz signal inband that is independent of the serial bit rate. The TREF[5:0] binary value represents the number of high-speed link bytes after this one at which the timing reference is inferred. An all ones value indicates no timing mark is associated with this cell.

The transmitter outputs are internally terminated current mode drivers. Correct termination at the receiver is required to provide the correct signal levels..

The internal transmit clock is synthesized from a 12.5 MHz to 25 MHz clock. The resulting data bit rate is eight times the frequency of the REFCLK input. All jitter below 1 MHz on REFCLK is passed unattenuated to the TXDn+/- outputs. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference input and a low noise board layout, the intrinsic jitter is typically less than 0.01 UI RMS and 0.10 UI peak-to-peak when measured using a band pass filter with 12 kHz and 1.3 MHz cutoff frequencies.

The eight truly differential receivers are capable of handling signal swings down to 100mV. A wide common mode range makes them compatible with LVDS signals. External termination resisters must be provided to match the cable impedance.

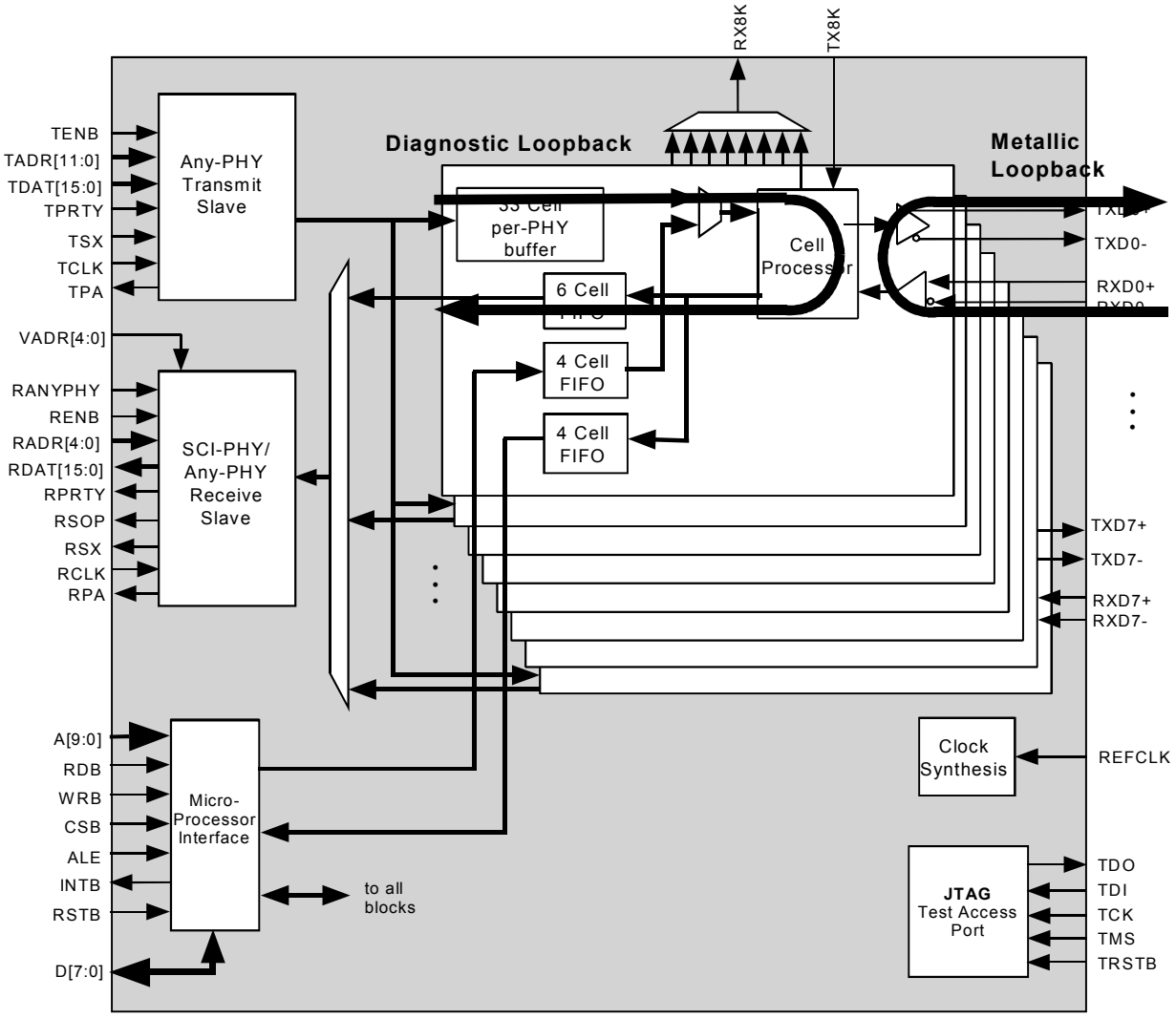
The receivers monitor for loss of signal (LOS) on the links. LOS is declared upon 2048 bit periods (13.2 μs at 155.52 Mb/s) without a signal transition in the scrambled data. As a consequence, a status bit is set, a maskable interrupt is asserted and the RDI codeword is sent repetitively in the BOC bit in the corresponding downstream link. The LOS indication is cleared when a signal transition has occurred in each of 16 consecutive intervals of 16 bit periods each.

Clock recovery is performed by a digital phase locked loop (DPLL). The implementation is robust against operating condition variations and power supply

noise. The receive link is constrained to be within 100 ppm of eight times the REFCLK frequency.

As shown in Fig. 5, two datapath loopbacks are provided on each LVDS link to aid in fault isolation and continuity verification. The metallic loopback routes receive data to the transmitter. The diagnostic loopback replaces the receive data with the transmit data. The two loopbacks can be enabled individually or simultaneously on the same link, and each link can be looped back independently of the other seven.

Fig. 5 Loopbacks



A diagnostic loopback is effected if the DLB bit of the Serial Link Maintenance register is set to logic 1. The transmit data and clock are inserted into the receive datapath downstream of the clock recovery.

The metallic loopback can be effected in one of three ways: after the receipt of a loopback activate bit-oriented code (as described on page 39), when the MLB bit of the Serial Link Maintenance register is set to logic 1, or when the RSTB input is asserted low. The loopback occurs at the LVDS transceiver after the conversion to digital but before clock recovery . The looped back data may be slightly distorted by the data slicing (conversion from differential to single-ended) and the re-buffering that occurs.

Metallic loopback is terminated if a loopback deactivate bit oriented code is received and validated, provided the MLB bit of the Serial Link Maintenance register is logic 0.

9.2.1 Link Integrity Monitoring

Although the serial link bit error rate can be inferred from the accumulated Header Check Sequence (HCS) errors, the option exists to perform error monitoring over the entire bit stream.

When the feature is enabled the second User Prepend byte transmitted shall be overwritten by the CRC-8 syndrome for the preceding cell. The encoding is valid for all cells, including stuff cells. The CRC-8 polynomial is $x^8 + x^2 + x + 1$. The receiver shall raise a maskable interrupt and optionally increment the HCS error count. Simultaneous HCS and cell CRC-8 errors result in a single increment.

9.2.2 Bit Oriented Codes

Bit Oriented Codes (BOCs) are carried in the BOC bit position in the System Prepend. The 63 possible codes can be used to carry predefined or user defined signaling.

Bit oriented codes are transmitted as a repeating 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0). The code to be transmitted is programmed by writing the Transmit Bit Oriented Code register. The autonomously generated Remote Defect Indication (RDI) code, which is generated upon a loss-of-signal or loss-of-cell-delineation, takes precedence over the programmed code. RDI insertion can be disabled via the RDIDIS bit of the Serial Link Maintenance register. RDI can be inserted manually by setting the Transmit Bit Oriented Code register to all zeros.

The receiver can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit

in the Bit Oriented Code Receiver Enable register. Unless fast declaration is necessary, it is recommended that the AVC bit be set to logic 0 to improve bit error tolerance. Valid BOC are indicated through the Receive Bit Oriented Code Status register. The BOC bits are set to all ones (111111) if no valid code has been detected. A maskable interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

When the receiver is out of cell delineation (OCD) and the Receive Bit Oriented Code Status register will produce all ones (111111).

The valid codes are provided in Table 3. The Reserved codes anticipate future enhanced feature set devices and should not be used. The User Defined codes may be used without restriction. Regardless of definition, all 63 codes may be validated and read by the microprocessor.

Note that processing of the metalic loopback activate code is handled as a special case. The RXDn+/- data is looped back onto TXDn+/- at the end of the reception of the loopback activate code rather than when the code is first validated. For loopback to be initiated the loopback activate code must be first validated (received 8 out of 10 times) and then invalidated, typical by reception of another code. The loopback is not enable upon initial validation of the loopback activate code because the looped back signal, which still contains the original loopback activate command, would cause the far-end receiver to go into metallic loopback as well, thereby forming an undesirable closed loop condition! The loopback is cleared immediately upon the validation of the loopback deactivate code, assuming the MLB register bit is logic 0.

To produce a loopback at the far end, program the Transmit Bit Oriented Code register with the loopback activate code for at least 1 ms and then revert to an another (typically idle) code. Upon termination of the loopback activate code, the data transmitted on TXDn+/- is expected to be received verbatim on the RXDn+/- inputs. When transmitting a loopback activate code, it is recommended the RDIDIS register bit be set to logic 1, or else a loss-of-signal or loss-of-cell-delineation event, would cause a premature loopback due to a pre-emptive Remote Defect Indication (RDI) code being sent.

The remote reset activate and deactivate code words are supported by the S/UNI-DUPLEX (PM7350) device. The S/UNI-VORTEX can send the reset activate code to cause the S/UNI-DUPLEX device to assert its active low RSTOB output. The deactivate code causes deassertion of RSTOB. See the S/UNI-DUPLEX datasheet for details.

The Remote Defect Indication (RDI) is sent whenever Loss of Signal (LOS) or Loss of Cell Delineation (LCD) is declared. This code word takes precedence over all others.

Table 3 : Assigned Bit Oriented Codes

Function	Codeword (left bit transmitted first)
Remote Defect Indication (RDI)	11111111 00000000
Loopback activate	11111111 01000000
Loopback deactivate	11111111 00100000
Remote reset activate	11111111 01100000
Remote reset deactivate	11111111 00010000
Reserved	11111111 01010000
. . .	. . .
Reserved	11111111 00000100
User Defined	11111111 01000100
. . .	. . .
User Defined	11111111 00111110
Idle Code	11111111 01111110

9.2.3 Cell Delineation Process

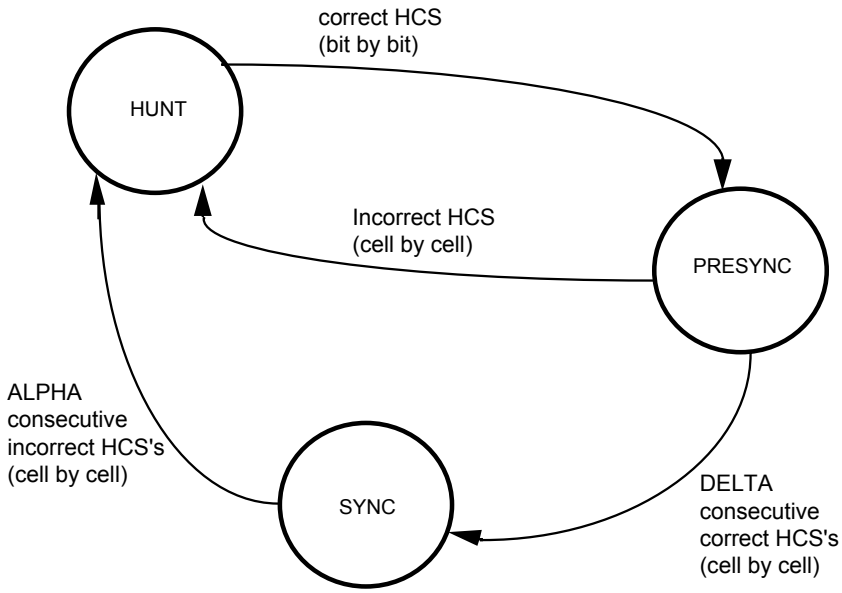
The S/UNI-VORTEX performs HCS cell delineation, payload descrambling, idle cell filtering and header error detection to recover valid cells from the receive high-speed links. These functions are performed in the spirit of ITU-T Recommendation I.432.1, but support 9 to 13 byte cell headers.

Cell delineation is the process of framing to cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 ($x^8 + x^2 + x + 1$) calculation over all octets of the cell header. In accordance with ITU-T Recommendation I.432.1, the coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries.

The cell delineation circuitry performs a sequential bit-by-bit hunt for a correct HCS sequence. This state is referred to as the HUNT state. When a correct HCS is found, a particular cell boundary is assumed and the PRESYNC state is entered. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells and the delineation state machine falls back to the HUNT state. If an incorrect HCS is not found in this

PRESYNC period then a transition to the SYNC state is made, cell delineation is declared and all non-idle cells with a correct HCS are passed on. In the SYNC state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Fig. 6.

Fig. 6: Cell delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6.

The loss of cell delineation (LCD) alarm is declared after 1318 consecutive cell periods (4.0 ms at 155.52Mb/s) in the HUNT or PRESYNC states. The LCD alarm is cleared after 1318 consecutive cells in the SYNC state.

All cells with an incorrect HCS octet are filtered out and counted. Header correction is not performed.

9.2.4 Protection Switching Protocol

The S/UNI-VORTEX and its sister device, the S/UNI-DUPLEX inherently support system architectures requiring fault tolerance and 1:1 redundancy of the system's common equipment. In point-to-point backplane architectures such as these, the 1:1 protection also includes the associated LVDS links connecting the

common equipment to the line cards. The S/UNI-VORTEX and S/UNI-DUPLEX, perform clock recovery, cell delineation, and header error monitoring for all receive high-speed serial links simultaneously. The maintained error counts and alarm status indications may be used by the control system to determine the state and viability of each high speed serial link.

In these architectures, the S/UNI-DUPLEX will be connected to two S/UNI-VORTEXs, one on the active common card and one on the spare common card . Upon a failure of the active card, the spare card becomes the conduit for traffic. The S/UNI-VORTEX facilitates link selection upon start-up as well as switching between links upon failure conditions.

Typically a centralized resource or cooperating distributed microprocessor subsystems will determine which common card is to be considered active for each downstream S/UNI-DUPLEX. The key to link selection lies in how the “ACTIVE” bit is handled by the S/UNI-VORTEX and S/UNI-DUPLEX. The control system uses the ACTIVE bit within each of the 8 Serial Link Maintenance registers to independently set the state of each link’s ACTIVE status. The current state of the link’s ACTIVE bit is sent downstream once per transmitted cell. The ACTIVE status is debounced and acted upon by the S/UNI-DUPLEX.

The S/UNI-DUPLEX will only accept data traffic from one of its two LVDS links, and normally it is the link marked ACTIVE that is considered to be the working link. However, the S/UNI-DUPLEX can override this using local control. Thus, although the S/UNI-VORTEX may indicate the ACTIVE and spare links, it is actually the S/UNI-DUPLEX that must effect the protection switching. See the S/UNI-DUPLEX data sheet for additional details.

The S/UNI-DUPLEX returns an ACTIVE bit status to indicate which link it has chosen as active. This reflected ACTIVE bit does not have a direct affect on the S/UNI-VORTEX, but its status is debounced (must remain the same for 3 received cells) and then stored by the S/UNI-VORTEX in the Receive High-Speed Serial Cell Filtering Configuration/Status register. The reflected status can be used by the local control system to confirm receipt of the ACTIVE status by the S/UNI-DUPLEX.

9.3 Cell Buffering and Flow Control

The possibility of congestion is inherent in an access multiplexer. In the downstream direction, the WAN link can generate a burst of cells for a particular modem at a rate far exceeding the modem’s bandwidth capacity. Therefore, feedback to the traffic scheduler is required to cause it to buffer and smooth cell bursts to prevent downstream buffer overflow. In the upstream direction, the subscribed aggregate bandwidth can exceed that accommodated by the WAN

uplink. Flow control is required to ensure fair access to the up-link, to minimize cell loss and to minimize the impact of greedy users on others.

By its very nature, the upstream and downstream flow control implemented by the S/UNI-VORTEX can only be explained in the context of an overall system, including the role played by the eight S/UNI-DUPLEX devices connected to the S/UNI-VORTEX. Therefore, the reader is referred to a companion document provided by PMC-Sierra titled *S/UNI-VORTEX & S/UNI-DUPLEX TECHNICAL OVERVIEW*. The document number is PMC-981025 and it can be obtained by one of the various means described on the last page of this document.

For the remainder of this data sheet we will focus on describing cell buffering and flow control as it is implemented by the S/UNI-VORTEX.

9.3.1 Downstream Traffic Flow Control

The S/UNI-VORTEX has 33 one cell deep buffers for each of the 8 downstream LVDS links. In the Section 9.1.1 on Page 29 we describe how the S/UNI-VORTEX responds to bus polling and asserts the TPA signal when another cell can safely be written into one of these downstream cell buffers. Now we will describe how, on a per link basis, the S/UNI-VORTEX schedules cells out of these 33 cell buffers and transmits them on their LVDS link. We describe an individual link here, but the reader is reminded that there is no scheduling interaction or interdependence among the 8 LVDS links – each has its own 33 cell buffer and each has its own scheduler.

Downstream scheduling only occurs when the previous cell has been fully transmitted over the downstream link. In other words, once a cell (data or stuff cell) has been scheduled the entire cell is sent before another cell can be scheduled. When there is no buffered data in any of the 33 buffers the S/UNI-VORTEX generates a stuff cell and sends it on the link. A stuff cell meets all the requirements of a standard data cell, including valid system overhead information, but stuff cells are discarded by the far-end receiver.

When there are one or more non-empty buffers, the S/UNI-VORTEX must decide which of the far-end channels (up to 32 PHYs and the microprocessor port) should have its buffered cell scheduled onto the downstream link. This decision consists of two steps: first any channel that is presenting a far-end buffer full status (described below) is eliminated from this scheduling round. If all far-end channels have full buffers a stuff cell is generated automatically. Otherwise, a simple round robin algorithm is used among the remaining eligible channels to share the downstream link fairly and schedule the next cell to be sent.

As shown in Table 2, each cell transmitted over each of the eight upstream LVDS upstream links contains 16 bits of information that convey the far-end cell buffer status (full or not full) for 16 of the maximum 32 active PHYs supported on each link. After two cells are received on the upstream link the downstream buffer status of all 32 far-end PHYs has been updated. A separate overhead bit per cell conveys the buffer status of the far-end microprocessor port.

Hence, at any given instant the S/UNI-VORTEX is using information that is either one or two cells out of date. The far-end device (typically the S/UNI-DUPLEX) is therefore required to have enough per PHY buffer space to accommodate the slight delay in conveying the “buffer full” information to the S/UNI-VORTEX. The S/UNI-VORTEX uses the full or not full information to determine which channels should be involved in the current round of scheduling, as discussed above.

9.3.2 Upstream Traffic Flow Control

The upstream traffic flow control within the S/UNI-VORTEX allows for some system engineering flexibility. When the system is engineered such that maximum aggregate burst upstream bandwidth is less than or equal to the link and device bandwidth at each stage of concentration, congestion will not occur prior to upstream traffic queuing in the TM device[1]. In this case, upstream traffic flow control is unnecessary and will not be utilized within the S/UNI-DUPLEX or S/UNI-VORTEX devices.

However, when a system is engineered such that upstream burst bandwidth capacity can exceed the link and bus bandwidth, then depending on the over subscription employed, misbehaving users, and traffic burst scenarios, congestion at the upstream S/UNI-VORTEX buffers can occur. To ensure that these buffers do not overflow, upstream traffic flow control is implemented by the S/UNI-VORTEX and S/UNI-DUPLEX.

Far-end scheduling of the up to 32 upstream PHY channels and the microprocessor channel onto the upstream LVDS link is discussed in the S/UNI-DUPLEX Data Sheet. This section discusses how upstream flow control is implemented to prevent overflow of the S/UNI-VORTEX’s upstream FIFOs.

Unlike the downstream direction, the upstream direction does not require per channel buffering or per channel buffer status indication. In the S/UNI-VORTEX, each of the 8 upstream LVDS serial links is provided with a simple six cell FIFO. The SCI-PHY/Any-PHY bus slave state machine services the 8 FIFOs with a weighted round-robin algorithm and presents the data to the upstream bus

[1] Upstream queues could congest due to restricted up-link capacity, in which case appropriate congestion management algorithms within the TM device should be invoked.

master as a single cell stream. Scheduling from the S/UNI-VORTEX onto the upstream bus is described more fully in Section 9.1.2 on Page 32.

In aggregate, the 8 upstream links can burst data into the S/UNI-VORTEX at up to 1.6 Gbps, which is twice the maximum bandwidth of the upstream bus. Further, the bus master may be servicing several S/UNI-VORTEX devices at once or be otherwise restricted in the maximum sustained bandwidth it is able to receive from the S/UNI-VORTEX. Therefore, the potential to overflow one or more of the 6 cell upstream FIFOs is a real possibility.

When any upstream FIFO has less than three empty cell buffers, it deasserts the cell available (CA[0]) bit sent in the system overhead of the corresponding downstream LVDS link (see Table 2). It is the responsibility of the far end device (typically a S/UNI-DUPLEX) to start sending stuff cells immediately upon indication that the S/UNI-VORTEX can accept no more traffic. By setting the full mark at 3 cells the S/UNI-VORTEX allows for up to two additional cells can be accepted after the cell available bit is deasserted. This accommodates far-end latency in reaction to the CA[0] indication.

9.4 Timing Reference Insertion and Recovery

The high-speed LVDS links are capable of transporting a timing reference in both directions, independent of the LVDS bit rate. As shown in Table 2, every cell transmitted over the LVDS contains a timing reference field called TREF[5:0]. Although the timing reference is targeted at a typical need of transporting an 8 kHz signal, its frequency is not constrained to 8 kHz. Any frequency less than the cell rate is permissible.

In the transmit direction, rising edges on the TX8K input are encoded in the cells transmitted on all eight serial links. For each of the 8 LVDS links, the rising edge of TX8K causes an internal counter to be initialized to the cell length minus 1. The counter decrements with each subsequent byte transmitted until the fourth byte of the next extended cell, at which point the state of the counter is written into the outgoing TREF[5:0] field. If no rising edge on TX8K has occurred, TREF[5:0] is set to all ones.

In the receive direction the S/UNI-VORTEX is typically receiving cells from a S/UNI-DUPLEX device, which implements the same TX8K process described above. As determined by the value of the RX8KSEL[2:0] bits in the Master Configuration register, the timing signal received over one of the eight LVDS links is recreated on RX8K.

The S/UNI-VORTEX monitors the TREF[5:0] field on the selected upstream LVDS link and initializes an internal counter to the value of TREF[5:0] each time the field is received. The counter decrements with each subsequent byte

received. When the count becomes zero, a rising edge is generated on RX8K. If the value of TREF[5:0] is all ones, RX8K remains low. RX8K is left asserted for two high speed (REFCLK) reference clock periods, and then it is deasserted.

The recovered timing event is generated one cell period later than the inserted timing with a resolution of one byte. Because of the limited resolution, some jitter is present. At a link rate of 155.52 Mb/s, 63ns of peak-to-peak jitter will occur on RX8K. An external local high-Q phase locked loop (PLL) can be used to remove the jitter.

9.5 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-VORTEX identification code is 173510CD hexadecimal.

9.6 Microprocessor Interface

The microprocessor interface is provided for device configuration, control and monitoring by an external microprocessor. Normal mode registers and test mode registers can be accessed through this port. Test mode registers are used to enhance the testability of the S/UNI-VORTEX.

The interface has an 8-bit wide data bus. Multiplexed address and data operation is supported.

9.6.1 Inband Communication Channel

To provide flexibility, two mechanisms are being provided for the transport of a control channel. Control channel cells can be inserted and extracted either via the microprocessor interface or via an external device transferring control channel cells across the SCI-PHY/Any-PHY interfaces.

The control channel cell insertion and extraction capabilities provide a simple unacknowledged (but flow controlled) cell relay capability. For a fully robust control channel implementation, it is assumed the local microprocessor and the remote entity are running a reliable communications protocol.

9.6.2 Insertion and Extraction Via the SCI-PHY/Any-PHY Interfaces

Control channel cells inserted via the downstream Any-PHY interface are treated in the same manner as normal data traffic with respect to flow control, buffering, and cell format.. The transmitting of control cells across the high-speed serial

link is throttled by the UPCA bit in the upstream cell prepends. The UPCA bit reflects the buffer availability on the line card.

In the downstream direction, the control channels for the eight links are provided with a polling address range set by the Control Channel Base Address register. As discussed in Section 9.1.1, the TPA status for each control channel can be discovered by presenting a TADR[11:0] value in the specified range. A transferred control channel cell is accepted when the ADDR[11:0] field in the cell structure corresponds to one of the eight addresses specified by the Control Channel Base Address register.

In the upstream direction, control channel cells are given no special treatment when they are directed to the upstream SCI-PHY/Any-PHY bus. The traffic management device can identify them by an encoding of “111110” in the ADDR[5:0] field in the cell prepend or H5.UDF field.

9.6.3 Insertion and Extraction Via the Micro-Processor Interface

Control cells can be inserted and extracted through the parallel microprocessor interface.

9.6.3.1 Writing Cells

The S/UNI-VORTEX contains a two cell buffer per high-speed link for the insertion of a cell by the microprocessor onto the high-speed serial links. Optional CRC-32 calculation over the last 48 bytes of the cell relieves the microprocessor of this task. The CRC-32 generator polynomial is consistent with AAL5:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

All cells written by the microprocessor will have binary 111110 encoded in the PHYID[5:0] field within the cell prepend bytes. This distinction between user cells and control cells provides a clear channel for both types of cells. The microprocessor cell format is illustrated in Fig. 7. The 8-bit cell data structure is fixed at 60 bytes long regardless of how the SCI-PHY/Any-PHY bus and LVDS link are configured. The microprocessor must transfer all bytes of the cell, including the unused ones. The unused bytes are included in the received cell when it is made available to the far-end microprocessor, but the value of the bytes is undefined.

Bytes marked with an asterisk in Fig. 7 must be included in cells written into the cell transfer register, but they will only be sent across the LVDS if the corresponding Transmit High-Speed Serial Configuration register and the far-

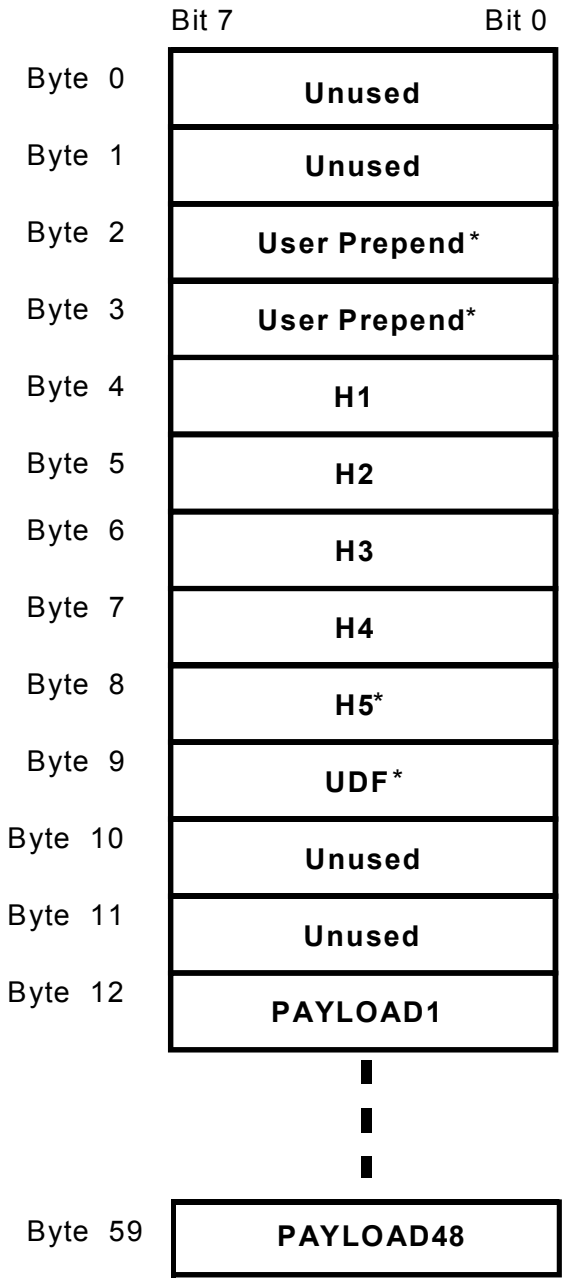
end's corresponding Receive High-Speed Serial Configuration register have been programmed to include them[1].

Other than what has already been mentioned, there are no constraints on the contents of cells written by the microprocessor. They are transported across the LVDS link transparently. Specifically, although the standard ATM header bytes H1-H5 are shown in Fig. 7 there is no restriction on the values they can contain.

See the Operation section for details on the cell write protocol.

[1] Obviously the near and far end must configure their corresponding High-Speed Serial Configuration registers such that the high speed link format is the same at both transmitter and receiver or the receiver will always be out of frame.

Fig. 7 Microprocessor Cell Format



*Depending on the serial link programming, these fields may be undefined or not transmitted.

9.6.3.2 Reading Cells

By default, control cells are not terminated by the Microprocessor Cell Buffer, but instead routed to the SCI-PHY/Any-PHY interface along with all other cells. Control cells that are routed to the SCI-PHY/Any-PHY bus will be stripped or padded (if required) to match the cell format of the bus.

The redirection of control cells must be enabled by the ROUTECC register bit in the Master Configuration register. If ROUTECC is a logic 1, all cells received on the high-speed serial link with binary 111110 in the PHYID[5:0] prepend field will be routed to the Microprocessor Cell Buffer. The buffer has a capacity of four cells dedicated to each high-speed link. The control channel is flow controlled to avoid cell loss.

A maskable interrupt status bit is set upon the receipt of a cell. The format of received cell when it is read from the Microprocessor Cell Buffer Data register is shown in Fig. 7. Unused bytes have undefined value. The value of the optional bytes depends on the configuration of the corresponding LVDS link and the source of the cell. Control cells that come from the far-end SCI-PHY/Any-PHY bus will have their optional fields defined only if both the SCI-PHY/Any-PHY bus and the LVDS link have been configured to carry them. Control cells that come from the far-end microprocessor port have their optional fields defined (i.e. equal to the value originally written by the far-end microprocessor) only if the LVDS link has been configured to carry them. This is discussed further in the Operations section.

See the Operation section for details on the cell read protocol.

9.7 Internal Registers

The microprocessor interface provides access to normal and test mode registers. The normal mode registers are required for mission mode operation, and test mode registers are used to enhance the testability of the S/UNI-VORTEX. The register set is accessed as follows:

9.8 Register Memory Map

Address	Register
0x000	Master Reset and Identity / Load Performance Meters
0x001	Master Configuration
0x002	Receive Serial Interrupt Status
0x003	Transmit Serial Interrupt Status
0x004	Miscellaneous Interrupt Statuses

0x005	Control Channel Base Address
0x006	Control Channel Base Address MSB
0x007	Clock Monitor
0x008	Downstream Cell Interface Configuration
0x009	Reserved
0x00A	Downstream Cell Interface Interrupt Enable
0x00B	Downstream Cell Interface Interrupt Status
0x00C	Upstream Cell Interface Configuration and Interrupt Status
0x00D – 0x00F	Reserved
0x010	Microprocessor Cell Buffer Interrupt Control and Status
0x011	Microprocessor Insert FIFO Control
0x012	Microprocessor Extract FIFO Control
0x013	Microprocessor Insert FIFO Ready
0x014	Microprocessor Extract FIFO Ready
0x015	Insert CRC-32 Accumulator (LSB)
0x016	Insert CRC-32 Accumulator (2nd byte)
0x017	Insert CRC-32 Accumulator (3rd byte)
0x018	Insert CRC-32 Accumulator (MSB)
0x019	Extract CRC-32 Accumulator (LSB)
0x01A	Extract CRC-32 Accumulator (2nd byte)
0x01B	Extract CRC-32 Accumulator (3rd byte)
0x01C	Extract CRC-32 Accumulator (MSB)
0x01D	Microprocessor Cell Buffer Data
0x01E – 0x07F	Reserved
0x080 – 0x09F	Registers associated with RXD0+/- and TXD0+/-
0x0A0 – 0x0BF	Registers associated with RXD1+/- and TXD1+/-
0x0C0 – 0x0DF	Registers associated with RXD2+/- and TXD2+/-
0x0E0 – 0x0FF	Registers associated with RXD3+/- and TXD3+/-
0x100 – 0x11F	Registers associated with RXD4+/- and TXD4+/-
0x120 – 0x13F	Registers associated with RXD5+/- and TXD5+/-
0x140 – 0x15F	Registers associated with RXD6+/- and TXD6+/-
0x160 – 0x17F	Registers associated with RXD7+/- and TXD7+/-

0x180 – 0x1FF	Reserved
0x200 – 0x3FF	Reserved for test registers.

9.8.1 Per-Link Registers

Each pair of serial links (RXDn+/- and TXDn+/-) has a identical bank of registers. These registers are located within the address space by a base address and offset according to the following formula:

register address = 0x080 + 0x20*(link index) + offset
where the link index = 0..7

Address Offset	Register
0x000	Receive High-Speed Serial Configuration
0x001	Receive High-Speed Serial Cell Filtering Configuration/Status
0x002	Receive High-Speed Serial Interrupt Enables
0x003	Receive High-Speed Serial Interrupt Status
0x004	Receive High-Speed Serial HCS Error Count
0x005	Receive High-Speed Serial Cell Counter (LSB)
0x006	Receive High-Speed Serial Cell Counter
0x007	Receive High-Speed Serial Cell Counter (MSB)
0x008	Receive High-Speed Serial FIFO Overflow
0x009	Upstream Round Robin Weight
0x00A	Logical Channel Base Address
0x00B	Logical Channel Address Range / Logical Channel Base Address MSB
0x00C	Downstream Logical Channel FIFO Control
0x00D	Downstream Logical Channel FIFO Interrupt Status
0x00E	Reserved
0x00F	Downstream Logical Channel FIFO Ready Level
0x010	Transmit High-Speed Serial Configuration
0x011	Transmit High-Speed Serial Cell Count Status
0x012	Transmit High-Speed Serial Cell Counter (LSB)
0x013	Transmit High-Speed Serial Cell Counter
0x014	Transmit High-Speed Serial Cell Counter (MSB)
0x015	Serial Link Maintenance
0x016	Reserved
0x017	Transmit Bit Oriented Code
0x018	Bit Oriented Code Receiver Enable

0x019	Receive Bit Oriented Code Status
0x01A – 0x01B	Reserved
0x01C	Upstream Link FIFO Control
0x01D – 0x01F	Reserved

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-DUPLEX. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-VORTEX to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-VORTEX operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-VORTEX operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x000: Master Reset and Identity / Load Performance Meters

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision number of the S/UNI-VORTEX to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-VORTEX.

In addition, writing to this register simultaneously loads all the performance meter registers in the S/UNI-VORTEX.

ID[3:0]:

The ID bits can be read to provide a binary S/UNI-VORTEX revision number.

TYPE[2:0]:

The TYPE bits can be read to distinguish the S/UNI-VORTEX from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-VORTEX to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-VORTEX is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-VORTEX out of reset. Holding the S/UNI-VORTEX in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset with the exception that the Master Test Register (0x200) is not reset by a software reset. Register 0x200 should be written after a software reset to ensure it is in a known state.

Register 0x001: Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R/W	MINTE	0
Bit 4	R/W	TPAEN	0
Bit 3	R/W	ROUTECC	0
Bit 2	R/W	RX8KSEL[2]	0
Bit 1	R/W	RX8KSEL[1]	0
Bit 0	R/W	RX8KSEL[0]	0

RX8KSEL[2:0]:

The RX8KSEL select (RX8KSEL[2:0]) bits determine the high-speed serial link from which RX8K is derived. RX8K is extracted from the RXDn+/- serial link whose index equals the binary RX8KSEL value.

ROUTECC:

The ROUTECC bit determines how the upstream control channel cells are handled. If ROUTECC is logic 0, the control channel cells are presented on the RDAT[15:0] cell bus. If ROUTECC is logic 1, the control channel cells are directed to the microprocessor port through a four cell FIFO.

TPAEN:

The TPA Enable (TPAEN) bit determines whether the TPA output is driven in response to polling. If TPAEN is logic 0, TPA is unconditionally high impedance. If TPAEN is logic 1, TPA drives upon the sampling of a TADR[11:0] value that lies in the range of addresses specified by the Control Channel Base Address, Logical Channel Base Address and Logical Channel Address Range registers. TPAEN should only be set to logic 1 after the aforementioned registers have been initialized.

MINTE:

The Master Interrupt Enable allows internal interrupt statuses to be propagated to the interrupt output. If MINTE is logic 1, INTB will be asserted low upon the assertion of an interrupt status bit whose individual enable is set. If MINTE is logic 0, INTB is unconditionally high-impedance.

Reserved:

The Reserved bit should be set be logic 0 for correct operation.

Register 0x002: Receive Serial Interrupt Status

Bit	Type	Function	Default
Bit 7	R	RXI[7]	X
Bit 6	R	RXI[6]	X
Bit 5	R	RXI[5]	X
Bit 4	R	RXI[4]	X
Bit 3	R	RXI[3]	X
Bit 2	R	RXI[2]	X
Bit 1	R	RXI[1]	X
Bit 0	R	RXI[0]	X

RXI[7:0]:

This register indicates whether there is a pending interrupt for a particular serial link. RXI[n] is associated with RXDn+/-. If RXI[n] is logic 1, at least one interrupt status bit within the associated Receive High-Speed Serial Interrupt Status, Receive High-Speed Serial FIFO Overflow or Receive Bit Oriented Code Status registers that has its corresponding enable set is a logic 1.

These bits are not self-clearing; they are only cleared to logic 0 by reading the associated Receive High-Speed Serial Interrupt Status, Receive High-Speed Serial FIFO Overflow or Receive Bit Oriented Code Status registers.

Register 0x003: Transmit Serial Interrupt Status

Bit	Type	Function	Default
Bit 7	R	TXI[7]	X
Bit 6	R	TXI[6]	X
Bit 5	R	TXI[5]	X
Bit 4	R	TXI[4]	X
Bit 3	R	TXI[3]	X
Bit 2	R	TXI[2]	X
Bit 1	R	TXI[1]	X
Bit 0	R	TXI[0]	X

TXI[7:0]:

This register indicates whether there is a pending interrupt for a particular serial link. TXI[n] is associated with TXDn+/-. If TXI[n] is logic 1, at least one interrupt status bit within the associated Transmit High-Speed Serial Cell Count Status or Downstream Logical Channel FIFO Interrupt Status registers that has its corresponding enable set is a logic 1.

These bits are not self-clearing; they are only cleared to logic 0 by reading the associated Transmit High-Speed Serial Cell Count Status or Downstream Logical Channel FIFO Interrupt Status registers.

Register 0x004: Miscellaneous Interrupt Statuses

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ROOLI	X
Bit 2	R	UPCBI	X
Bit 1	R	UCIFI	X
Bit 0	R	DCIFI	X

DCIFI:

This bit indicates whether there is a pending interrupt for the Downstream Cell Interface. If DCIFI is logic 1, at least one interrupt status bit within the Downstream Cell Interface Interrupt Status register that has its corresponding enable set is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Downstream Cell Interface Interrupt Status register.

UCIFI:

This bit indicates whether there is a pending interrupt for the Upstream Cell Interface. If UCIFI is logic 1, the interrupt status bit in the Upstream Cell Interface Configuration And Interrupt Status register has its corresponding enable set and is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Upstream Cell Interface Configuration and Interrupt Status register.

UPCBI:

This bit indicates whether there is a pending interrupt for the Microprocessor Cell Buffer. If UPCBI is logic 1, at least one interrupt status bit within the Microprocessor Cell Buffer Interrupt Control and Status register that has its corresponding enable set is a logic 1.

This bit is not self-clearing; it is only cleared to logic 0 by reading the Microprocessor Cell Interrupt Status register.

ROOLI:

The Reference Out of Lock interrupt (ROOLI) status is a logic 1 if the ROOLV bit of the Clock Monitor register has changed state since the last time this register was read. The ROOLI bit is reset when this register is read.

Register 0x005: Control Channel Base Address

Bit	Type	Function	Default
Bit 7	R/W	CCBA[10]	0
Bit 6	R/W	CCBA[9]	0
Bit 5	R/W	CCBA[8]	0
Bit 4	R/W	CCBA[7]	0
Bit 3	R/W	CCBA[6]	0
Bit 2	R/W	CCBA[5]	0
Bit 1	R/W	CCBA[4]	0
Bit 0	R/W	CCBA[3]	0

CCBA[10:3]

This register in conjunction with the CCBA[11] bit of the Control Channel Base Address MSB register determines the location of the control channels for the S/UNI-VORTEX within the available address space for the purposes of polling and transfer selection. This register is only relevant to the downstream direction; no address remapping is done in the upstream.

The value of CCBA[11:3]*8 is subtracted from the TADR[11:0] input value sampled. If the difference is less than 8, TPA will drive the buffer availability status (provided the TPAEN register bit is logic 1) of the control channel whose link index (the ‘n’ in TXDn+/- and RXDn+/-) matches the difference.

The value of CCBA[11:3]*8 is subtracted from the ADDR[11:0] value encoded in the cell structures (see Fig. 3) received on TDAT[15:0]. If the difference is less than 8, the cell shall be written to the control channel buffer whose link index matches the difference.

Register 0x006: Control Channel Base Address MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	CCBA[11]	0

CCBA[11]

This is the most significant bit of the Control Channel Base Address.

Register 0x007: Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ROOLE	0
Bit 3	R	ROOLV	X
Bit 2	R	REFCLKA	X
Bit 1	R	RCLKA	X
Bit 0	R	TCLKA	X

This register provides activity monitoring of the S/UNI-VORTEX clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

The register also reports the state of the clock synthesis unit that generates the internal clocks.

TCLKA:

The TCLK active (TCLKA) bit monitors for low to high transitions on the TCLK transmit FIFO clock input. TCLKA is set high on a rising edge of TCLK, and is set low when this register is read.

RCLKA:

The RCLK active (RCLKA) bit monitors for low to high transitions on the RCLK receive FIFO clock input. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transitions on the REFCLK reference clock input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read.

ROOLV:

The reference out of lock status indicates the clock synthesis phase locked loop is unable to lock to the reference on REFCLK. ROOLV is a logic one if the synthesized clock frequency is not within 488 ppm of eight times the REFCLK frequency.

ROOLE:

The ROOLE bit is an interrupt enable for the transmit reference out of lock status. When ROOLE and the Master Interrupt Enable bit of the Master Configuration register are set to logic one, and the INTB output is asserted low when the ROOLV bit changes state.

Register 0x008: Downstream Cell Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	H5UDF	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	INADDUDF	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	PREPEND	0
Bit 1		Unused	X
Bit 0	R/W	PTYP	0

PTYP:

The Parity Type (PTYP) bit selects even or odd parity for input TPRTY. When set to logic 1, TPRTY is the even parity bit for TDAT[15:0]. When set to logic 0, TPRTY is the odd parity bit for TDAT[15:0].

PREPEND:

The PREPEND bit determines whether a word is prepended to each cell. When PREPEND is logic 1, the optional “Word 1” illustrated in Fig. 3 (p. 34) is included in the data structure expected on TDAT[15:0].

Reserved:

The Reserved bit should be set be logic 0 for correct operation.

INADDUDF:

The INADDUDF (inband addressing in UDF byte) bit re-locates the inband address. When this bit is set, the logical channel address for in band selection is located in the twelve lower bits of the H5 and UDF bytes and there is no extended address word in front of the prepend word. The H5UDF bit must also be set (its default value) if this bit is set or the interface will not function correctly.

Although the ability to carry the inband address in the H5/UDF fields is provided for compatibility with devices that cannot generate a prepend, there are a couple of constraints that must be respected in this configuration:

1. The logical channel participating in a cell transfer cannot be polled until nine TCLK periods after the cell transfer is complete.

2. Once the cell transfer is started, the TENB input must remain low until after the H5/UDF word has been transferred. After that, it is permissible for TENB to toggle high to momentarily halt the cell transfer.

H5UDF:

The H5UDF bit determines whether or not the H5/UDF octets are included in cells transferred over the interface. When H5UDF is logic 1 (default), the H5 and UDF octets are included, i.e. the optional “Word 4” illustrated in Fig. 3 (p. 32) is included in the data structure expected on TDAT[15:0].

Register 0x00A: Downstream Cell Interface Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	CELLXFERRE	0
Bit 0	R/W	PARERRE	0

The Master Interrupt Enable bit of the Master Configuration register must also be logic 1 for these enables to take effect.

CELLXFERRE:

The Cell Transfer Error Interrupt Enable (CELLXFERRE) register bit is the interrupt enable for invalid start of cell. When a start of cell occurs when not expected, INTB is asserted low if this bit is set to logic 1. No external interrupt is generated if this bit is set to zero (Even if the interrupt is not enabled, it is always reported in the Downstream Cell Interface Interrupt Status register).

PARERRE:

The Parity Error Interrupt Enable (PARRERRE) register bit is the interrupt enable for invalid parity over the TDAT[15:0] data bus. When a parity error occurs over the TDAT[15:0] data bus, an external interrupt is generated if this bit is set to one. No external interrupt is generated if this bit is set to zero (Even if the interrupt is not enabled, it is always reported in the Downstream Cell Interface Interrupt Status register).

Reserved:

This bit must be logic 0 for correct operation.

Register 0x00B: Downstream Cell Interface Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CELLXFERRI	X
Bit 0	R	PARERRI	X

CELLXFERRI:

The Cell Transfer Error Interrupt Status (CELLXFERRI) read only register bit reports the current status of the interrupt for invalid start of cell. When TSX is asserted when not expected, an interrupt is generated. The interrupt is reset when this register is read.

The same event that asserts this bit may also result in a corrupted cell being transmitted on a high-speed serial link.

PARERRI:

The Parity Error Interrupt Status (PARERRI) read only register bit reports the current status of the interrupt for invalid parity over the input data bus. When a parity error occurs over the TDAT[15:0] data bus, an interrupt is generated. The interrupt is reset when this register is read.

Register 0x00C: Upstream Cell Interface Configuration and Interrupt Status

Bit	Type	Function	Default
Bit 7	R	CELLXFERRI	X
Bit 6	R/W	CELLXFERRE	0
Bit 5		Unused	X
Bit 4	R/W	INADDUDF	0
Bit 3	R/W	H5UDF	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	PREPEND	0
Bit 0	R/W	PTYP	0

PTYP:

The Parity Type (PTYP) bit selects even or odd parity for the RPRTY output. When set to logic 1, RPRTY completes even parity bit for RDAT[15:0]. When set to logic 0, RPRTY completes odd parity bits for RDAT[15:0].

PREPEND:

The PREPEND bit determines whether a word is prepended to each cell. When PREPEND is logic 1, the optional “Word 1” illustrated in Fig. 3 (p. 34) is included in the data structure presented on RDAT[15:0].

Reserved:

This bit must be logic 0 for correct operation.

H5UDF:

The H5UDF bit determines whether or not the H5/UDF octets are included in cells transferred over the interface. When H5UDF is logic 1 (default), the H5 and UDF octets are included, i.e. the optional “Word 4” illustrated in Fig. 3 (p. 32) is included in the data structure presented on RDAT[15:0].

INADDUDF:

The INADDUDF (inband addressing in UDF byte) bit re-locates the inband address. When this bit is set, the logical channel address for in band selection is located in the fourteen lower bits of the H5 and UDF bytes and there is no extended address word in front of the prepend word. This bit supercedes the H5UDF bit, in that it forces the inclusion of “Word 4”. This bit has no effect if the RANYPHY input is logic 1.

CELLXFERRE:

The Cell Transfer Error Interrupt Enable (CELLXFERRE) bit allows the generation of an interrupt on an invalid selection by an external master device. This occurs when a cell transfer is attempted, but the VORTEX has indicated no cell is available by returning RPA low when polled. When CELLXFERRE is set to logic 1, the INTB output is asserted low when the CELLXFERRI bit is logic 1.

CELLXFERRI:

The CELLXFERRI bit provides a status of the Cell Transfer Error Interrupt. This interrupt status is asserted when an external master device selects the Upstream Cell Interface (i.e. RADR[4:0] value equals the state of VADR[4:0] when RENB is last sampled high) for a transfer without a cell being available. This bit does not indicate the case where RENB is held low beyond the end of a cell transfer, when there is not a second cell to transfer. This bit is reset immediately after a read to this register.

Register 0x010: Microprocessor Cell Buffer Interrupt Control and Status

Bit	Type	Function	Default
Bit 7	R	EXTCRCERRI	X
Bit 6	R	EXTRDYI	X
Bit 5	R	INSOVRI	X
Bit 4	R	INSRDYI	X
Bit 3	R/W	EXTCRCERRE	0
Bit 2	R/W	EXTRDYE	0
Bit 1	R/W	INSOVRE	0
Bit 0	R/W	INSRDYE	0

The Master Interrupt Enable bit of the Master Configuration register must also be logic 1 for the interrupt enables to take effect.

INSRDYE:

The INSRDYE bit allows the generation of an interrupt when an Insert FIFO becomes available. When INSRDYE is set to logic 1, the INTB output is asserted low when the INSRDYI bit is logic 1.

INSOVRE:

The INSOVRE bit controls the generation of an interrupt upon an overflow of an insert buffer. When INSOVRE is set to logic 1, the INTB output is asserted low when the INSOVRI bit is logic 1.

EXTRDYE:

The EXTRDYE bit allows the generation of an interrupt when an Extract FIFO becomes ready. When EXTRDYE is set to logic 1, the INTB output is asserted low when the EXTRDYI bit is logic 1.

EXTCRCERRE:

The EXTCRCERRE bit controls the generation of the interrupt upon a CRC-32 error. When EXCRCERRE is set to logic 1, the INTB output is asserted low when the EXTCRCERRI bit is logic 1.

INSRDYI:

The INSRDYI bit provides a status of the Insert FIFOs Ready Interrupt. This bit is set to logic 1 when one of the Insert FIFOs becomes ready to accept a

cell (i.e. a cell is transferred from a full FIFO) or upon the completion of a cell write if at least one more cell can be written. The ready status of a specific FIFO is indicated by a logic 1 at the corresponding bit of the Microprocessor Insert FIFO Ready register. The INSRDYI bit is reset immediately after a read to this register.

INSOVRI:

The INSOVRI bit indicates the status of the write access to a Microprocessor Insert FIFO. This bit is set to logic 1 when a write access has being attempted to a full Microprocessor Insert FIFO and the data has been discarded. This bit is reset immediately after a read to this register.

EXTRDYI:

The EXTRDYI bit provides a status of the Microprocessor Extract FIFOs Ready Interrupt. This bit is set to logic 1 when one of the Microprocessor Extract FIFOs becomes ready for a cell read (i.e. upon reception of the only cell in the FIFO) or upon the completion of a cell read if there is at least one more cell to be read from the FIFO. Ready status of a specific FIFO is indicated by a logic 1 at the corresponding bit of the Microprocessor Extract FIFO Ready register. The EXTRDYI bit is reset immediately after a read to this register.

EXTCRCERRI:

The EXTCRCERRI bit indicates the CRC-32 status of a cell read from an Extract FIFO. When the EXTCRCCHK bit is set to logic 1, the EXTCRCERRI bit is updated when the last byte of a cell is read by the microprocessor. It is set to logic 1 if the value of the Extract CRC Accumulator register differs from the expected CRC-32 remainder polynomial. Otherwise, it is set to logic 0.

This bit is also reset immediately after a read to this register.

Register 0x011: Microprocessor Insert FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	INSCRCEND	0
Bit 4	R/W	INSCRCPR	1
Bit 3	W	INSRST	X
Bit 2	R/W	INSFSEL[2]	0
Bit 1	R/W	INSFSEL[1]	0
Bit 0	R/W	INSFSEL[0]	0

INSFSEL[2:0]:

The INSFSEL[2:0] bits are used to select the one of eight Microprocessor Insert FIFOs for a cell write operation. The Insert FIFO has to be selected prior to starting a cell transfer. The value of INSFSEL[2:0] corresponds to the index of the serial link (i.e. the ‘n’ in TXDn+/-) on which the cell will be presented. The Microprocessor Insert FIFO has to be selected prior to starting the cell transfer. Due to synchronization delays, a read of the Microprocessor Cell Buffer Data register should not be initiated until two REFCLK periods after completion of the write of these bits.

INSRST:

The INSRST bit allows the microprocessor to abort a cell write to the Microprocessor Insert FIFO. If INSRST is set to a logic 1 when previously logic 0, the insert write pointer is reset without completing the transaction. Setting INSRST after the last write (i.e. at the beginning of the next cell) has no effect. To abort a cell, the microprocessor must have written at least the first byte of the cell but less than 56 bytes.

INSRST is not readable.

This bit is cleared on every write to Microprocessor Cell Data register.

INSCRCPR:

The INSCRCPR bit is used to force the value of the Insert CRC-32 accumulation register to its preset value. If INSCRCPR is set to logic 1, the Insert CRC-32 accumulation register is kept to its preset value. If INSCRCPR is set to logic 0, CRC-32 calculations are performed on inserted cells. CRC-

32 calculations are performed on the cell payload bytes being written to the Microprocessor Cell Data register.

Due to synchronization delays, a write of the Microprocessor Cell Buffer Data register should not be initiated until two REFCLK periods after completion of the write of this bit.

INSCRCEND:

The INSCRCEND bit is used to indicate that the following inserted cell is the last one of the CPCS-PDU. Setting this bit to logic 1 will cause the last four bytes of the cell transferred from the microprocessor to be replaced by the value of the ones complement of the Insert CRC-32 Accumulation register.

Register 0x012: Microprocessor Extract FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	EXTCRCCHK	0
Bit 4	R/W	EXTCRCPR	1
Bit 3	W	EXTABRT	X
Bit 2	R/W	EXTFSEL[2]	0
Bit 1	R/W	EXTFSEL[1]	0
Bit 0	R/W	EXTFSEL[0]	0

EXTFSEL[2:0]:

The EXTFSEL [2:0] bits are used to select the one of eight Microprocessor Extract FIFOs for a cell read operation. The value of EXTFSEL[2:0] corresponds to the index of the serial link (i.e. the ‘n’ in RXDn+/-) on which the cell was received. The Microprocessor Extract FIFO has to be selected prior to starting the cell transfer. Due to synchronization delays, a read of the Microprocessor Cell Buffer Data register should not be initiated until two REFCLK periods after completion of the write of these bits.

EXTABRT:

The EXTABRT bit allows the microprocessor to discard a cell without reading the remaining contents. If EXTABRT is set to a logic 1 when previously logic 0, the extract pointer is reset, effectively discarding the remaining contents of the cell. Setting EXTABRT after the last read (i.e. at the beginning of the next cell) has no effect. To abort a cell, the microprocessor must have read at least the first word of the cell but no more than 56 bytes.

Due to synchronization delays, no cell extraction operation should be initiated until two REFCLK periods after completion of the write of this bit.

EXTABRT is not readable.

It is cleared on every read from normal mode Microprocessor Cell Data register.

EXTCRCPR:

The EXTCRCPR bit is used to force the value of the Extract CRC-32 accumulation register to its preset value. If EXTCRCPR is set to logic 1, the Insert CRC-32 accumulation register is kept to its preset value. If EXTCRCPR is set to logic 0, CRC-32 verification is performed on extracted cells. The CRC-32 calculations are performed on the bytes being read from the location of the Microprocessor Cell Data register corresponding to the payload of extract cells.

Due to synchronization delays, a read of the Microprocessor Cell Buffer Data register should not be initiated until two REFCLK periods after completion of the write of this bit.

EXTCRCCHK:

The EXTCRCCHK bit is used to enable the CRC-32 field check. Setting this bit to logic 1 will cause the S/UNI-VORTEX to verify if the value of the Extract CRC-32 Accumulation register is equal to the expected CRC-32 remainder polynomial at the end of a cell read access by the microprocessor. If EXTCRCCHK is logic 1, the EXTCRCERRI bit will be set to logic 1 if the CRC-32 is incorrect.

Register 0x013: Microprocessor Insert FIFO Ready

Bit	Type	Function	Default
Bit 7	R	INSRDY[7]	X
Bit 6	R	INSRDY[6]	X
Bit 5	R	INSRDY[5]	X
Bit 4	R	INSRDY[4]	X
Bit 3	R	INSRDY[3]	X
Bit 2	R	INSRDY[2]	X
Bit 1	R	INSRDY[1]	X
Bit 0	R	INSRDY[0]	X

INSRDY[7:0]:

The INSRDY[7:0] bits provide the ready status of the Microprocessor Insert FIFOs. A logic 1 in a INSRDY[7:0] bit indicates that the corresponding Microprocessor Insert FIFO is ready to accept a cell. The bit index corresponds to the serial link index.

Note that the INSRDY bit for the FIFO currently being written will always return a logic 0.

Register 0x014: Microprocessor Extract FIFO Ready

Bit	Type	Function	Default
Bit 7	R	EXTRDY[7]	X
Bit 6	R	EXTRDY[6]	X
Bit 5	R	EXTRDY[5]	X
Bit 4	R	EXTRDY[4]	X
Bit 3	R	EXTRDY[3]	X
Bit 2	R	EXTRDY[2]	X
Bit 1	R	EXTRDY[1]	X
Bit 0	R	EXTRDY[0]	X

EXTRDY[7:0]:

The EXTRDY[7:0] bits provide the ready status of the Microprocessor Extract FIFOs. A logic 1 in a EXTRDY[7:0] bit indicates that the corresponding Microprocessor Extract FIFO has at least one cell available for reading. The bit index corresponds to the serial link index.

Note that the EXTRDY bit for the FIFO currently being read will always return a logic 0.

Register 0x015: Insert CRC-32 Accumulator (LSB)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[7]	1
Bit 6	R/W	INSCRCACC[6]	1
Bit 5	R/W	INSCRCACC[5]	1
Bit 4	R/W	INSCRCACC[4]	1
Bit 3	R/W	INSCRCACC[3]	1
Bit 2	R/W	INSCRCACC[2]	1
Bit 1	R/W	INSCRCACC[1]	1
Bit 0	R/W	INSCRCACC[0]	1

Register 0x016: Insert CRC-32 Accumulator (2nd byte)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[15]	1
Bit 6	R/W	INSCRCACC[14]	1
Bit 5	R/W	INSCRCACC[13]	1
Bit 4	R/W	INSCRCACC[12]	1
Bit 3	R/W	INSCRCACC[11]	1
Bit 2	R/W	INSCRCACC[10]	1
Bit 1	R/W	INSCRCACC[9]	1
Bit 0	R/W	INSCRCACC[8]	1

Register 0x017: Insert CRC-32 Accumulator (3rd byte)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[23]	1
Bit 6	R/W	INSCRCACC[22]	1
Bit 5	R/W	INSCRCACC[21]	1
Bit 4	R/W	INSCRCACC[20]	1
Bit 3	R/W	INSCRCACC[19]	1
Bit 2	R/W	INSCRCACC[18]	1
Bit 1	R/W	INSCRCACC[17]	1
Bit 0	R/W	INSCRCACC[16]	1

Register 0x018: Insert CRC-32 Accumulator (MSB)

Bit	Type	Function	Default
Bit 7	R/W	INSCRCACC[31]	1
Bit 6	R/W	INSCRCACC[30]	1
Bit 5	R/W	INSCRCACC[29]	1
Bit 4	R/W	INSCRCACC[28]	1
Bit 3	R/W	INSCRCACC[27]	1
Bit 2	R/W	INSCRCACC[26]	1
Bit 1	R/W	INSCRCACC[25]	1
Bit 0	R/W	INSCRCACC[24]	1

INSCRCACC[31:0]:

The four registers of INSCRCACC[31:0] allows the microprocessor to read or write the contents of the Insert CRC Accumulator register. This register accumulates the CRC-32 value over the data being written to a Microprocessor Insert FIFO.

The rising edge of WRB for two successive write accesses to these registers must separated by at least three REFCLK periods.

Register 0x019: Extract CRC-32 Accumulator (LSB)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[7]	1
Bit 6	R/W	EXTCRCACC[6]	1
Bit 5	R/W	EXTCRCACC[5]	1
Bit 4	R/W	EXTCRCACC[4]	1
Bit 3	R/W	EXTCRCACC[3]	1
Bit 2	R/W	EXTCRCACC[2]	1
Bit 1	R/W	EXTCRCACC[1]	1
Bit 0	R/W	EXTCRCACC[0]	1

Register 0x01A: Extract CRC-32 Accumulator (2nd byte)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[15]	1
Bit 6	R/W	EXTCRCACC[14]	1
Bit 5	R/W	EXTCRCACC[13]	1
Bit 4	R/W	EXTCRCACC[12]	1
Bit 3	R/W	EXTCRCACC[11]	1
Bit 2	R/W	EXTCRCACC[10]	1
Bit 1	R/W	EXTCRCACC[9]	1
Bit 0	R/W	EXTCRCACC[8]	1

Register 0x1B: Extract CRC-32 Accumulator (3rd byte)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[23]	1
Bit 6	R/W	EXTCRCACC[22]	1
Bit 5	R/W	EXTCRCACC[21]	1
Bit 4	R/W	EXTCRCACC[20]	1
Bit 3	R/W	EXTCRCACC[19]	1
Bit 2	R/W	EXTCRCACC[18]	1
Bit 1	R/W	EXTCRCACC[17]	1
Bit 0	R/W	EXTCRCACC[16]	1

Register 0x01C: Extract CRC-32 Accumulator (MSB)

Bit	Type	Function	Default
Bit 7	R/W	EXTCRCACC[31]	1
Bit 6	R/W	EXTCRCACC[30]	1
Bit 5	R/W	EXTCRCACC[29]	1
Bit 4	R/W	EXTCRCACC[28]	1
Bit 3	R/W	EXTCRCACC[27]	1
Bit 2	R/W	EXTCRCACC[26]	1
Bit 1	R/W	EXTCRCACC[25]	1
Bit 0	R/W	EXTCRCACC[24]	1

EXTCRCACC[31:0]:

The four registers of EXTCRCACC[31:0] allows the microprocessor to read or write the contents of the Insert CRC Accumulator register. The Extract CRC-32 Accumulator Register accumulates the CRC-32 value of the data being read from a Microprocessor Extract FIFO.

The rising edge of WRB for two successive write accesses to these registers must separated by at least three REFCLK periods.

Register 0x01D: Microprocessor Cell Buffer Data

Bit	Type	Function	Default
Bit 7	R/W	MCDAT[7]	X
Bit 6	R/W	MCDAT[6]	X
Bit 5	R/W	MCDAT[5]	X
Bit 4	R/W	MCDAT[4]	X
Bit 3	R/W	MCDAT[3]	X
Bit 2	R/W	MCDAT[2]	X
Bit 1	R/W	MCDAT[1]	X
Bit 0	R/W	MCDAT[0]	X

MCDAT[7:0]:

The MCDAT[7:0] is used to write to the selected Microprocessor Insert FIFO or read from the selected Microprocessor Extract FIFO by the microprocessor.

When inserting cells, the Microprocessor Insert FIFO Ready register may be polled to determine which FIFO is ready to receive a cell. Alternately, an interrupt may be generated by setting the Microprocessor Insert FIFO Interrupt Enable Register bit accordingly. Selection of the Microprocessor Insert FIFO is done by writing the INSFSEL[2:0] bits of the Microprocessor Insert FIFO Control Register. A cell is transferred to a Microprocessor Insert FIFO by performing successive write accesses to the Microprocessor Cell Data register. The rising edge of WRB for two successive write accesses to this register must separated by at least three REFCLK periods.

When extracting cells, the Microprocessor Extract FIFO Ready register may be polled to determine which FIFO has a cell available to be read. Alternately, an interrupt may be generated by setting the Microprocessor Extract FIFO Interrupt Enable Register bit accordingly. Selection of the Microprocessor Extract FIFO is done by writing the EXTFSEL[2:0] bits of the Extract FIFO Control Register. A cell is transferred from an Extract FIFO by performing successive read accesses to the Microprocessor Cell Data register. The falling edge of RDB for two successive read accesses to this register must separated by at least three REFCLK periods.

Registers 0x080, 0x0A0, 0x0C0, 0x0E0, 0x100, 0x120, 0x140, 0x160: Receive High Speed Serial Configuration

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	1
Bit 5		Unused	X
Bit 4	R/W	CNTCELLERR	0
Bit 3	R/W	CELLCRC	0
Bit 2	R/W	PREPEND	0
Bit 1	R/W	USRHDR[1]	1
Bit 0	R/W	USRHDR[0]	0

These registers configure, on a per-link basis, the format of the cells expected on the eight RXDn+/- serial links.

USRHDR[1:0]:

The USRHDR[1:0] bits determine the length of the expected User Header field of the received cells.

USRHDR[1:0]	Bytes in User Header
00	4
01	5
10	6
11	Reserved

PREPEND:

The PREPEND bit determines if the User Prepend field is expected to exist in the received cells. If PREPEND is logic 1, a two byte User Prepend is expected to follow the System Prepend field.

CELLCRC:

The CELLCRC bit determines whether the entire high speed serial data structure is expected to be protected by a CRC-8 code word. The PREPEND bit must be logic 1 for this bit to have effect. If CELLCRC and PREPEND are logic 1, the second User Prepend byte is expected to contain the CRC-8

syndrome for the preceding cell. A non-zero remainder shall result in a maskable interrupt and, if enabled by the CNTCELLERR bit, a cell error count increment. If CELLCRC is logic 0, the contents of the second User Prepend byte are not examined.

CNTCELLERR:

The CNTCELLERR bit allows the redefinition of the Receive High-Speed Serial HCS Error Count register to include the number of cell CRC-8 errors. If CNTCELLERR and CELLCRC are logic 1, each non-zero remainder for the CRC-8 protecting the entire cell or non-zero remainder HCS results in an increment. (Simultaneous cell CRC-8 and HCS errors result in a single increment.) If either CNTCELLERR or CELLCRC is logic 0, the count represents the number of HCS errors.

DDSCR and HDSCR:

The Disable Descramble (DDSCR) and Header Descramble enable (HDSCR) bits control the descrambling of the cell by the $x^{43} + 1$ self-synchronous descrambler. When DDSCR is a logic one, cell header and payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled and cell header descrambling is determined by HDSCR. HDSCR enables descrambling of the System Prepend, User Prepend, User Header, and HCS byte collectively. The operation of the DDSCR and HDSCR bits is summarized below:

DDSCR	HDSCR	Operation
1	X	Cell payload and header descrambling is disabled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	0	Cell payload is descrambled. Cell header is left unscrambled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	1	Cell payload and header are both descrambled.

Registers 0x081, 0x0A1, 0x0C1, 0x0E1, 0x101, 0x121, 0x141, 0x161: Receive High-Speed Serial Cell Filtering Configuration/Status

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	Reserved	0
Bit 4	R	OCDV	X
Bit 3		Unused	X
Bit 2	R	ACTV	X
Bit 1	R	LCDV	X
Bit 0	R	LOSV	X

These registers provide the status of each individual RXDn+/- serial link.

LOSV:

The LOSV gives the Loss of Signal state. LOSV becomes logic 1 upon 2048 bit periods (13.2 μs at 155.52 Mb/s) without a signal transition in the scrambled data. LOSV becomes logic 0 when a signal transition has occurred in each of 16 consecutive intervals of 16 bit periods each.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCDV is logic 1, an out of cell delineation (OCD) defect has persisted for 1318 cells. LCDV becomes logic 0 when cell delineation has been maintained for 1318 cells.

ACTV:

The ACTV bit provides the debounced state of the ACTIVE bit in the cell prepend. ACTV reflects the state of the ACTIVE bit when it has been the same for three consecutive valid cells.

OCDV:

The OCDV bit indicates the cell delineation state. When OCDV is logic 1, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries. When OCDV is logic 0, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of a HCS error. When HCSPASS is logic 0, cells containing a HCS error are dropped. When HCSPASS is logic 1, cells are passed to the FIFO interface regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the ‘SYNC’ state, and hence will never lose cell delineation. This bit is provided for diagnostic purposes only.

Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

Reserved:

This bit must be logic 0 for correct operation.

Registers 0x082, 0x0A2, 0x0C2, 0x0E2, 0x102, 0x122, 0x142, 0x162: Receive High-Speed Serial Interrupt Enables

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	HCSE	0
Bit 5	R/W	XFERE	0
Bit 4	R/W	OCDE	0
Bit 3	R/W	CELLERRE	0
Bit 2	R/W	ACTE	0
Bit 1	R/W	LCDE	0
Bit 0	R/W	LOSE	0

These registers allow changes in the Receive High-Speed Serial Cell Filtering Configuration/Status register bits, HCS errors and counter transfers to cause assertion low the INTB output.

The Master Interrupt Enable bit of the Master Configuration register must also be logic 1 for the interrupt enables to take effect.

LOSE:

The LOSE bit enables the generation of an interrupt upon a change in the Loss of Signal state. When LOSE is set to logic 1, the interrupt is enabled.

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD (Loss of Cell Delineation) state. When LCDE is set to logic 1, the interrupt is enabled.

ACTE:

The ACTE bit enables the generation of an interrupt due to a change in the ACTV register bit. When ACTE is set to logic 1, the interrupt is enabled.

CELLERRE:

The CELLERRE bit enables the generation of an interrupt due to a non-zero remainder of the CRC-8 protecting the entire cell. When CELLERRE and CELLCRC are set to logic 1, the interrupt is enabled.

OCDE:

The OCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OCDE is set to logic 1, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a HCS error. When HCSE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive cell counter and HCS error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

Registers 0x083, 0x0A3, 0x0C3, 0x0E3, 0x103, 0x123, 0x143, 0x163: Receive High-Speed Serial Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OVR	X
Bit 6	R	XFERI	X
Bit 5	R	HCSI	X
Bit 4	R	OCDI	X
Bit 3	R	CELLERRI	X
Bit 2	R	ACTI	X
Bit 1	R	LCDI	X
Bit 0	R	LOSI	X

These registers provide an indication of events that have occurred since the last time it was read. These bits are not affected by the programming of the Receive High-Speed Serial Interrupt Enables register, which only determines whether the status of the bits in these registers is propagated to the INTB output.

LOSI:

The LOSI bit is set to logic 1 whenever the associated LOSV register bit changes state. This bit is reset immediately after a read to this register.

LCDI:

The LCDI bit is set to logic 1 whenever the associated LCDV register bit changes state. This bit is reset immediately after a read to this register.

ACTI:

The ACTI bit is set to logic 1 whenever the associated ACTV register bit changes state. This bit is reset immediately after a read to this register.

CELLERRI:

The CELLERRI bit is set high when a non-zero remainder occurs for the CRC-8 protecting the entire cell. This bit is reset immediately after a read to this register.

HCSI:

The HCSI bit is set high when a HCS error is detected. This bit is reset immediately after a read to this register.

XFERI:

The XFERI bit indicates that a transfer of accumulated counter data has occurred. A logic 1 in this bit position indicates that the receive cell counter and error counter holding registers have been updated. This update is initiated by writing to the associated (i.e. this link only) Receive High-Speed Serial HCS Error Count register, one of the associated Receive High-Speed Serial Cell Counter registers or the Load Performance Meters (0x000) register. This bit is reset immediately after a read to this register.

OCDI:

The OCDI bit is set high when the cell delineation state machine enters or exits the SYNC state. The current value of the OCD state is available in the OCDV bit in the associated Receive High-Speed Serial Cell Filtering Configuration/Status register. The OCDI bit is reset immediately after a read to this register.

OVR:

The OVR bit is the overrun status of the associated accumulation holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred, and that the contents of the receive cell counter and HCS error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0x084, 0x0A4, 0x0C4, 0x0E4, 0x104, 0x124, 0x144, 0x164: Receive High-Speed Serial HCS Error Count

Bit	Type	Function	Default
Bit 7	R	HCSERR[7]	X
Bit 6	R	HCSERR[6]	X
Bit 5	R	HCSERR[5]	X
Bit 4	R	HCSERR[4]	X
Bit 3	R	HCSERR[3]	X
Bit 2	R	HCSERR[2]	X
Bit 1	R	HCSERR[1]	X
Bit 0	R	HCSERR[0]	X

HCSERR[7:0]:

If the either the CELLCRC or CNTCELLERR bit of the Receive High Speed Serial Configuration register is logic 0, the HCSERR[7:0] bits indicate the number of HCS error events that occurred during the last accumulation interval on the associated RXDn+/- link.

If the CELLCRC and CNTCELLERR bits are logic 1, the HCSERR[7:0] bits indicate the number of cells with non-zero cell CRC-8 or HCS remainders.

The contents of this register become valid a maximum of 300 ns after a transfer is triggered by a write to this register, one of the associated (i.e. this link only) Receive High-Speed Serial Cell Counter registers or the Load Performance Meters (0x000) register, and remain valid until another transfer is triggered.

The count saturates at all ones.

Registers 0x085, 0x0A5, 0x0C5, 0x0E5, 0x105, 0x125, 0x145, 0x165: Receive High-Speed Serial Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Registers 0x086, 0x0A6, 0x0C6, 0x0E6, 0x106, 0x126, 0x146, 0x166: Receive High-Speed Serial Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Registers 0x087, 0x0A7, 0x0C7, 0x0E7, 0x107, 0x127, 0x147, 0x167: Receive High-Speed Serial Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[23]	X
Bit 6	R	RCELL[22]	X
Bit 5	R	RCELL[21]	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[23:0]:

The RCELL[23:0] bits indicate the number of valid cells received during the last accumulation interval. Cells filtered due to HCS errors or as stuff cells are not counted. The counter should be polled at least every 30 seconds to avoid saturation.

The contents of these registers become valid a maximum of 300 ns after a transfer is triggered by a write to these registers, the associated Receive High-Speed Serial HCS Error Count register or the Load Performance Meters (0x000) register, and remain valid until another transfer is triggered.

The count saturates at all ones.

Registers 0x088, 0x0A8, 0x0C8, 0x0E8, 0x108, 0x128, 0x148, 0x168: Receive High-Speed Serial FIFO Overflow

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	UPFOVRI	X
Bit 4	R	FOVRI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPFOVRE	0
Bit 0	R/W	FOVRE	0

The status bits in this register provide an indication of cell loss due to over flows in the Upstream Link FIFOs. Generally, the FOVRI and UPFOVRI status bits should never be asserted; their assertion would indicate that the flow control protocol is being ignored.

FOVRE:

The FOVRE bit enables the assertion of the INTB output upon FOVRI transitioning high. When FOVRE is set to logic 1, the interrupt is enabled.

UPFOVRE:

The UPFOVRE bit enables the assertion of the INTB output upon UPFOVRI transitioning high. When UPFOVRE is set to logic 1, the interrupt is enabled.

FOVRI:

The FOVRI bit is set to logic 1 when a valid cell is lost due to an over flow of the associated Upstream Link FIFO. This bit is reset immediately after a read to this register.

UPFOVRI:

The UPFOVRI bit is set to logic 1 when a valid control channel cell is lost due to an over flow of the associated Upstream Microprocessor Cell Buffer. This bit is reset immediately after a read to this register.

Registers 0x089, 0x0A9, 0x0C9, 0x0E9, 0x109, 0x129, 0x149, 0x169: Upstream Round Robin Weight

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RRW[1]	0
Bit 0	R/W	RRW[0]	0

These registers differentiate the access to the RDAT[15:0] bandwidth for each serial link. The number of opportunities queued cells have of being transferred over RDAT[15:0] is proportional to the programmed weight. Under uncongested conditions, a higher weight will result in a slightly lower cell delay variation (CDV). Under congested situations (i.e. the instantaneous offered load exceeds the RDAT[15:0] bandwidth), the ultimate maximum throughput of a link before cell loss (at the cell buffers on the line card) is proportional to the weighting.

Note that if several S/UNI-VORTEX devices reside on a RDAT[7:0] bus, the allocation of bandwidth between the S/UNI-VORTEX devices is dependant on the polling algorithm employed by the bus master.

RRW[1:0]

The Round Robin Weight (RRW(1:0]) selects one of four possible polling weights for the associated serial link.

RRW[1:0]	Weight
01	1
10	2
11	3
00	4

Registers 0x08A, 0x0AA, 0x0CA, 0x0EA, 0x10A, 0x12A, 0x14A, 0x16A: Logical Channel Base Address

Bit	Type	Function	Default
Bit 7	R/W	LCBA[10]	0
Bit 6	R/W	LCBA[9]	0
Bit 5	R/W	LCBA[8]	0
Bit 4	R/W	LCBA[7]	0
Bit 3	R/W	LCBA[6]	0
Bit 2	R/W	LCBA[5]	0
Bit 1	R/W	LCBA[4]	0
Bit 0	R/W	LCBA[3]	0

LCBA[10:3]

These registers in conjunction with the LCBA[11] bit of the Logical Channel Range / Logical Channel Base Address MSB registers determine the location of the logical channels for the serial links within the available address space for the purposes of polling and transfer selection. This register is only relevant to the downstream direction; no address remapping is done in the upstream.

The value of LCBA[11:3]*8 is subtracted from the TADR[11:0] input value sampled. If the difference is within the range set by the LCAR[1:0] register bits, TPA will drive the buffer availability status (provided the TPAEN register bit is logic 1) of the logical channel whose index matches the difference.

The value of LCBA[11:3]*8 is subtracted from the ADDR[11:0] value encoded in the cell structures (see Fig. 3) received on TDAT[15:0]. If the difference is within the range set by the LCAR[1:0] register bits, the cell shall be written to the logical channel buffer whose index matches the difference.

Note that address wraps are supported. For example, if LCBA[11:3] is 0x1FF and the range is 32 addresses, the addresses from 0xFF8 through 0xFFF and 0x000 through 0x017 are matched.

Register 0x08B, 0x0AB, 0x0CB, 0x0EB, 0x10B, 0x12B, 0x14B, 0x16B: Logical Channel Address Range / Logical Channel Base Address MSB

Bit	Type	Function	Default
Bit 7	R/W	LCAR[1]	0
Bit 6	R/W	LCAR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	LCBA[11]	0

LCAR[1:0]

The Logical Channel Address Range determines the range of addresses relative to the Logical Channel Base Address that corresponds to the logical channels of the serial link. The default maps 32 logical channels to a serial link, but 8, 16 or 24 channels may be mapped to each link to provide a more compact address space and hence allowing support of more channels.

LCAR[1:0]	Addresses Allocated
01	8
10	16
11	24
00	32

The address space is contiguous starting at the associated Logical Channel Base Address. The offset from the base address corresponds to the logical channel index (PHYID[4:0] value encoded in the serialized cell).

LCBA[11]:

This is the most significant bit of the Logical Channel Base Address for the link.

Registers 0x08C, 0x0AC, 0x0CC, 0x0EC, 0x10C, 0x12C, 0x14C, 0x16C: Downstream Logical Channel FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	FOVRE	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset all the logical channel FIFOs for a link. When FIFORST is set to logic 0, the FIFO channels operate normally. When FIFORST is set to logic 1, all the FIFOs are immediately emptied and ignore writes. The FIFOs remain empty and continue to ignore writes until logic 0 is written to FIFORST. This results in a continuous stream of stuff cells on TXDn+/-.

If a user cell is currently being sent over the LVDS link it will likely be corrupted by the reset. If the header portion of the cell has been sent then this corruption will not be detected at the receiver if header error detection is enabled. However it will likely be detected if cell error detection is enabled. See Transmit High-Speed Serial Configuration Register, CELLCRC bit, and Received High-Speed Serial Configuration Register, CELLCRC bit for details.

FOVRE:

The FOVRE bit enables the assertion of the INTB output due to a FIFO overrun error condition. When FOVRE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the interrupt is enabled.

Register 0x08D, 0x0AD, 0x0CD, 0x0ED, 0x10D, 0x12D, 0x14D, 0x16D: Downstream Logical Channel FIFO Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	FOVRI	X

FOVRI:

The FOVRI bit indicates an interrupt due to a logical channel FIFO overrun error condition. A likely cause is an inappropriate programming of the Downstream Logical Channel FIFO Control FIFO Ready Level register for the existing ratio between the TXD+/- bit rate and the TCLK frequency. FOVRI is cleared to logic 0 when the register is read.

Registers 0x08F, 0x0AF, 0x0CF, 0x0EF, 0x10F, 0x12F, 0x14F, 0x16F: Downstream Logical Channel FIFO Ready Level

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FREADY[5]	1
Bit 4	R/W	FREADY[4]	1
Bit 3	R/W	FREADY[3]	0
Bit 2	R/W	FREADY[2]	0
Bit 1	R/W	FREADY[1]	1
Bit 0	R/W	FREADY[0]	0

FREADY[5:0]:

The FIFO Ready Level (FREADY[5:0]) register is used to set the earliest time TPA can be reasserted after a cell has been written into a downstream buffer. Writing a cell into a downstream buffer causes its TPA value to be deasserted. After the number of bytes read from the downstream buffer (and subsequently serialized on TXDn+/-) is greater than or equal to the binary value of FREADY[5:0], the TPA value returned when that channel is polled will be logic 1, thus indicating a write to the logical channel can be initiated. If the buffer is empty when the channel is polled, then FREADY[5:0] is not relevant since TPA will always be asserted on an empty buffer.

FREADY[5:0] must be set such as to avoid a FIFO overflow. It should always be less than the cell length (52, 54 or 56 depending on how the Any-PHY bus is configured). A low value of FREADY[5:0] has the potential to increase the maximum sustained cell rate for a single logical channel, but it has to be large enough to ensure the FIFO writes do not catch up to the FIFO reads. The FREADY[5:0] programming is discussed in the Operations section on Page 127. As a minimum requirement, the programmed value must respect the following constraint to guarantee no cell loss:

$$FREADY > \max(9, 56 - 28 * \frac{f_{REFCLK}}{f_{TCLK}})$$

The default value of 50 is compatible with all permissible clock frequency ranges but it will not be sufficient if a single high speed PHY is all that is connected to the far-end S/UNI-DUPLEX.

Registers 0x090, 0x0B0, 0x0D0, 0x0F0, 0x110, 0x130, 0x150, 0x170: Transmit High-Speed Serial Configuration

Bit	Type	Function	Default
Bit 7	R/W	DSCR	0
Bit 6	R/W	HSCR	1
Bit 5	R/W	Unused	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	CELLCRC	0
Bit 2	R/W	PREPEND	0
Bit 1	R/W	USRHDR[1]	1
Bit 0	R/W	USRHDR[0]	0

These registers configure, on a per-link basis, the format of the cells transmitted on the eight TXDn+/- serial links.

USRHDR[1:0]:

The USRHDR[1:0] bits determine the length of the User Header field of the transmitted cells. The User Header defaults to six bytes.

USRHDR[1:0]	Bytes in User Header
00	4
01	5
10	6
11	Reserved

PREPEND:

The PREPEND bit determines if the User Prepend field is inserted into the transmitted cells. If PREPEND is logic 1, a two byte User Prepend is inserted after the System Prepend field.

CELLCRC:

The CELLCRC bit determines whether the entire high speed serial data structure is protected by a CRC-8 code word. The PREPEND bit must be logic 1 for this bit to have effect. If CELLCRC and PREPEND are logic 1, the second User Prepend byte is overwritten by the CRC-8 syndrome for the

preceding cell. If CELLCRC is logic 0, the contents of the second User Prepend byte are transported transparently.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet for a single cell is inverted prior to insertion. After the insertion, DHCS is automatically reset to logic 0. To invert the HCS octet in another cell, DHCS must be set to logic 1 again.

DSCR and HSCR:

The Disable Scramble enable (DSCR) and Header Scramble enable (HSCR) bits control the scrambling of the cell. When DSCR is logic one, cell header and payload scrambling is disabled. When DSCR is logic zero, payload scrambling is enabled and cell header scrambling is determined by HSCR. HSCR enables scrambling of the System Prepend, User Prepend, User Header, and HCS byte collectively. The operation of the DSCR and HSCR bits is summarized below:

DSCR	HSCR	Operation
1	X	Cell payload and header scrambling is disabled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	0	Cell payload is scrambled. Cell header is left unscrambled. THIS CONFIGURATION SHOULD ONLY BE USED FOR DIAGNOSTIC PURPOSES.
0	1	Cell payload and header are both scrambled.

Registers 0x091, 0x0B1, 0x0D1, 0x0F1, 0x111, 0x131, 0x151, 0x171: Transmit High-Speed Serial Cell Count Status

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register indicates whether the associated Transmit Cell Count registers have been updated with new data and whether this data overwrites unacknowledged data. This status is maintained on a per-serial link basis.

OVR:

The OVR bit is the overrun status of the associated Transmit Cell Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and thus the contents of the Transmit Cell Count registers have been overwritten. OVR is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic 1 in this bit position indicates that the associated Transmit Cell Count registers have been updated. This update is initiated by writing to one of the associated Transmit Cell Count register locations or by writing to the Load Performance Meters (0x000) register. XFERI is set to logic 0 when this register is read.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the associated Transmit Cell Count registers. When XFERE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the INTB output is asserted low if the XFERI bit is a logic 1.

Registers 0x092, 0x0B2, 0x0D2, 0x0F2, 0x112, 0x132, 0x152, 0x172: Transmit High-Speed Serial Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Registers 0x093, 0x0B3, 0x0D3, 0x0F3, 0x113, 0x133, 0x153, 0x173: Transmit High-Speed Serial Cell Counter

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x094, 0x0B4, 0x0D4, 0x0F4, 0x114, 0x134, 0x154, 0x174: Transmit High-Speed Serial Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[23]	X
Bit 6	R	TCELL[22]	X
Bit 5	R	TCELL[21]	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[23:0]:

The TCELL[23:0] bits indicate the number of cells inserted into the transmission stream during the last accumulation interval. Stuff cells inserted into the transmission stream for rate decoupling are not counted.

A write to any one of the Transmit Cell Counter registers for a particular serial link or a write to the Load Performance Meters (0x000) register loads the registers with the current counter value and resets the internal 24 bit counter. The counter should be polled at least every 30 seconds to avoid saturating. The contents of these registers become valid within 300 ns after a transfer is triggered by a write to any of the link-associated Transmit Cell Count Registers or to the Load Performance Meters (0x000) register, and remain valid until another transfer is triggered.

The count saturates at all ones.

Registers 0x095, 0x0B5, 0x0D5, 0x0F5, 0x115, 0x135, 0x155, 0x175: Serial Link Maintenance

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	RDIDIS	0
Bit 3	R/W	TXDIS	0
Bit 2	R/W	MLB	0
Bit 1	R/W	DLB	0
Bit 0	R/W	ACTIVE	0

ACTIVE:

The value of this bit is encoded in the ACTIVE field of the cell structure transmitted on TXDn+/-.

DLB:

The Diagnostic Loopback enable bit allows TXDn+/- data to replace receive data. When DLB is logic one, the upstream circuitry for the serial link is timed off the internal transmit clock and the TXDn+/- data is multiplexed into the upstream datapath just after the clock recovery.

MLB:

The Metallic Loopback enable bit allows RXDn+/- data to be presented on TXD+/-. When LLB is logic one, the sliced receive data replaces the transmit data at the high-speed transmitter.

Note that the loopback can also be activated remotely through inband bit oriented codes.

TXDIS:

The Transmit Disable bit disables the high-speed outputs. If TXDIS is logic one, the associated TXDn+/- outputs do not drive valid logic levels, but instead float. TXDIS does not affect the differential output impedance; it is always within the range specified in the D.C. Characteristics section.

RDIDIS:

The RDI Disable bit disables the automatic transmission of a RDI codeword on TXDn+/-. If RDIDIS is logic zero, the declaration of LOS or LCD results in the RDI codeword being transmitted in the BOC bit position.

Note that RDI can be sent manually by writing all zeros to the Transmit Bit Oriented Code register.

Reserved

This bit should be logic 0 for correct operation.

Registers 0x097, 0x0B7, 0x0D7, 0x0F7, 0x117, 0x137, 0x157, 0x177: Transmit Bit Oriented Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

This register enables the generation of a bit oriented code and selects the 6-bit code to be transmitted in the BOC bit position on TXDn+/-.

The contents of this register will be transmitted repeatedly in the BOC bit position of the TXDn+/- high-speed serial link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, provided a Remote Defect Indication (RDI) is not currently being transmitted. The default value represents an idle code.

Registers 0x098, 0x0B8, 0x0D8, 0x0F8, 0x118, 0x138, 0x158, 0x178: Bit Oriented Code Receiver Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

This register selects the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status of the BOC received on RXDn+/-.

IDLE:

The IDLE bit enables the assertion of the INTB output when there is a transition from a validated BOC to idle code. When IDLE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the interrupt is enabled.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects an alternate validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion. Unless fast declaration is necessary, it is recommended that AVC be set to logic 0 to improve bit error tolerance.

BOCE:

The BOCE bit enables the assertion of the INTB output when a valid BOC is detected. When BOCE and the Master Interrupt Enable bit of the Master Configuration register are set to logic 1, the interrupt is enabled.

Register 0x099, 0x0B9, 0x0D9, 0x0F9, 0x119, 0x139, 0x159, 0x179: Receive Bit Oriented Code Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	X
Bit 6	R	BOCI	X
Bit 5	R	BOC[5]	X
Bit 4	R	BOC[4]	X
Bit 3	R	BOC[3]	X
Bit 2	R	BOC[2]	X
Bit 1	R	BOC[1]	X
Bit 0	R	BOC[0]	X

BOC[5:0]:

The BOC[5:0] bits indicate the current state value of the received bit-oriented code. The value is updated when the BOC has been a valid code 8 out of 10 or 4 out of 5 times, as selected by the AVC bit of the Bit Oriented Code Receiver Enable register. These bits are set to all ones (111111) if no valid code has been detected. An update is accompanied by a logic 1 in the BOCI bit.

IDLEI:

The IDLEI bit position indicates the detection of a transition from a valid BOC to idle or unvalidated state code value of 111111. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle or invalid code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

IDLEI will also be set when no code is currently validated. Note that failure to meet the 8 of 10 (or 4 of 5) persistency criteria, either due to LVDS bit errors or a change to a new code, does result in IDLEI being set to logic 1.

BOCI:

The BOCI bit position indicates the detection of a valid BOC. BOCI becomes logic 1 when BOC[5:0] changes from the transition or IDLE code value of 1111111. BOCI is cleared to logic 0 when the register is read.

BOCI will not be set at the transition to a validated IDLE code.

Registers 0x09C, 0x0BC, 0x0DC, 0x0FC, 0x11C, 0x13C, 0x15C, 0x17C: Upstream Link FIFO Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the upstream FIFO for a link. When FIFORST is set to logic 0, the FIFO operates normally. When FIFORST is set to logic 1, all the FIFOs are immediately emptied and ignore writes. While the FIFO is reset the flow control information sent to the far end (via the LVDS link) indicates “buffer full or unavailable”. The FIFO remains empty until logic 0 is written to FIFORST. To prevent unstable behavior during cell format configuration, FIFORST should be left asserted while changing the cell format or length.

Assertion of the FIFORST bit may result in a corrupted cell being transferred across the receive SCI-PHY/Any-PHY bus if there is currently active traffic on the associated high-speed serial link. Traffic for the other seven serial links not associated with the FIFORST bit will not be affected.

There is an upstream FIFO for each of the LVDS links. The eight FIFOs feed cells one at a time into the upstream Utopia or Any-PHY bus. Therefore, a reset on one of these FIFOs may cause the current cell being transferred over the bus to be corrupted. The specific conditions that will lead to corruption are as follows:

1. There must be at least one user cell in the upstream FIFO being reset. This cell will have arrived sometime previously over the LVDS.

2. The cell currently being transferred (or about to be transferred) over the upstream bus must be from the link being reset. Note that if several links are active there is no way for software to determine which link will be providing the next cell to the upstream bus.

3. The bus master need not have started the cell transfer (in response to the asserted RPA from the S/UNI-VORTEX) for cell corruption to occur. The S/UNI-VORTEX uses a partial look ahead buffer that cannot be reset by the upstream FIFO reset. Even if the bus master suspends cell transfers during the time when the upstream FIFO is reset, the next cell read from the S/UNI-VORTEX will be corrupted if conditions 1 and 2 existed during the FIFO reset. The simplest approach is to allow the bus master to continue normal operation during a FIFO reset. If required, the bus master can discard any cells received from that link after it is reset.

Reserved:

This bit should be logic 0 for correct operation.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-VORTEX. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[9]) is high.

The S/UNI-VORTEX supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port, except the TXDn+/- and RXDn+/- signals.

A limited RAM built-in-self-test (BIST) is available.

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x200: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-VORTEX test features. All bits, except PMCTST and PMCATST, are reset to zero by a reset of the S/UNI-VORTEX. This register is not affected by the RESET bit of the Master Reset and Identity Register (0x000).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-VORTEX . While the HIZIO bit is a logic one, all output pins of the S/UNI-VORTEX except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-VORTEX for board level testing. When IOTST is a logic one, all blocks are held in test mode.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-VORTEX to drive the data bus and holding the CSB pin low tri-states the data bus. The

DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-VORTEX for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-VORTEX microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the VORTEX for PMC's manufacturing tests. PMCATST is cleared when CSB is high and RSTB is low or when PMCATST is written as logic 0

Register 0x201: Master Test Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LINK_TM[2]	X
Bit 1	R/W	LINK_TM[1]	X
Bit 0	R/W	LINK_TM[0]	X

This register is used to globally control the S/UNI-VORTEX when in test mode. LINK_TM[2:0] are reset to logic 0 when CSB is logic 1. All register bits can also be reset by writing a logic 0 to the corresponding register bit.

LINK_TM[2:0]:

The LINK_TM[2:0] bits can be used to select which high-speed link of the S/UNI-VORTEX is under test when the PMCTST or IOTST register bit is set to logic 1. The LINK_TM[2:0] bits are not cleared by RSTB; therefore, they must be written to prior to testing.

11.1 RAM Built-In-Self-Test

The S/UNI-VORTEX contains built-in-self-test (BIST) circuitry for production testing of the device. A subset of the functionality is available for in situ screening against damage during handling and board manufacture.

The tests are controlled through the microprocessor port. The only other signals involved are the TCLK and RCLK inputs. The following procedure tests the numerous RAMs simultaneously:

1. Hold TCLK and RCLK low.

2. Set the RESET bit of the Master Reset and Identity register (0x000) to logic 1 to place the device in a known state.

3. Write the following register locations to select the test mode and initialize the BIST circuitry:

   Write 0x01 to 0x2nC, 0x3mC where n = 8, 9, A…F; m = 0,1,2…7

   Write 0x02 to 0x2nD, 0x3mD

   Write 0x55 to 0x2nE, 0x3mE

   These registers do not have default values and must be written.

4. Clear the RESET bit of the Master Reset and Identity register (0x000) to logic 0.

5. Set the IOTST bit of the Master Test register (0x200) to logic 1. This activates the BIST test mode.

6. Start toggling the TCLK and RCLK inputs at up to their specified maximum frequency. The two clocks must be frequency locked.

7. After exactly 16384 clock cycles read the following registers and compare against the expected data. Any discrepancies represent a test failure. Letting the test run indefinitely simply causes the test sequences to be repeated.

A[9:0]	Expected D[7:0]	
0x007	xxx0xx11	(Ensures TCLK and RCLK have toggled.)
0x2nE, 0x3mE	xxxx001x	

8. Repeat steps 1 through 7, but with the step 3 writes replaced with:

   Write 0x03 to 0x2nC, 0x3mC where n = 8, 9, A…F; m = 0,1,2...7

   Write 0x02 to 0x2nD, 0x3mD

   Write 0x55 to 0x2nE, 0x3mE

   This tests the second port on the RAMs.

11.2 JTAG Test Port

The S/UNI-VORTEX JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 0H

Part Number - 7351H

Manufacturer's identification code - 0CDH

Device identification - 173510CDH

Boundary Scan Register

Length - 98 bits

Table 4: Boundary Scan Register

Pin/Enable	Register Bit	Cell Type	Pin/Enable	Register Bit	Cell Type
RX8KOEB[6]	0	ENABLE	TDAT[4]	49	IN_CELL
RX8K	1	OUT_CELL	TDAT[3]	50	IN_CELL
VADR[4]	2	IN_CELL	TDAT[2]	51	IN_CELL
VADR[3]	3	IN_CELL	TDAT[1]	52	IN_CELL
VADR[2]	4	IN_CELL	TDAT[0]	53	IN_CELL
VADR[1]	5	IN_CELL	TCLK	54	IN_CELL
VADR[0]	6	IN_CELL	TPRTY	55	IN_CELL
RANYPHY	7	IN_CELL	TSX	56	IN_CELL
RADR[4]	8	IN_CELL	TPAOEB[4]	57	ENABLE
RADR[3]	9	IN_CELL	TPA	58	OUT_CELL
RADR[2]	10	IN_CELL	TENB	59	IN_CELL
RADR[1]	11	IN_CELL	TADR[11]	60	IN_CELL
RADR[0]	12	IN_CELL	TADR[10]	61	IN_CELL
RSX	13	OUT_CELL	TADR[9]	62	IN_CELL
RSOP	14	OUT_CELL	TADR[8]	63	IN_CELL
RENB	15	IN_CELL	TADR[7]	64	IN_CELL
RCLK	16	IN_CELL	TADR[6]	65	IN_CELL
RPAOEB[3]	17	ENABLE	TADR[5]	66	IN_CELL
RPA	18	OUT_CELL	TADR[4]	67	IN_CELL
RPRTY	19	OUT_CELL	TADR[3]	68	IN_CELL
RDAT[15]	20	OUT_CELL	TADR[2]	69	IN_CELL
RDAT[14]	21	OUT_CELL	TADR[1]	70	IN_CELL
RDAT[13]	22	OUT_CELL	TADR[0]	71	IN_CELL
RDAT[12]	23	OUT_CELL	A[0]	72	IN_CELL
RDAT[11]	24	OUT_CELL	A[1]	73	IN_CELL
RDAT[10]	25	OUT_CELL	A[2]	74	IN_CELL
RDAT[9]	26	OUT_CELL	A[3]	75	IN_CELL
RDAT[8]	27	OUT_CELL	A[4]	76	IN_CELL
RDAT[7]	28	OUT_CELL	A[5]	77	IN_CELL
RDAT[6]	29	OUT_CELL	A[6]	78	IN_CELL
RDAT[5]	30	OUT_CELL	A[7]	79	IN_CELL
RDAT[4]	31	OUT_CELL	A[8]	80	IN_CELL
RDAT[3]	32	OUT_CELL	A[9]	81	IN_CELL
RDAT[2]	33	OUT_CELL	CSB	82	IN_CELL
RDAT[1]	34	OUT_CELL	RDB	83	IN_CELL
RDATOEB[2]	35	ENABLE	ALE	84	IN_CELL
RDAT[0]	36	OUT_CELL	RSTB	85	IN_CELL
TX8K	37	IN_CELL	WRB	86	IN_CELL
TDAT[15]	38	IN_CELL	DOEB[1]	87	ENABLE
TDAT[14]	39	IN_CELL	D[0]	88	IO_CELL
TDAT[13]	40	IN_CELL	D[1]	89	IO_CELL
TDAT[12]	41	IN_CELL	D[2]	90	IO_CELL
TDAT[11]	42	IN_CELL	D[3]	91	IO_CELL
TDAT[10]	43	IN_CELL	D[4]	92	IO_CELL
TDAT[9]	44	IN_CELL	D[5]	93	IO_CELL
TDAT[8]	45	IN_CELL	D[6]	94	IO_CELL
TDAT[7]	46	IN_CELL	D[7]	95	IO_CELL
TDAT[6]	47	IN_CELL	INTB[5]	96	OUT_CELL
TDAT[5]	48	IN_CELL	REFCLK	97	IN_CELL

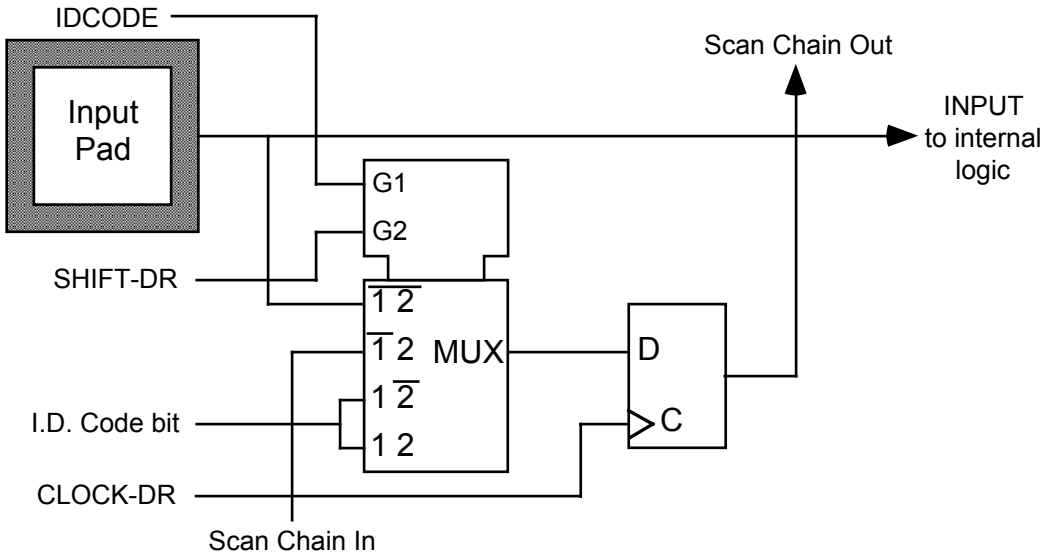
NOTES:

1. DOEB is the active low output enable for D[7:0].
2. RDATOEB is the active low output enable for RSOP, RSX, RDAT[15:0], and RPRTY.
3. RPAOEB is the active low output enable for RPA.
4. TPAOEB is the active low output enable for TPA.
5. When set high, INTB will be set to high impedance.
6. RX8KOEB is the active low output enable for RX8K.
7. RX8KOEB is the first bit of the boundary scan chain scanned in and out. It is closest to TDO.

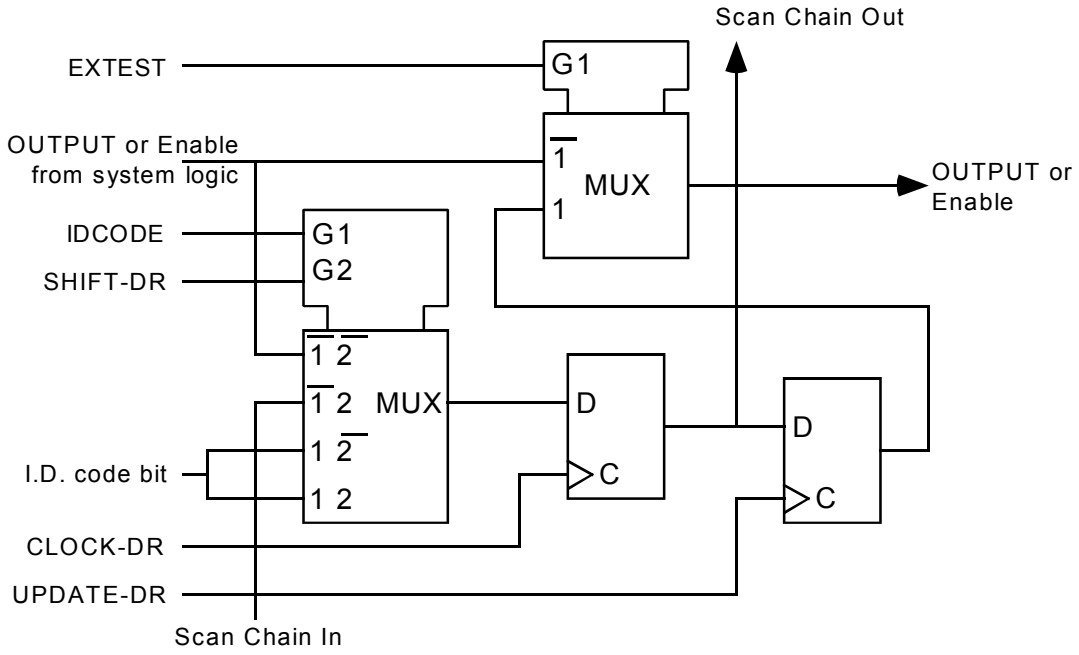
11.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

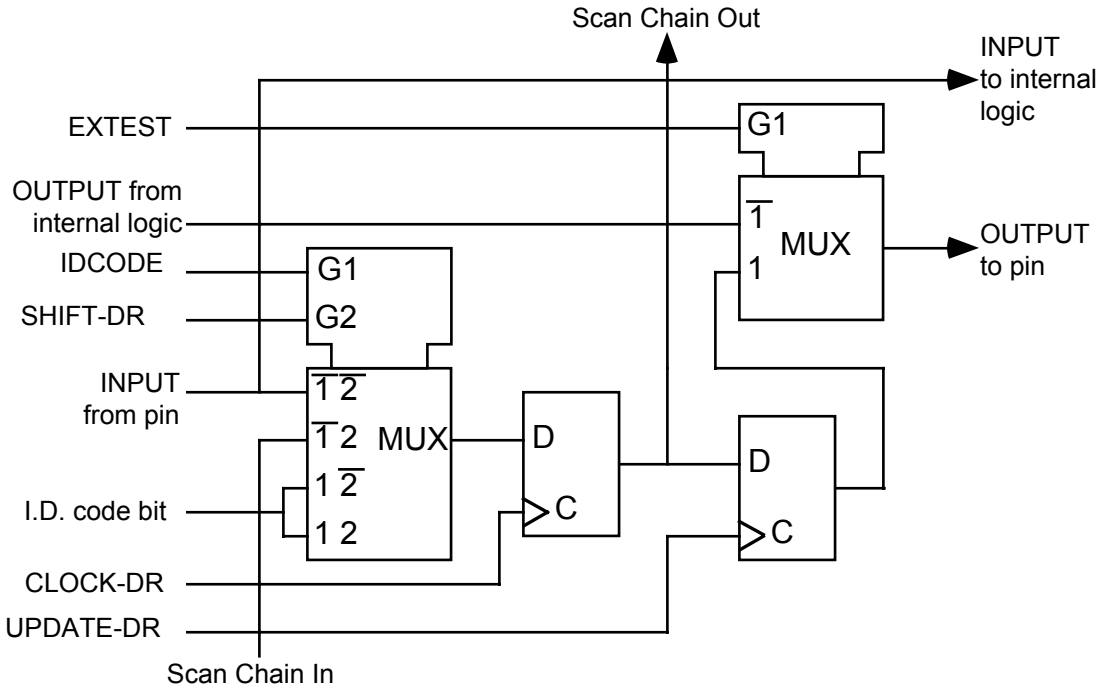
Input Observation Cell (IN_CELL)



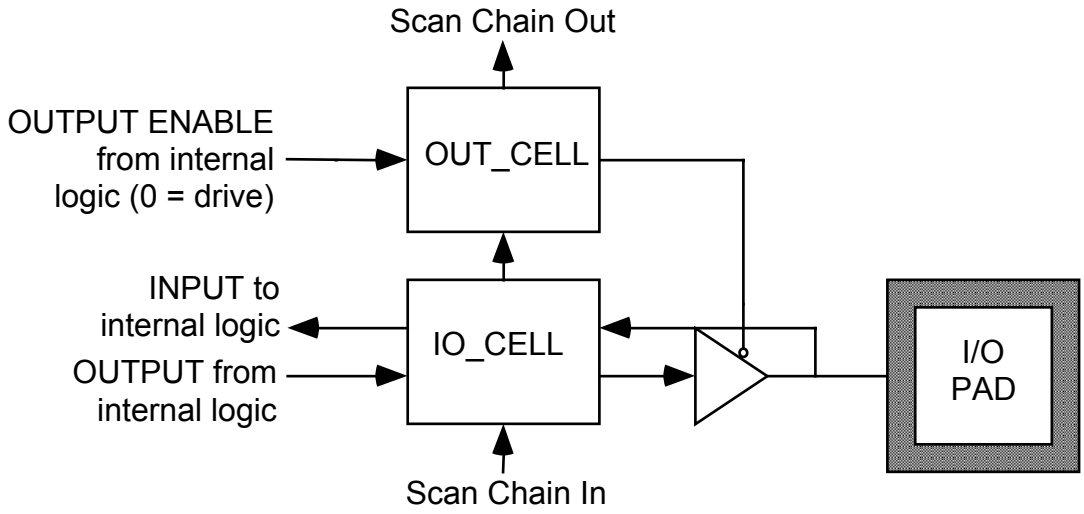
Output Cell (OUT_CELL)



Bidirectional Cell (IO_CELL)



Layout of Output Enable and Bidirectional Cells



12 OPERATION

This section complements Section 9 Functional Description, by describing in greater detail some of the programming and cross-functional issues that a designer using the S/UNI-VORTEX may want to consider.

12.1 Determining the Value for FREADY[5:0]

As discussed in Section 9.1.1, a downstream cell transfer should be initiated only after polling the appropriate downstream channel and ensuring that the buffer is empty, as indicated by that channel's TPA (Transmit Packet Available) output being asserted. The cell buffer status for each downstream channel (i.e. the status that will be driven onto the TPA output when the channel is polled) is deasserted when the first byte of a cell is written into the buffer. It is re-asserted only after the number of bytes programmed into the FREADY[5:0] field of the associated Downstream Logical Channel FIFO Ready Level register have been serialized onto a high-speed link. Determining whether or not it is necessary for you to adjust the default value of FREADY[5:0] is discussed in this section.

Each S/UNI-VORTEX has a total of 264 downstream cell buffers. There are 33 buffers per LVDS link (32 PHYs plus the microprocessor port), and 8 links in total. Each link is independent of, but identical to the others, so we need only describe how a single link works for you to understand how all downstream links function.

At the end of each cell transfer on the LVDS link the downstream scheduler polls (round-robin) its 33 buffers looking for the next buffer with a whole cell to send (the scheduler ignores buffers that are in the process of having a cell written to them). If there is no cell to send the scheduler immediately injects a stuff cell on the link. Once the link starts sending out the cell from a buffer, the entire cell will be sent before the scheduler begins its next scheduling cycle. Since a buffer cannot have more than one cell stored in it at a time, no single downstream channel can ever operate at a bandwidth greater than ½ the bandwidth of the LVDS link. Even if there are no other channels active, the scheduler will inject a stuff cell before the next cell from the same channel is available.

So what does this mean to the system designer? The maximum **per channel** bandwidth (i.e. ½ the LVDS line rate) will only be sustained if the bus master always writes the next cell into the downstream buffer within the time it takes to transmit a single cell over the LVDS link. Since the system bus is normally running much faster than the LVDS link this is not a problem in most designs. However, there are two scenarios in which the designer may be concerned about the time delay between TPA asserted and the last byte of the cell being written into the buffer:

1. There is considerable latency between the bus master seeing the TPA asserted and when it initiates the cell transfer to the S/UNI-VORTEX. For example the bus master (typically an ATM switching device) may have to perform a lookup, fetch the cell out of external memory, place the cell into an output buffer in the switching device, etc..

2. The system bus is running at the same rate (or only slightly faster) than the LVDS link, and hence it takes a relatively long time to write the cell into the buffer.

To assist the designer in these “tight timing” scenarios the S/UNI-VORTEX allows the value of FREADY[5:0] to be adjusted. To understand how this helps, let us step through the sequence of events that determine when a particular downstream buffer’s TPA (Transmit Packet Available) status is asserted and deasserted:

1. If the channel’s buffer is empty when the channel is polled, then TPA is asserted. At some point after seeing TPA asserted the bus master will start its write into the channel’s downstream buffer.

2. TPA status is deasserted when the first write into the buffer occurs. With the default extended length Any-PHY cells (PHY address in Word 0), the cell can be directed into the buffer immediately after Word 0 is available. Hence TPA is deasserted starting with Word 1 of the cell transfer. However, if the shorter cell length option is enabled and the H5/UDF field contains the PHY address (i.e. INADDUDF = 1 in the Downstream Cell Interface Configuration register) then TPA is deasserted after nine cycles after the last word of the cell is written. *This must be taken into account by the bus master device when establishing the polling algorithm to be used when INADDUDF=1*.

3. At some point after the entire cell has been written into the buffer, the downstream LVDS link scheduler will put this channel at the head of the queue and start to serialize and send the buffer contents downstream on the LVDS link. As mentioned previously, the entire cell must be present in the buffer before it is eligible for scheduling onto the LVDS link. The cell will be read out of the buffer at the LVDS line rate, not the line rate of the far-end PHY. The far-end S/UNI-DUPLEX provides a shallow rate decoupling buffer for each PHY, thereby allowing the LVDS link to run full speed for even the slowest PHYs.

4. The TPA status for that buffer is reasserted once the number of bytes defined in the link’s FIFO Ready Level (FREADY[5:0]) field have been serialized and sent down the link. If the FREADY[5:0] is set to a value greater than or equal to the cell length then FREADY has no real effect – that channel’s TPA status will remain deasserted until the entire cell has

been sent out on the LVDS link. If FREADY is set to a value less than the cell length then TPA will be asserted in advance of the buffer being completely empty.

5. The bus master can use this advanced TPA signal to shorten the time until the next cell is fully written into the buffer. The bus master can initiate the write of the next cell anytime after TPA is asserted. However, under no circumstances should the bus master complete the write of the full cell before the current cell is serialized and sent out on the LVDS link. Doing so will result in buffer overflow and data corruption.

6. Starting the write of the next cell while there is still a few bytes remaining from the previous cell does not impact how the FREADY value is used. The counter that tracks the number of bytes serialized from each cell will not be reset until the previous cell has left the buffer. In other words, when determining the value of the FIFO Ready Level you can ignore the fact that cell writes can be partially overlapped.

From the above discussion it is clear that reducing the value of FREADY[5:0] from its default value of 50 must be done carefully. A value of 50 or greater will never result in buffer overflow even under worse case conditions, which are:

- bus running at 800 Mbps,
- LVDS link running at 100 Mbps

Since word 0 is stripped from the cell before it is stored in the downstream buffer, the longest cell stored in the buffer is 56 bytes (this assumes the optional user prepend is enabled). In the worse case scenario the LVDS link is running 8 times slower than the system bus, which means in the time it takes to send the remaining 6 bytes out on the LVDS link there will at most be 48 bytes written into the buffer via the system bus. Since this is less than the cell length overflow cannot occur if FREADY[5:0] is left at its default value.

If your system design is such that your downstream PHYs are operating near the maximum supported rate (½ the LVDS line rate) and your system bus is less than the maximum you may want to advance the TPA signal by reducing FREADY[5:0]. The closer to the LVDS line rate the system bus is running, the lower FREADY[5:0] can be set. To determine the minimum value for FREADY[5:0] you must take into account the ratio between the LVDS link rate and the Any-PHY bus rate. You should also take into account the minimum latency between TPA asserted and the bus master starting the next write cycle. FREADY[5:0] should not be set lower than 9 for the reasons discussed previously.

12.2 Interaction Between Bus and LVDS Configurations

Since the far-end and near-end devices are configured independently it is important to take into account how the optional fields (the Any-PHY address field, the H5/UDF header bytes, and the user prepend word) are treated on an end-to-end basis. The following table summarizes the possible cell format options and summarizes the resultant impact on the cell contents at the receiving end.

Note the following:

- In general the S/UNI-VORTEX's LVDS links will be connected to S/UNI-DUPLEX devices. Hence the far end registers would normally reside in the S/UNI-DUPLEX device. However, there is nothing preventing a S/UNI-VORTEX from being connected to another S/UNI-VORTEX over the LVDS connection. Therefore, the following tables identify register appropriate for a S/UNI-VORTEX to S/UNI-VORTEX connection. The results are similar for a S/UNI-VORTEX to S/UNI-DUPLEX connection except the S/UNI-DUPLEX can function as a true Utopia L2 bus master or bus slave. Refer to the S/UNI-DUPLEX datasheet for details.

- The downstream bus (from bus master to S/UNI-VORTEX) can only operate in Any-PHY mode, meaning Any-PHY bus timing and addressing must be used. However, if the Downstream Cell Interface Configuration register (0x008) is set such that the PHY address is mapped into the H5/UDF field (INADDUDF = 1) then the minimum length cell can be 54 bytes long rather than Any-PHY's default 56 byte cell.

- The upstream bus can be configured as SCI-PHY (Input pin RANYPHY = 0) or Any-PHY (RANYPHY = 1). Setting the INADDUDF bit of register 0x00C to 1 when the bus is configured as Any-PHY has no effect. However, in SCI-PHY mode setting the INADDUDF bit of register 0x00C to 1 and the PREPEND bit to 0 ensures the upstream bus is Utopia L2 compliant.

- For control cells written or read via the microprocessor port, bytes 0&1 correspond to the microprocessor port's unique PHY address field. However since this field is fixed there is no useful information in these bytes. Bytes 10&11 are always undefined. Bytes 2&3 correspond to the user prepend bytes, and bytes 8&9 correspond to the H5&HDF bytes. Control cells transferred across the SCI-PHY/Any-PHY buses are formatted like all other cells.

- The PHY address field is transported across the LVDS in an extra word added to each user cell. Therefore it is not necessary that the H5/UDF field be sent over the LVDS link **even if the bus interfaces are configured to embed the PHY address in the H5/UDF fields**. This will slightly increase

the effective throughput of the LVDS, but it will impact control cells inserted and extracted via the microprocessor port as described in section 12.5.

- Some valid combinations are not shown in Table 5. Some of the missing combinations are readily derived from the table. Other combinations make little sense. For example, there is no use sending prepend information over the LVDS link if the receiving bus is not configured for prepends. Even if the near-end bus is configured for prepend it is more bandwidth efficient to turn off prepend on the LVDS link (the default setting) and hence discard the prepend at the near-end bus interface.

Table 5 From near-end downstream bus to far-end upstream bus

Near end downstream Reg 0x0008			Far-end upstream Reg 0x00C			LVDS: both ends must match e.g. Reg 0x080 and 0x90			Resultant Cell contents at far-end Bus or Microprocessor
H5UDF	INADDUDF	PREPEND	H5UDF	INADDUDF	PREPEND	USRHDR	PREPEND	CELLCRC	Note: USRHDR is a two bit value that defines the number of header bytes transferred over the LVDS link. 00 = 4 bytes 01 = 5 bytes (UDF not sent) 10 = 6 bytes (default) 11 = reserved Note: The LVDS transmitter adds 5 overhead bytes to every cell, which includes room for PHY address information. Thus the LVDS cell format is the same whether the PHY address arrives as a prepend or embedded in the H5/UDF field.
1	0	0	1	0	0	6	0	0	THIS IS THE DEFAULT CONFIGURATION • 59 byte cells (5 system, 6 header bytes, 48 data bytes) are transferred from a 56 byte bus to a 56 byte bus. • At the far-end bus, the address and H5 & UDF bytes are valid, and a cell prepend does not exist. • Control cell prepend bytes 2&3 are undefined, header bytes 8&9 are valid at far-end microprocessor.
1	0	0	1	0	0	5	0	0	• 58 byte cells (5 header bytes, UDF is removed) are transferred from a 56 byte bus to a 56 byte bus. • At the far-end bus, H5 is valid, UDF is undefined, and a cell prepend does not exist. • Control cell prepend bytes 2&3 and header byte 9 are undefined at Rx. Header byte 8 is defined.
1	0	0	1	0	0	4	0	0	• 57 byte cells (4 header bytes, H5&UDF are removed) are transferred from a 56 byte bus to a 56 byte bus. • At the far-end bus, the PHY address is valid, and H5 & UDF exist but are undefined. A cell prepend does not exist. • Control cell prepend bytes 2&3 and header bytes 8&9 are undefined at far-end microprocessor.
X	1	0	X	1	0	6	0	0	THIS CONFIGURATION NOT VALID IF RANYPHY = 1 • 59 byte cells (6 header bytes) are transferred from a 54 byte bus to a 54 byte bus.

Near end downstream Reg 0x0008			Far-end upstream Reg 0x00C			LVDS: both ends must match e.g. Reg 0x080 and 0x90			Resultant Cell contents at far-end Bus or Microprocessor
H5UDF	INADDUDF	PREPEND	H5UDF	INADDUDF	PREPEND	USRHDR	PREPEND	CELLCRC	Note: USRHDR is a two bit value that defines the number of header bytes transferred over the LVDS link. 00 = 4 bytes 01 = 5 bytes (UDF not sent) 10 = 6 bytes (default) 11 = reserved Note: The LVDS transmitter adds 5 overhead bytes to every cell, which includes room for PHY address information. Thus the LVDS cell format is the same whether the PHY address arrives as a prepend or embedded in the H5/UDF field.
									• At the far-end the H5 & UDF bytes contain the PHY address, and neither an address field nor a cell prepend exist. • Control cell prepend bytes 2&3 are undefined, header bytes 8&9 are valid at far-end microprocessor. If the control cell came from the downstream bus bytes 8&9 have no useful information (just the microprocessor port's PHY ID). If the control cell came from the microprocessor then bytes 8&9 will contain the value sent (i.e. they are not overwritten by the PHY ID)
X	1	0	X	1	0	5	0	0	THIS CONFIGURATION NOT VALID IF RANYPHY = 1 • 58 byte user cells (5 header bytes, UDF is removed) are transferred from a 54 byte bus to a 54 byte bus. • At the far-end bus the H5 & UDF bytes contain the PHY address, and neither an address field (Word 0) nor a prepend exist. • Control cell prepend bytes 2&3 and header byte 9 are undefined at the Rx end. If the cell came from the microprocessor port then header byte 8 is what was written. However, if the cell came from the bus then byte 8 is just half of the PHY ID value, and hence contains no useful information.
X	1	0	X	1	0	4	0	0	THIS CONFIGURATION NOT VALID IF RANYPHY = 1 • 57 byte user cells (4 header bytes, H5/UDF are removed) are transferred from a 54 byte bus to a 54 byte bus. • At the far-end bus the H5 & UDF bytes contain the PHY address, and neither an address field (Word 0) nor a prepend exist. • At the far end the control cell prepend bytes 2&3 and header bytes 8&9 are undefined regardless of source of the cell.
1	0	1	1	0	1	6	1	0	• 61 byte cells (5 system, 2 prepend, 6 header, 48 data bytes) are transferred from a 58 byte bus to a 58 byte bus. • Prepend, PHY address and H5 & UDF bytes are valid. • Control cell prepend bytes 2&3 and header bytes 8&9 are valid at far-end microprocessor.

Near end downstream Reg 0x0008			Far-end upstream Reg 0x00C			LVDS: both ends must match e.g. Reg 0x080 and 0x90			Resultant Cell contents at far-end Bus or Microprocessor
H5UDF	INADDUDF	PREPEND	H5UDF	INADDUDF	PREPEND	USRHDR	PREPEND	CELLCRC	Note: USRHDR is a two bit value that defines the number of header bytes transferred over the LVDS link. 00 = 4 bytes 01 = 5 bytes (UDF not sent) 10 = 6 bytes (default) 11 = reserved Note: The LVDS transmitter adds 5 overhead bytes to every cell, which includes room for PHY address information. Thus the LVDS cell format is the same whether the PHY address arrives as a prepend or embedded in the H5/UDF field.
1	0	1	1	0	1	4	1	0	• 59 byte cells (prepend + 4 header bytes, H5&UDF are removed) are transferred from a 58 byte bus to a 58 byte bus. • Prepend and PHY address valid, H5 & UDF exist but are undefined. • Control cell header bytes 8&9 are undefined at Rx. Prepend bytes 2&3 are defined.
1	0	1	X	1	0	6	0	0	THIS CONFIGURATION NOT VALID IF RANYPHY = 1 • 59 byte cells (5 system, 6 header bytes, 48 data bytes) are transferred from a 58 byte bus to a 54 byte bus. • At receiving bus the H5 & UDF bytes contain the PHY address. The near-end cell prepend is stripped off and not sent over the LVDS link. The H5/UDF field is sent to the far end, but over-written by the PHY address (the next example shows a similar, but more bandwidth efficient configuration). • Control cell header bytes 8&9 are valid at far-end microprocessor. Prepend bytes 2&3 are undefined.
1	0	1	X	1	0	6	0	0	THIS CONFIGURATION NOT VALID IF RANYPHY = 1 • 57 byte cells (4 header bytes) are transferred from a 58 byte bus to a 54 byte bus. • At receiving bus the H5 & UDF bytes contain the PHY address. The near-end cell prepend and H5/UDF is stripped off and not sent over the LVDS link. • Control cell prepend bytes 2&3 and header bytes 8&9 are undefined at far-end microprocessor.
X	1	0	1	0	1	4	0	0	• 57 byte cells (4 header bytes) are transferred from a 54 byte bus to a 58 byte bus. • At far-end the prepend, PHY address, and H5/UDF fields are all present. Word 0 contains the PHY address, but the prepend and H5/UDF fields are undefined. • Control cell prepend bytes 2&3 and header bytes 8&9 are undefined at far-end microprocessor.
X	1	0	1	0	1	4	1	1	• 59 byte cells (5 system, 2 CRC, 4 header bytes) are transferred from a 54 byte bus to a 58 byte bus. • At far-end the prepend, PHY address, and H5/UDF fields are all present. Word 0 contains the PHY address, the

Near end downstream Reg 0x0008			Far-end upstream Reg 0x00C			LVDS: both ends must match e.g. Reg 0x080 and 0x90			Resultant Cell contents at far-end Bus or Microprocessor
H5UDF	INADDUDF	PREPEND	H5UDF	INADDUDF	PREPEND	USRHDR	PREPEND	CELLCRC	Note: USRHDR is a two bit value that defines the number of header bytes transferred over the LVDS link. 00 = 4 bytes 01 = 5 bytes (UDF not sent) 10 = 6 bytes (default) 11 = reserved Note: The LVDS transmitter adds 5 overhead bytes to every cell, which includes room for PHY address information. Thus the LVDS cell format is the same whether the PHY address arrives as a prepend or embedded in the H5/UDF field.
									first byte the prepend is undefined, the second byte contains the CRC8 from the previous cell. H5/UDF is undefined. • Control cell prepend byte 2 is carried as is, but prepend byte 3 is overwritten with the CRC8. Header bytes 8&9 are undefined.
X	1	0	X	1	0	4	1	1	THIS CONFIGURATION NOT VALID IF RANYPHY = 1 • 56 byte cells (5 system, 2 CRC, 4 header bytes) are transferred from a 54 byte bus to a 54 byte bus. • At far-end the H5/UDF fields contains the PHY address. There is no prepend. • Control cell prepend bytes 2 is carried as is. Prepend byte 3 is overwritten with the CRC8. Header bytes 8&9 are undefined.

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12.3 Minimum Programming

Besides the bus configuration described in the previous section, very little configuration is required to make the part function. As an absolute minimum the following registers must be written before any cell traffic is possible:

1. Logical Channel Base Address registers (0x08A, 0x0AA, 0x0CA, 0x0EA, 0x10A, 0x12A, 0x14A and 0x16A) and Logical Channel Address Range/Logical Channel Base Address MSB registers (0x08B, 0x0AB, 0x0CB, 0x0EB, 0x10B, 0x12B, 0x14B and 0x16B) - These registers map the eight LVDS links into the 4096 channel address space of the downstream Any-PHY bus. The address mapping must match the configuration of the bus master.

2. Control Channel Base Address register (0x005) and Control Channel Base Address MSB register (0x006) – These registers determine the location of the eight control channels within the address space of the

downstream Any-PHY bus. If control channel cells are not being inserted via the Any-PHY bus, care must be taken to set this register to an address not used by the bus master.

3. TPAEN bit of the Master Configuration register (0x001) – This bit must be a logic 1 before the TPA output will respond to polling.

Beyond the minimum, the following bits are commonly modified:

1. MINTE bit of the Master Configuration register (0x001) – This bit must be logic 1 to enable interrupt servicing. If MINTE is logic 0, the INTB output will be unconditionally high-impedance. Note that individual interrupt sources must enabled in addition to setting MINTE.

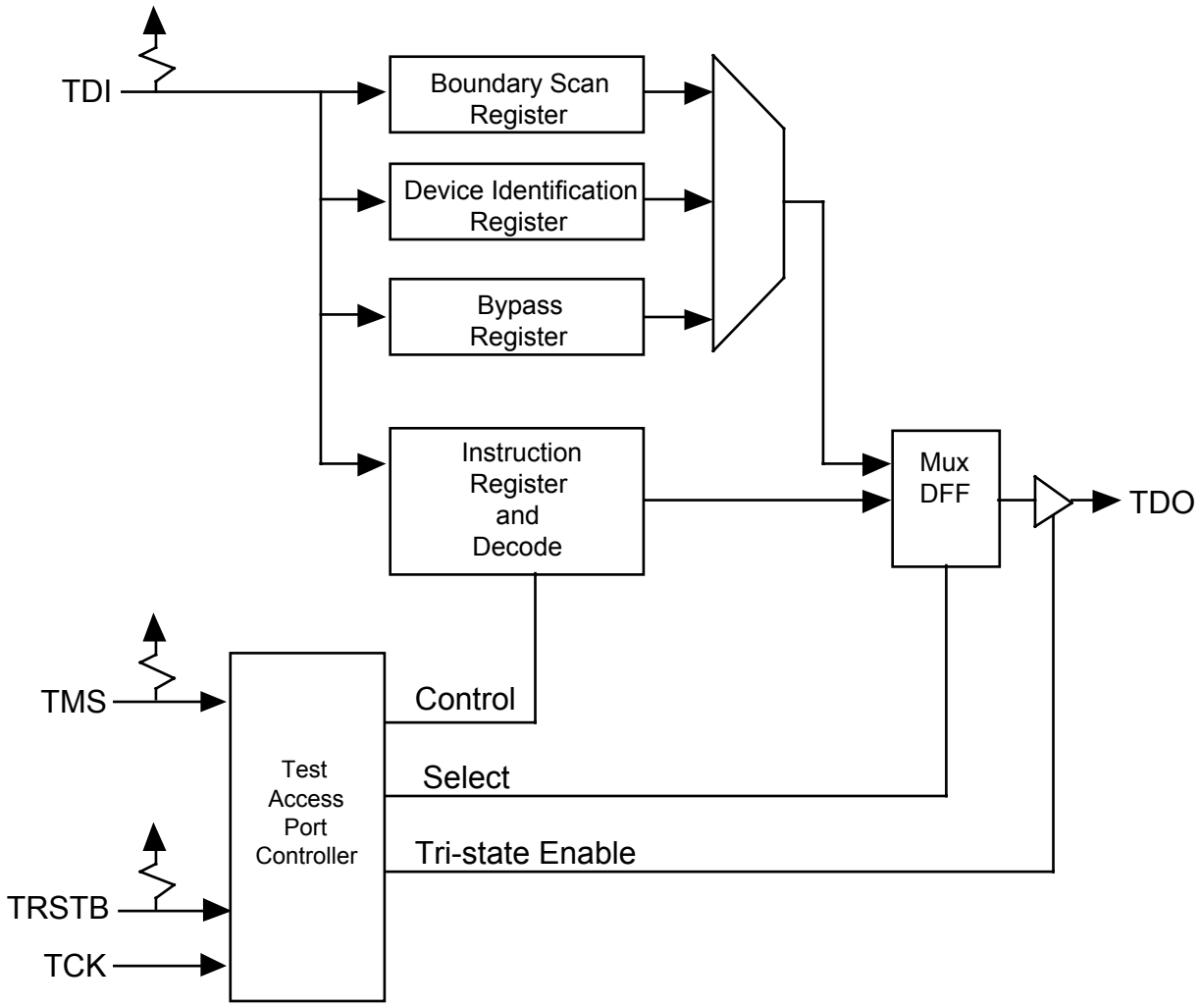
2. ROUTECC bit of the Master Configuration register (0x001) – This bit must be set to logic 1 if the control channel cells are to be read from the microprocessor port. If ROUTECC is logic 0, the control channel cells are routed to the SCI-PHY/Any-PHY upstream bus with a PHY ID of “111110”.

3. ACTIVE bit of the Serial Link Maintenance register (0x095, 0x0B5, 0x0D5, 0x0F5, 0x115, 0x135, 0x145, 0x165) – If this is the active as opposed to the spare card, this bit must be set to logic 1 to communicate this to the S/UNI-DUPLEX. Each bit is independent to allow load sharing configurations.

12.4 JTAG Support

The S/UNI-VORTEX supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standard. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Fig. 8.

Fig. 8 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

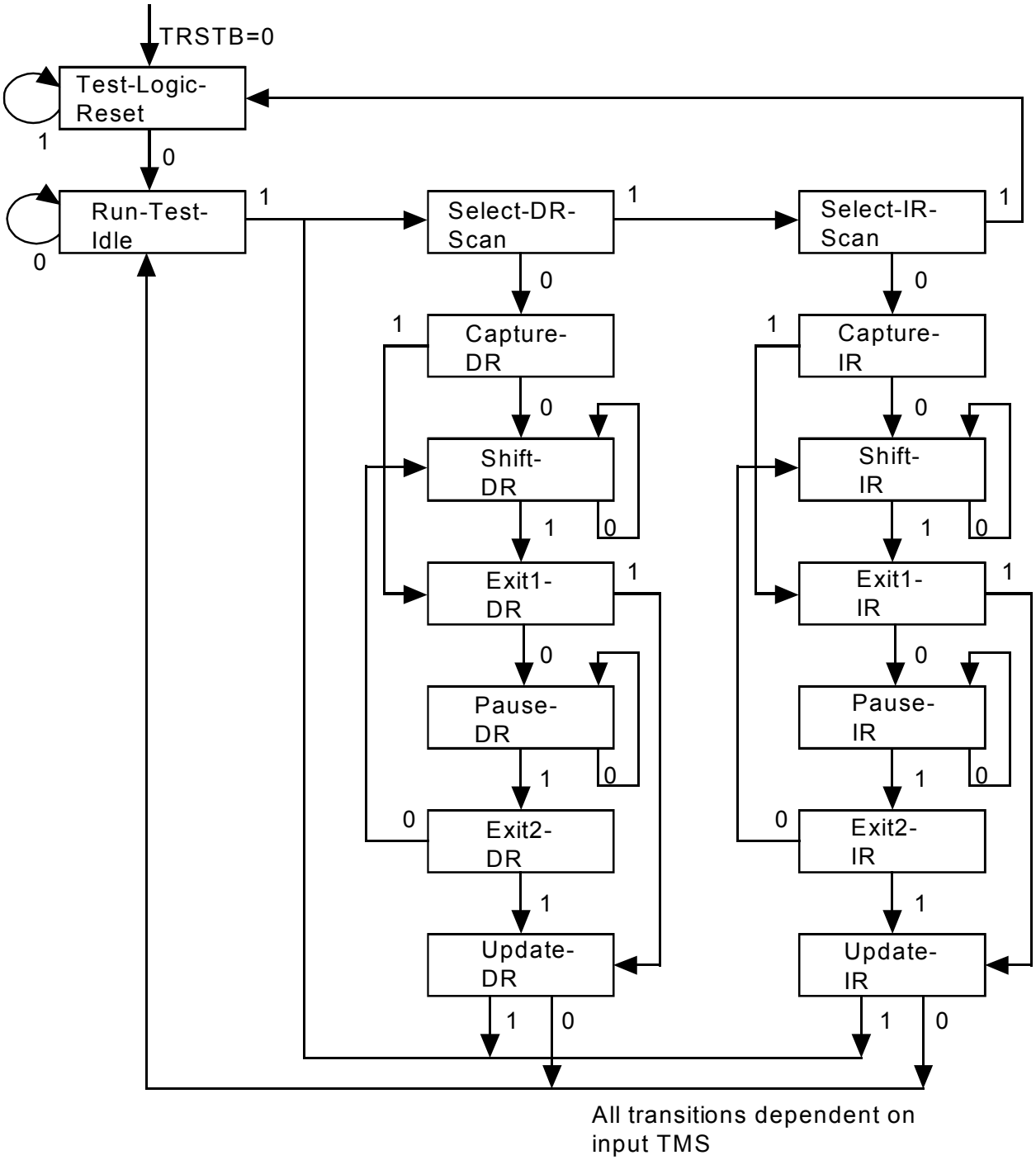
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is illustrated in Fig. 9.

Fig. 9 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

12.4.1 Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

12.5 Microprocessor Inband Communication

Control channel cells can be inserted and extracted through the parallel microprocessor interface. In both the upstream and downstream directions, each high-speed serial link has a dedicated queue for the control channel cells.

Although the interface is based on cell-at-a-time transfers, the goal is to provide efficient transmission and reception of packets of information. The microprocessor will have to perform the packet segmentation and reassembly function, but the S/UNI-VORTEX includes hardware support for CRC-32 generation and verification. It consists of two accumulator registers: the Insert CRC-32 Accumulator register for the downstream direction and the Extract CRC-32 Accumulator for control channel in the upstream direction.

To allow context change[1], each accumulator register can be preset, read and written by the microprocessor.

12.5.1 Inserting Cells Into Control Channels

Cells are inserted into control channels by manipulating the Microprocessor Insert FIFO Control and Microprocessor Insert FIFO Ready registers. The following steps are required to insert a cell:

1. Poll the INSRDY[7:0] bits in the Microprocessor Insert FIFO Ready register. Alternately, service the interrupts that result from setting the INSRDYE bit in the Microprocessor Cell Buffer Interrupt Control and Status register.

2. If a multi-cell CRC-32 calculation is required set the INSCRCPR of the Microprocessor Insert FIFO Control register to logic 0 to enable the CRC-32 process. The Insert CRC-32 Accumulation register can be preset by writing a logic 1 to INSCRCPR prior to enabling the CRC-32 calculation.

[1] A context change is, for example, when you are in the middle of sending a multi-cell packet on LVDS link A when a high priority event causes you to want to interrupt the packet transfer and send a packet out on link B. You would complete the current cell write to Link A, save the partial CRC, switch links, send the cells for link B, switch back to link A, reload the partial CRC and continue with the rest of link A's packet.

If the cell is not the first of the message, write the Insert CRC-32 Accumulator register with the value stored at the end of the previous cell for the same control channel. This step is not necessary if the last cell inserted belonged to the same control channel as the current cell.

Insertion of the CRC-32 field is done by setting the INSCRCEND bit of the Microprocessor Insert FIFO Control register to logic 1 prior to writing the last cell of the CPCS-PDU. The S/UNI-VORTEX will overwrite the data of the last four bytes of the cell payload written by the microprocessor with the ones complement of the content of the Insert CRC-32 Accumulator register.

3. Select the Insert FIFO by writing its identification number to the INSFSEL[2:0] field of the Insert FIFO Control register.

4. Write the cell contents to the Microprocessor Cell Data register. Cell data is entered in the format illustrated in Fig. 7.

5. If the cell is not the last of the message, read and store the contents of the Insert CRC-32 accumulator register. This step is not necessary if the next cell to be inserted belongs to the same control channel as the current cell.

The above sequence is repeated as needed to insert more cells. The assertion of a INSRDY bit of the Insert FIFO indicates that the associated FIFO is ready again to be written to. Setting INSRST of the Insert FIFO Control register to logic 1 prior to writing the last cell byte allows the overwriting of the cell data.

12.5.2 Reading Cell Data From a Control Channel

Reading cell data from a control channel is done by manipulating the Microprocessor Extract FIFO Control and Microprocessor Extract FIFO Ready registers. The following steps are required to read a cell from one of the Extract FIFOs.

1. Poll the EXTRDY[7:0] bits in the Microprocessor Extract FIFO Ready register. The EXTRDY[n] bit indicates the status of the FIFO receiving control channel cells from the RXDn+/- high speed link. Alternately, service the interrupts that result from setting the EXTRDYE bit in the Microprocessor Cell Buffer Interrupt Control and Status register.

2. Select the Extract FIFO corresponding to the desired high speed link by writing its identification number to the EXTFSEL bit of the Microprocessor Extract FIFO Control register.

3. Read the header of the cell to determine if it is the end of message and to which virtual channel it belongs.

4. If CRC-32 protection is required, set the EXTCRCPR of the Microprocessor Extract FIFO Control and Status register to logic 0 to enable the CRC-32 process. The Extract CRC-32 accumulation register can be preset for the first cell of a message by writing a logic 1 to EXTCRCPR prior to enable the CRC-32 calculation. If the cell is not the first one of a message and does not belong to the same control channel as the previous cell read, initialize the Extract CRC-32 Accumulator Registers to the value saved from the previous cell read for the control channel.

   CRC-32 field check is done by setting the EXTCRCCHK bit of the Microprocessor Extract FIFO Control register to logic 1. This causes the S/UNI-VORTEX to verify that the contents of the CRC-32 Accumulator register is equal to the expected CRC-32 remainder polynomial when the last byte of the cell is read from the Extract FIFO. The microprocessor can verify the CRC-32 field check result either through interrupt servicing or polling techniques.

   When interrupt servicing is used, the microprocessor enables the CRC-32 field check prior to reading the last cell of the CPCS-PDU by setting the EXTCRCCHK bit. An interrupt is raised if a CRC-32 error is found and the EXTCRCERRE bit is set.

   When polling is used, the EXTCRCERRE bit is kept to logic 0 and CRC-32 field check is always enabled. The microprocessor verifies the value of the EXTCRCERRI bit after reading the last cell of a CPCS-PDU.

5. Read the cell contents from the Microprocessor Cell Data register. Cell data is extracted in the format illustrated in Fig. 7.

6. If the cell is not the last of the message, read and store the contents of the Extract CRC-32 Accumulator register. This step is not necessary if the next cell extracted is known to belong to the same control channel as the current cell.

The above sequence is repeated as needed to read more cells. The assertion of the EXTRDY[7:0] bit of an Extract FIFO indicates that the FIFO is ready again to be read from. Setting EXTABRT of the Extract FIFO Control register to logic 1 allows the microprocessor to discard a cell without reading the remaining contents.

13 FUNCTIONAL TIMING

While the following diagrams present representative waveforms, they are not an attempt to unambiguously describe the interfaces. The Pin Description section is intended to present the detailed pin behavior and constraints on use.

Fig. 10 gives an example of the functional timing of the upstream interface when configured as a 16-bit SCI-PHY Level 2 compliant slave. The interface is programmed to include a user prepend (W1) as well the inband address (W0).

The interface responds to the polling of address “A” (which equals VADR[4:0]) by asserting RPA. As a result, the master selects the S/UNI-VORTEX by presenting “A” again during the last cycle RENB is high. Had not the device been selected, RSX, RSOP, RDAT[15:0] and RPRTY would have remained high-impedance.

Fig. 10 illustrates that a cell transfer may be paused by deasserting RENB. The device is reselected by presenting address “A” the last cycle RENB is high to resume the transfer.

Fig. 10 Upstream SCI-PHY Interface Timing

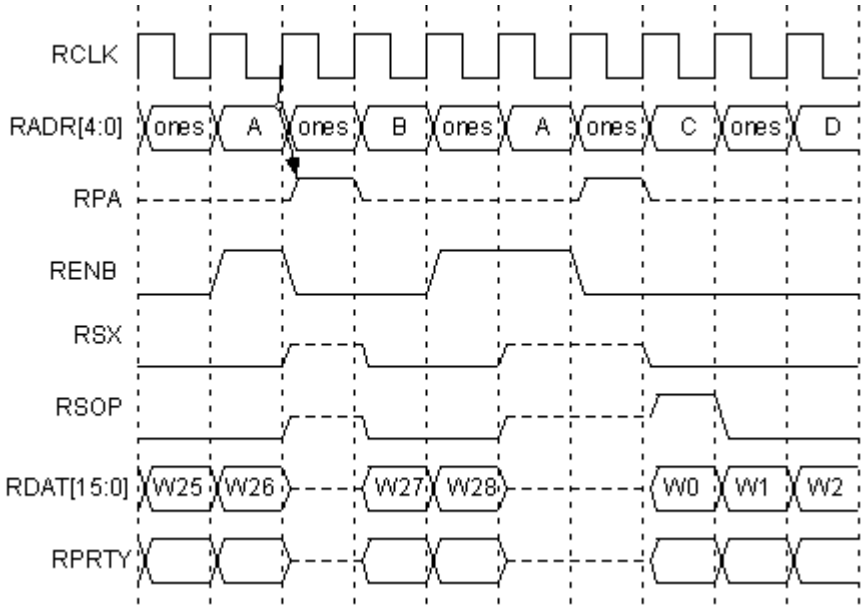


Fig. 11 gives an example of the functional timing of the upstream interface when configured as a 16-bit Any-PHY compliant slave. The user prepend (W1) is excluded in this example. Note that relative to SCI-PHY mode, all outputs have an additional cycle latency.

The interface responds to the polling of address “A” (which equals VADR[4:0]) by asserting RPA. As a result, the master selects the S/UNI-VORTEX by presenting “A” again during the last cycle RENB is high. Had not the device been selected, RSX, RSOP, RDAT[15:0] and RPRTY would have remained high-impedance.

Fig. 11 illustrates that a cell transfer may be paused by deasserting RENB. No explicit reselection is required to resume the transfer, only reassertion of RENB. Upon completion of the cell transfer, the interface autonomously deselects itself. As a result, it is permissible to hold RENB low beyond the end of the cell transfer as shown.

Fig. 11 Upstream Any-PHY Interface Timing

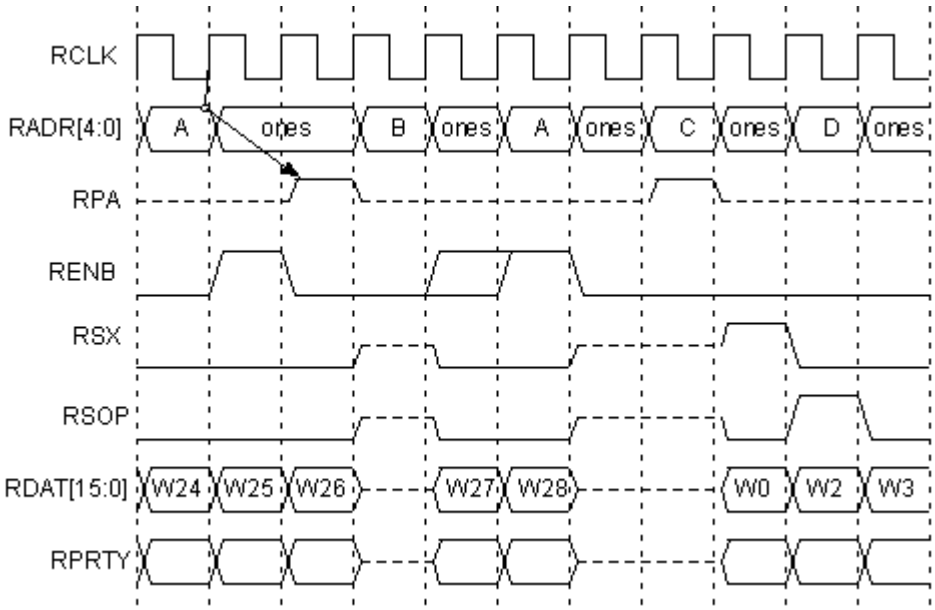


Fig. 12 is an example of the functional timing of the polling aspect of the downstream cell interface. Addresses “A”, “C” and “D” lie within the address space defined by the Control Channel Base Address, Logical Channel Base Address and Logical Channel Address Range registers; therefore, the device responds to those polls. The polls of logical channels “C” and “D” illustrate that polls in consecutive cycles are permitted.

Once a logic high is returned on TPA in response to a poll, a cell may be transferred as per Fig. 13.

Fig. 12 Downstream Any-PHY Interface Polling Timing

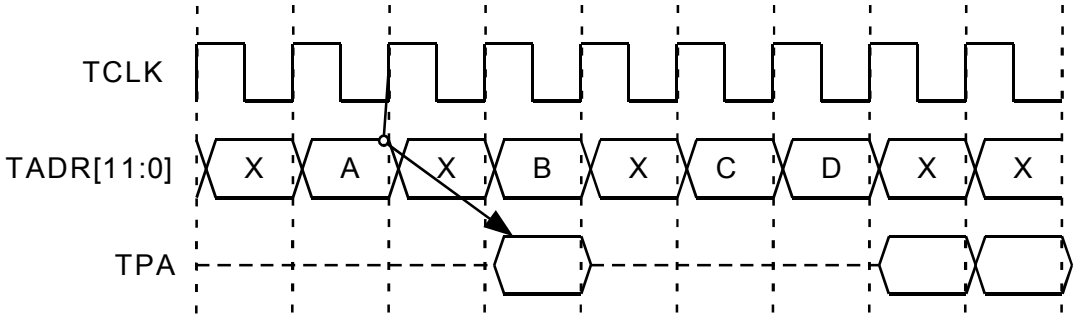
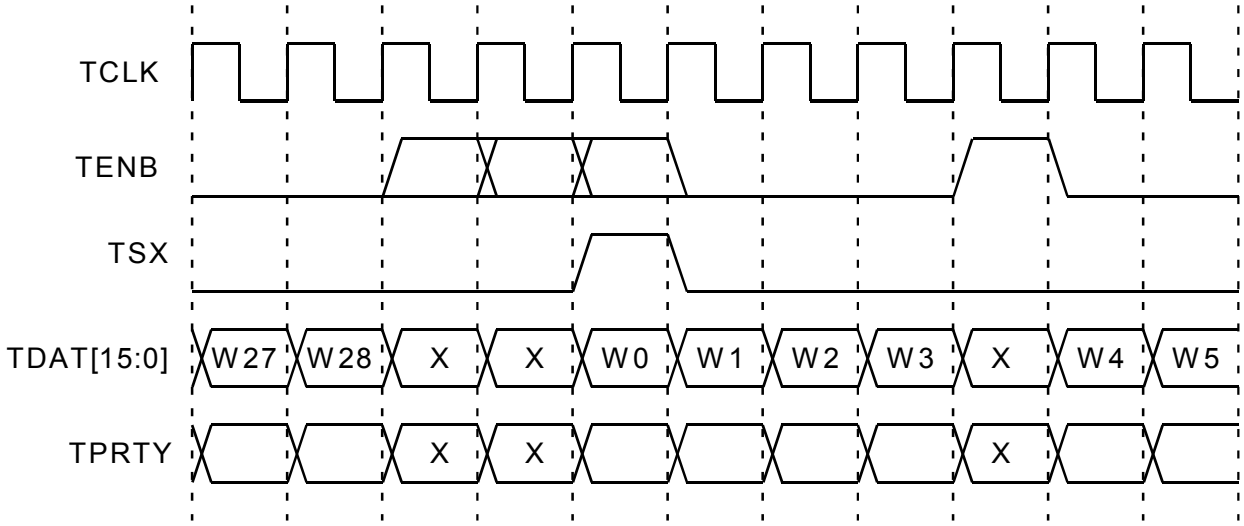


Fig. 13 is an example of the functional timing of the transfer aspect of the downstream cell interface. In this example, the user prepend is included in the data structure. A transfer is permitted when polling has established a buffer is available for the elected logical channel. The TSX input initiates the cell transfer as well as identifying the inband address (W0). The cell is accepted if the inband address is within the ranges defined by the Control Channel Base Address, Logical Channel Base Address and Logical Channel Address Range registers; otherwise, it is ignored.

It is permissible for TENB to be held low because a cell transfer is only initiated upon TSX assertion and automatically terminates upon the last word (W28) of the cells. TENB is ignored when TSX is high. The existence of TENB allows the master to pause a cell transfer as shown in Fig. 13.

Fig. 13 Downstream Any-PHY Interface Transfer Timing



14 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Case Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} =3.3 V ±10%

(Typical Conditions: T_C = 25°C, V_{DD} = 3.3 V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	3	3.3	3.6	Volts	
V_{BIAS}	5 V Tolerant Bias	VDD	5.0	5.5	Volts	
V_{IL}	Input Low Voltage (TTL Only)	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{BIAS} +0.5	Volts	Guaranteed Input HIGH Voltage for RANYPHY, A[8:0], RDB, WRB, CSB, ALE, D[7:0], TDI, TCK and TMS
V_{IH}	Input High Voltage (TTL Only)	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage for TENB, TADR[11:0], TDAT[15:0], TPRTY, TSX, TCLK, RENB, RADR[4:0], RCLK, VADR[4:0]
V_{OL}	Output or Bidirectional Low Voltage (TTL Only)		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -2 mA minimum. Note 3
V_{OH}	Output or Bidirectional High Voltage (TTL Only)	2.4	3.0		Volts	V_{DD} = min, I_{OH} = 2 mA minimum. Note 3
V_{T+}	Reset Input High Voltage	2.0		V_{BIAS} +0.5	Volts	TTL Schmitt for RSTB and TRSTB
V_{T-}	Reset Input Low Voltage			0.8	Volts	TTL Schmitt for RSTB and TRSTB

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	TTL Schmitt for RSTB and TRSTB
V_{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Input Differential Sensitivity			100	mV	
$\|V_{HYST}\|$	LVDS Input Differential Hysteresis	25			mV	
R_{IN}	LVDS Differential Input Impedance	10			kΩ	
V_{LOH}	LVDS Output voltage high		1375	1475	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	925	1025		mV	R_{LOAD}=100Ω ±1%
V_{ODM}	LVDS Output Differential Voltage	250	350	400	mV	R_{LOAD}=100Ω ±1% When the device is in reset, the differential voltage is approximately 80 mV. Once the device is out of reset, the voltage returns to the normal level.
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Single-Ended	70		130	Ω	V_{CM}=1.0V and 1.4V
ΔR_O	LVDS Output Impedance Mismatch between TXOP and TXON			10	%	V_{CM}=1.0V and 1.4V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$\Delta\|V_{ODM}\|$	Change in $\|V_{ODM}\|$ between "0" and "1"			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between "0" and "1"			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND. Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP1}	Operating Current Processing Cells			1000	mA	V_{DD} = 3.63 V, Outputs Unloaded, TXDn+/- and RXDn+/- 200 Mb/s TFCLK = RFCLK = 52 MHz

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

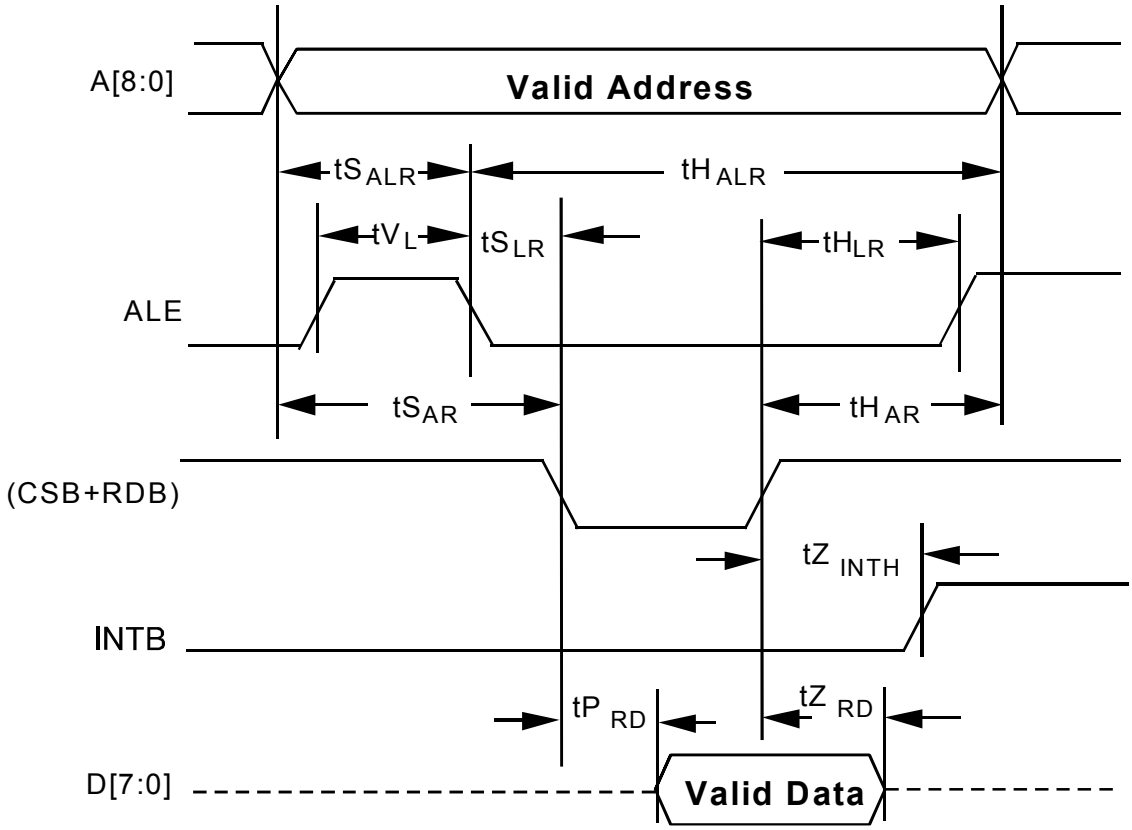
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%)

Microprocessor Interface Read Access (Fig. 14)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Fig. 14 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.

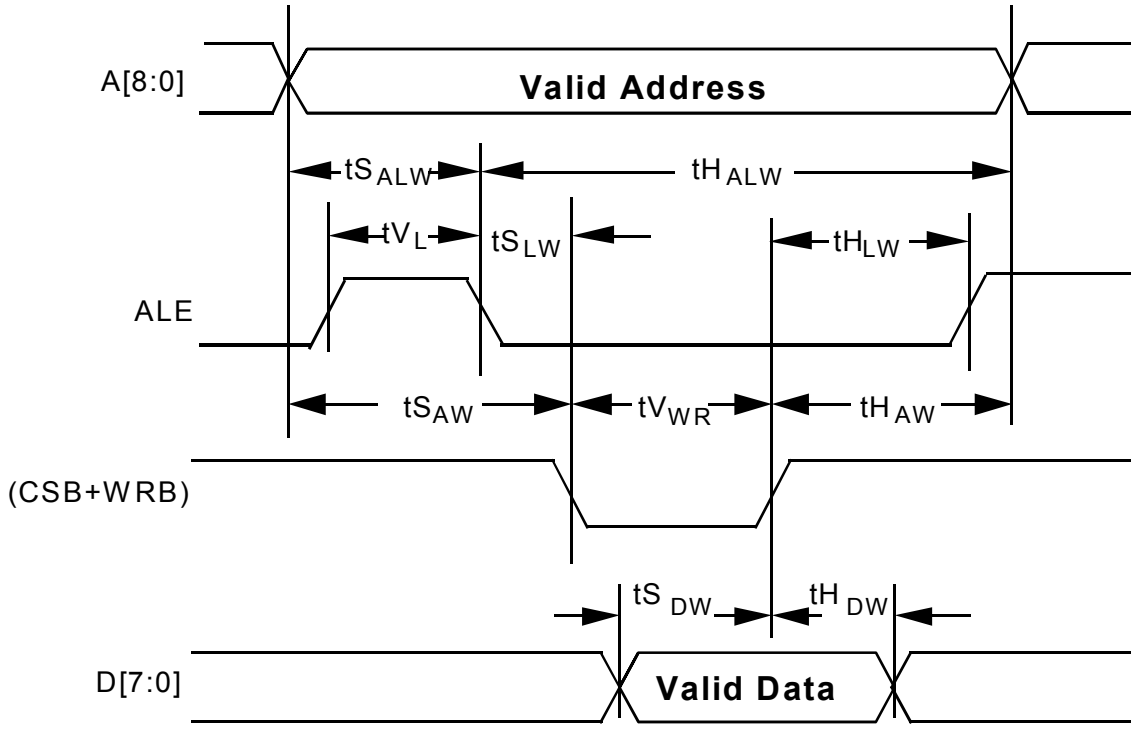
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Microprocessor Interface Write Access (Fig. 15)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 15 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2 In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

3 Parameter tH_{AW} is not applicable if address latching is used.

4 When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5 When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

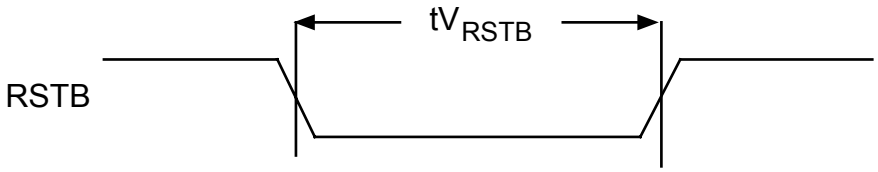
17 A.C. TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%)

RSTB Timing (Fig. 16)

Symbol	Parameter	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Fig. 16 RSTB Timing



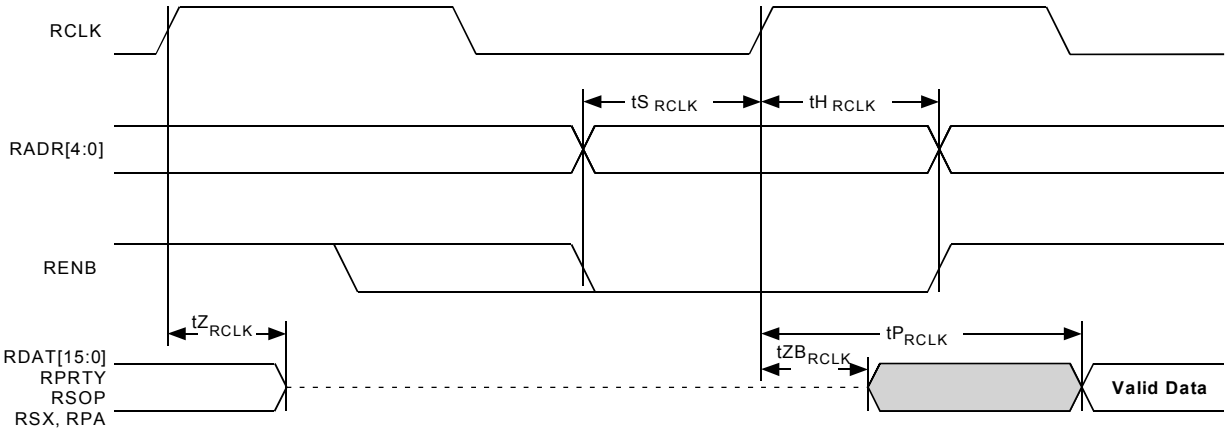
REFCLK Timing

Symbol	Parameter	Min	Max	Units
f_{REFCLK}	REFCLK Frequency	12.5	25	MHz
D_{REFCLK}	REFCLK Duty Cycle	20	80	%

Receive SCI-PHY Interface (Fig. 17)

Symbol	Description	Min	Max	Units
f_{RCLK}	RCLK Frequency	0	52	MHz
D_{RCLK}	RCLK Duty Cycle	40	60	%
tS_{RCLK}	RENB and RADR[4:0] Set-up time to RCLK	3		ns
tH_{RCLK}	RENB and RADR[4:0] Hold time to RCLK	0.5		ns
tP_{RCLK}	RCLK High to Output Valid	2	12	ns
tZ_{RCLK}	RCLK High to Output High-Impedance	2	12	ns
tZB_{RCLK}	RCLK High to Output Driven	0		ns

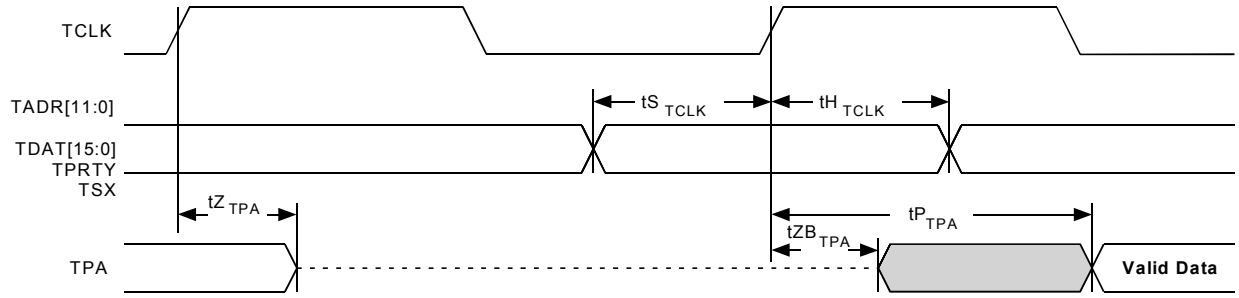
Fig. 17 Receive SCI-PHY/Any-PHY Interface Timing



Transmit Any-PHY Interface(Fig. 18)

Symbol	Description	Min	Max	Units
f_{TCLK}	TCLK Frequency	0	52	MHz
D_{TCLK}	TCLK Duty Cycle	40	60	%
tS_{TCLK}	TENB, TADR[11:0], TDAT[15:0], TPRTY and TSX Set-up time to TCLK	3		ns
tH_{TCLK}	TENB, TADR[11:0], TDAT[15:0], TPRTY and TSX Hold time to TCLK	0		ns
tP_{TPA}	TCLK High to TPA Valid	2	12	ns
tZ_{TPA}	TCLK High to TPA High-Impedance	2	12	ns
tZB_{TPA}	TCLK High to TPA Driven	0		ns

Fig. 18 Transmit SCI-PHY Interface Timing



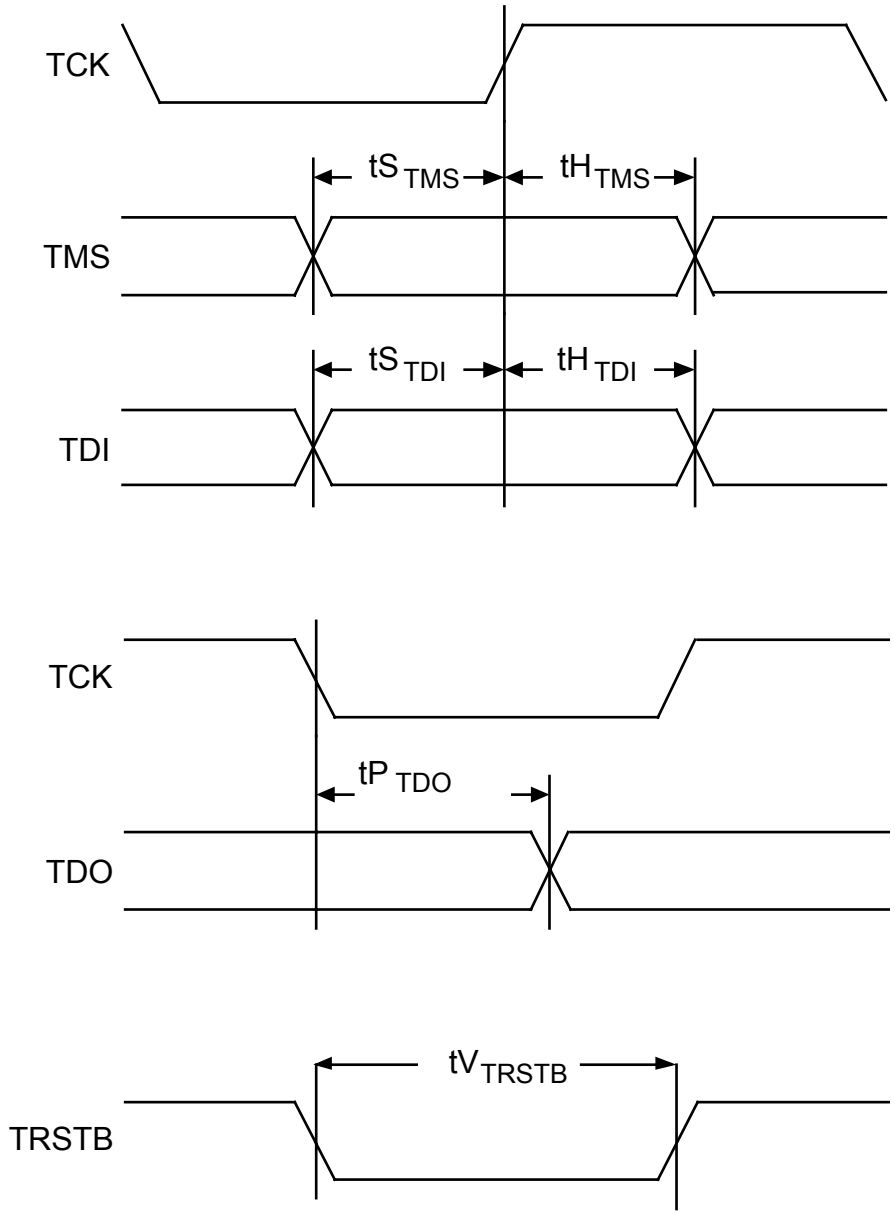
High-Speed Serial Interface

Symbol	Description	Min	Max	Units
	RXDn+/- Bit Rate	$8f_{REFCLK}$ -100ppm	$8f_{REFCLK}$ +100ppm	Mb/s
t_{FALL}	V_{ODM} fall time, 20%-80%	300	700	ps
t_{RISE}	V_{ODM} rise time, 20%-80%	300	700	ps
t_{SKEW}	Differential Skew		50	ps

JTAG Port Interface (Fig. 19)

Symbol	Description	Min	Max	Units
	TCK Frequency		4	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Fig. 19 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

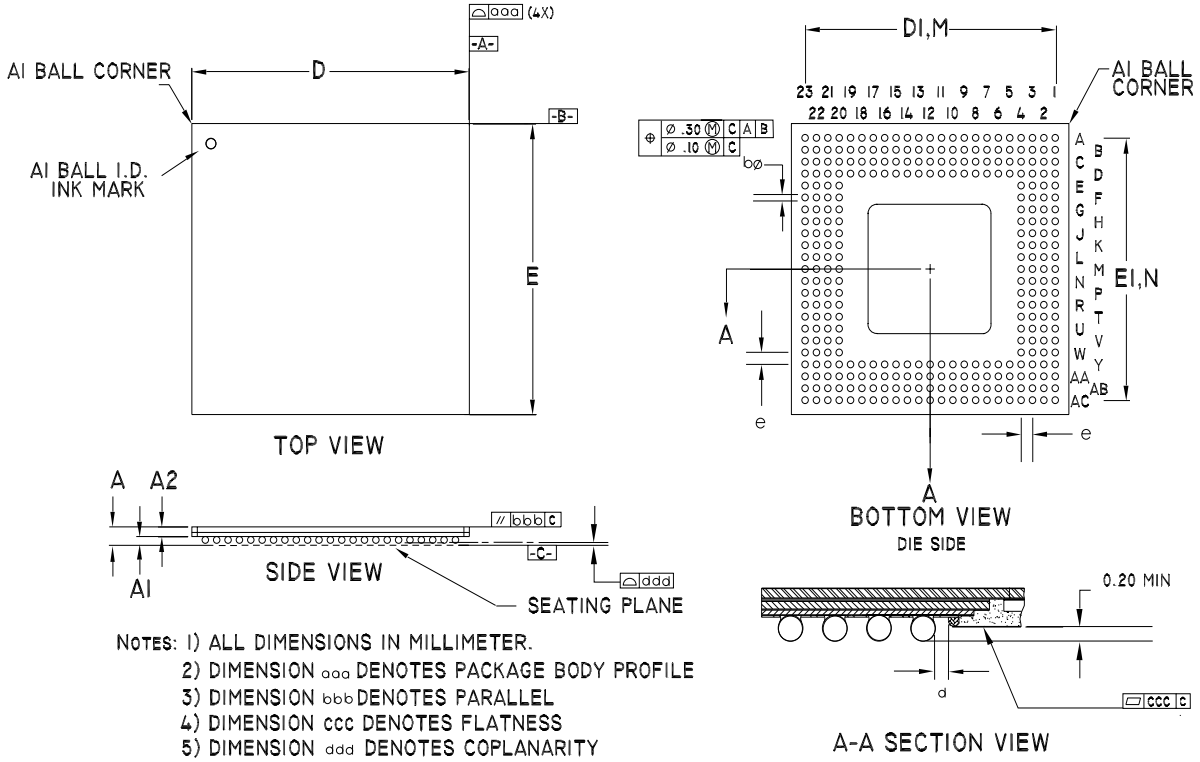
2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

18 ORDERING AND THERMAL INFORMATION

PART NO.	DESCRIPTION
PM7351-BI	304 Enhanced Ball Grid Array (SBGA)

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM7351-BI	-40°C to 85°C	15 °C/W	5 °C/W

19 MECHANICAL INFORMATION



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE
3) DIMENSION bbb DENOTES PARALLEL
4) DIMENSION ccc DENOTES FLATNESS
5) DIMENSION ddd DENOTES COPLANARITY

PACKAGE TYPE: 304 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 31 X 31 X 1.51 MM															
DIM.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	d
MIN.	1.30	0.50	0.80	30.90	27.84	30.90	27.84			0.60					0.50
NOM.	1.51	0.60	0.91	31.00	27.94	31.00	27.94	23x23	1.27	0.75					
MAX.	1.70	0.70	1.00	31.10	28.04	31.10	28.04			0.90	0.20	0.25	0.20	0.20	

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