AN-6006

FAN5068 Component calculation and simulation tools

Background / Overview

To simplify designs using the FAN5068 DDR/ACPI control IC, Fairchild provides:

- An Excel workbook to calculate recommended external component values
  and
- A continuous time behavioral model of the modulator that runs in PSPICE A/D v 9.1 or above. The model is small enough to run under Cadence's Orcad Lite Edition (includes Orcad Capture and PSPICE A/D), which can be ordered on CD or may be downloaded at:
  http://www.orcad.com/downloads/demo/default.asp

Information on the FAN5068, including the datasheet can be found on:
http://www.fairchildsemi.com/pf/FA/FAN5068.html

This package of design aids (including this document) is can be downloaded from:
http://www.fairchildsemi.com/collateral/AN-6006.zip.

To install, copy AN-6006.ZIP to an empty folder (e.g. "FAN5068Design"). Then unzip AN-6006.ZIP into that folder.

Recommended design procedure:

1. Use the spreadsheet (FAN5068 Design calculation aid.xls) to calculate the output filter using the "Output Filter" tab.
2. Use the "Main Sheet" tab of the spreadsheet to calculate the other component values once you have selected the output L and C.
3. Use the "Compensation" tab to design the compensation network.
4. Input the values you have selected into the PSPICE model. Generate a Bode plot by simulating with the "application circuit-ac sweep" simulation profile. Make sure to simulate over the corners of VIN and IOUT for your application.
5. Once you are satisfied with the small signal stability, you can view the transient response by simulating using the "application circuit-transient response" simulation profile. Be sure the follow the instructions at the bottom of the Application Circuit, Page 1 sheet for resetting RLOAD before simulating transient response.

Design Calculation Spreadsheet: FAN5068 Design calculation aid.xls

For instructions on the use of this spreadsheet, see the "Instructions" tab of the spreadsheet.

PSPICE Simulation Model

The simulation model is a sampled data continuous time model, which is adapted from Ray Ridley and Dennis Feucht's modeling work for current mode controllers [1,2,3]. It is set up to provide a bode plot where the red trace is Phase Margin (in degrees) and the green trace is gain (in dB). For stable response, we recommend at least 45° of phase margin when the gain crosses 0dB. The model also provides transient response using a pulsed current source (I1) as the load. The IC's error-amp behavioral model is based on Ray Kendall's Macromodelling article in EDN. [4]

To run the model start Capture (9.1 or higher), open **FAN5068.opj** (this is the "project" file for Capture). Double click on Page 1 Under .\fan5068.dsn\Application Circuit.

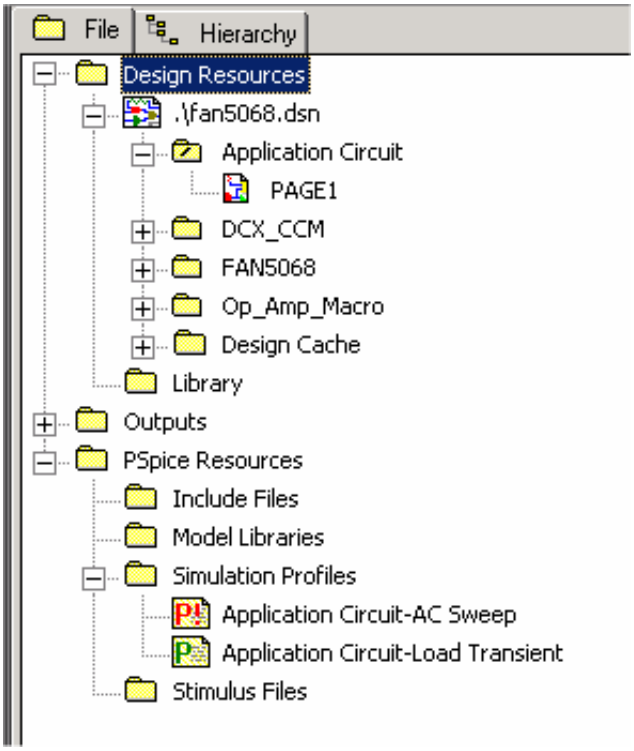

Figure 1. FAN5068.OPJ project

The parameters for this model are entered in the "Parameters" block on the lower left-hand corner of the schematic. As such, there should be no need to edit the schematic itself.

Double click on any parameter in that block to set the values in the schematic. Once the schematic is set up, F11 (function key) will display the Bode plot.

To choose between Bode plot (AC small signal) and Transient response, go to the project window and right click the appropriate model. If you are simulating for transient response, be sure to set up RLOAD. You will know if you forgot this step, as the inductor current [I(L1)] trace will be much higher (probably beyond the Y axis limit) than the pulse load current [I(I1)].

Alternately, from the schematic view, select the type of simulation profile from the drop-down box as shown below.

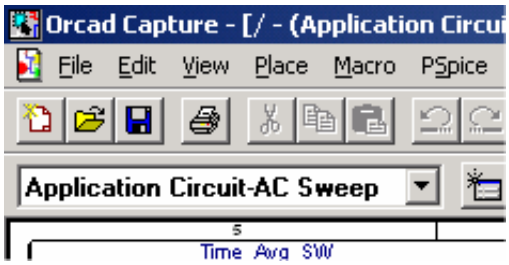

Figure 2. Simulation profile select drop-down

Troubleshooting the plot window

Some older versions of PSPICE may not automatically load the probe settings (which are contained in the *.prb files). These settings define the XY axis settings, trace colors, and which signals are displayed. If you run a simulation and the probe window has no trace, then add a trace, and input the expressions for the signals to plot:

Gain: DB(V(Out)/V(Sig)) **Phase**: P(V(Out)/V(Sig))

Copy and paste these expressions into the add trace window as shown below. The also schematic contains the expressions for the BODE plot in the lower right hand corner

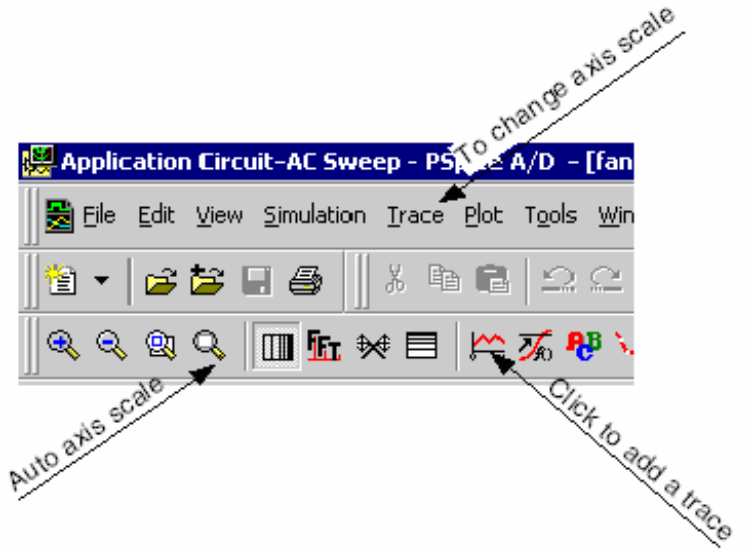

Figure 3. Tips for adjusting probe window settings and adding traces

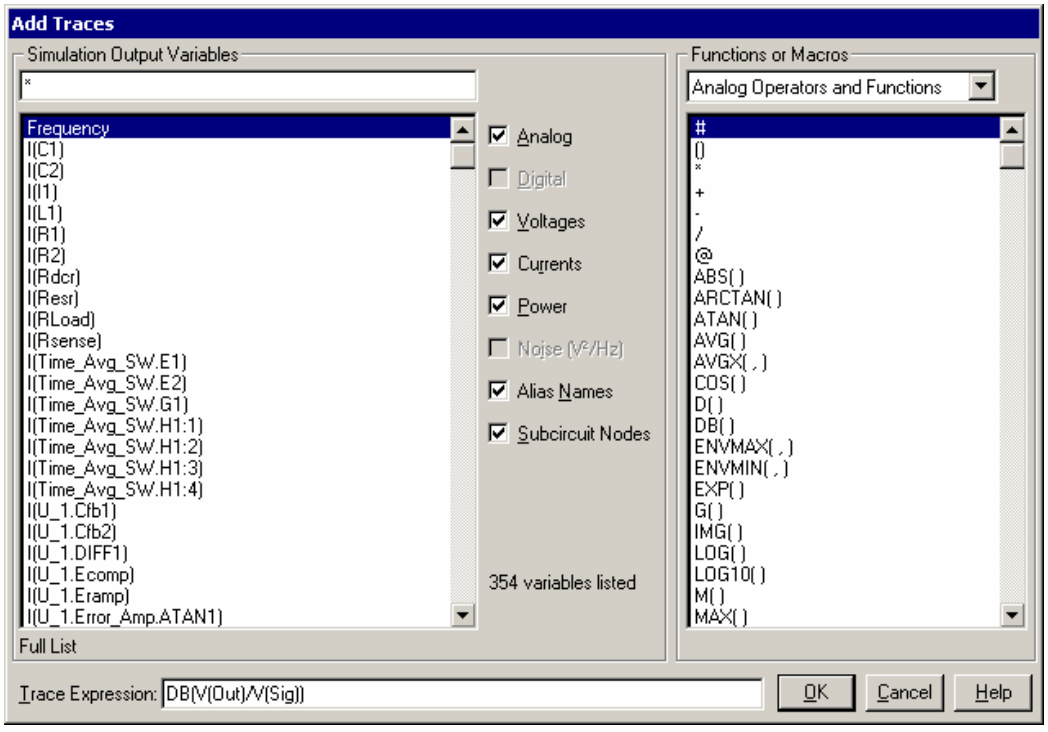

Figure 4. Adding the trace (Gain example)

References:

[1] Ray Ridley, *An Accurate and Practical Small-Signal Model for Current-Mode Control*, 1999, http://www.ridleyengineering.com/downloads/curr.pdf

[2] Dennis Feucht, *The Tymerski Switch Model*, http://www.chipcenter.com/eexpert/dfeucht/dfeucht036.html

[3] Dennis Feucht, *Basic Power Converter Configurations*, http://www.chipcenter.com/eexpert/dfeucht/dfeucht037.html

[4] Ray Kendall, *Modular macromodeling techniques for Spice simulators*, EDN, March 7, 2002 http://www.reed-electronics.com/ednmag/contents/images/198891.pdf