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MP3 Audio Decoder **PT8401**

Description

The PT8401 is a single chip MPEG audio decoder capable of decoding all layers compressed elementary streams, as specified in MPEG 1 and MPEG 2 ISO standards. With external A/D converter, it can also compress incoming signal by using ADPCM algorithm, therefore it can also playback ADPCM bitstream.

Features

- Supports all the sampling frequency of MPEG1 (32/44.1/48KHz), MPEG2(16/22.05/24KHz) and MPEG2.5
- Serial Bit Stream Input Interface
- I^2S/Normal Audio Data Output Format delivered via an Serial Bus
- Power Saving Mode Support
- Supports DAC Master Clock (256*fs / 384*fs for 16 / 24 bit DAC)
- Built-in Tone and Digital Equalizer Control
- Bass Booster Function
- 3D Sound Effect Function
- Pause Function
- Fast Forward Function
- Available in 44-pin Plastic LQFP Package

Applications

- Portable MP3 Player (Flash Memory Type)
- PDA with MP3 Player
- Cellular Phone with MP3 Player
- Hard Disk MP3 Player (IDE Interface)
- CD MP3 Player
- Digital Voice Recorder

Block Diagram

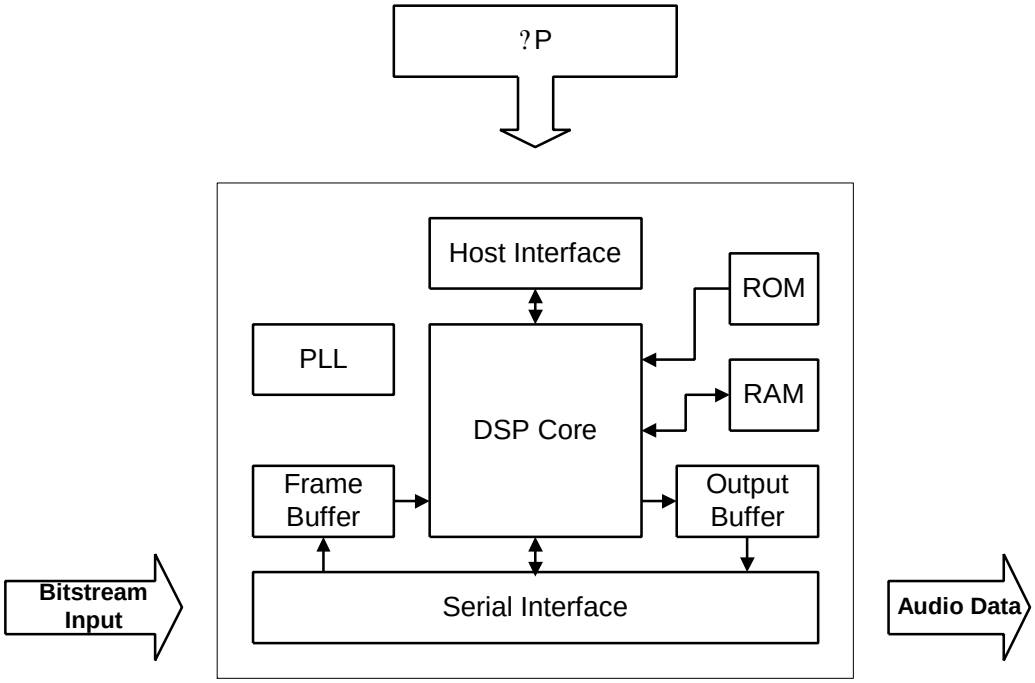


Figure 1: PT8401 Block Diagram

Typical Application Diagram

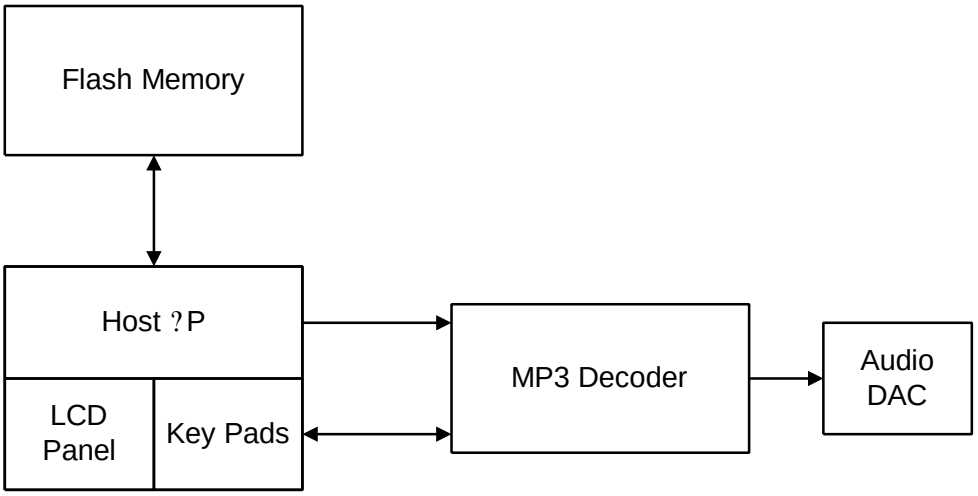


Figure 2: Typical Application Diagram

Pin Configuration

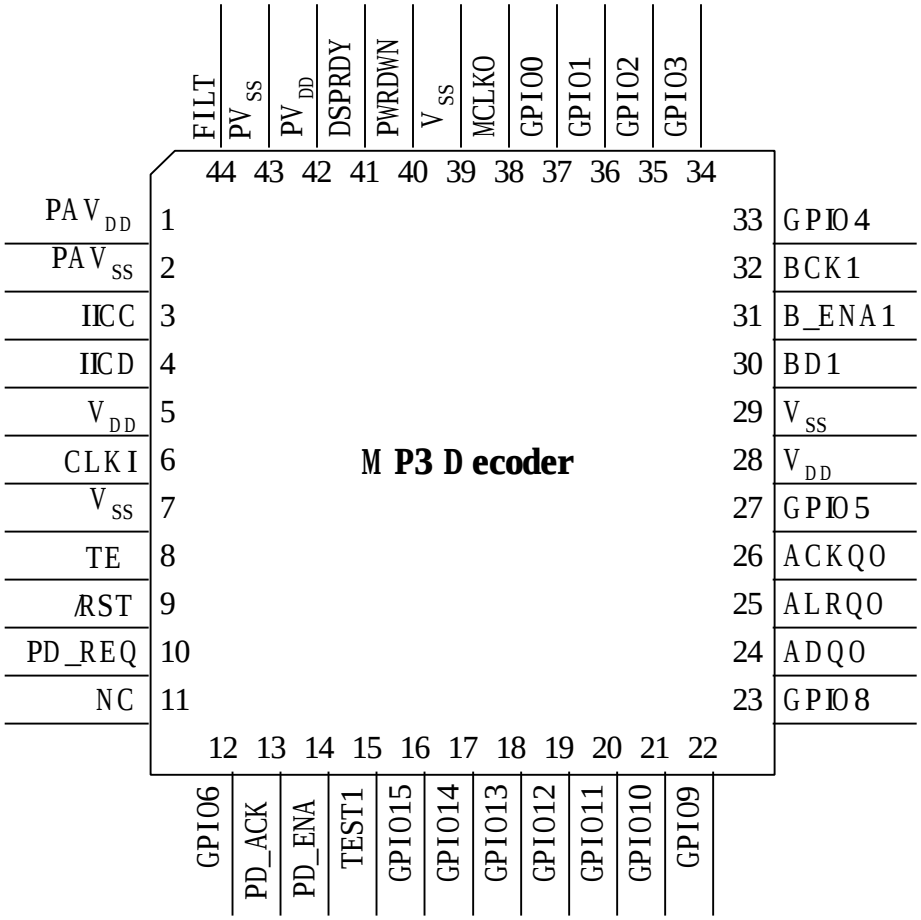


Figure 3: PT8401 Pin Configuration

Pin Description

Pin Name	I/O	Description	Pin No.
PAVDD	Power	Analog Supply Positive for PLL	1
PAVSS	Power	Analog Supply Ground for PLL	2
IICC	I/O	I^2C Clock Line	3
IICD	I/O	I^2C Data Line	4
VDD	Power	Digital Supply Positive	5
CLKI	I	Clock Input	6
VSS	Power	Digital Supply Ground	7
TE	I	Test Enable	8
/RST	I	Reset	9
PD_REQ	O	Parallel Data Request	10
NC	-	No Connection	11
GPIO6	I/O	General Purpose IO 6	12
PD_ACK	O	Parallel Data Acknowledge Signal	13
PD_ENA	I	Parallel Data Enable Transmission	14
TEST1	I	Test Pin. It is advisable to connect to Digital Ground	15
GPIO15/DATA_REQ	I/O	General Purpose IO15 or Data Request	16
GPIO14	I/O	General Purpose IO14	17
GPIO13	I/O	General Purpose IO13	18
GPIO12/ACKQI2	I/O	General Purpose IO12 or Second Serial Input Clock	19
GPIO11/ALRQI2	I/O	General Purpose IO11 or Second Serial Input Frame Identification	20
GPIO10/ADQI2	I/O	General Purpose IO10 or Second Serial Input Data	21
GPIO9	I/O	General Purpose IO9	22
GPIO8	I/O	General Purpose IO8	23
ADQO	O	Serial Output Data	24
ALRQO	O	Serial Output Frame Identification	25
ACKQO	O	Serial Output Clock	26
GPIO5	I/O	GPIO5 or Start-Up Configuration	27
VDD	Power	Digital Supply Positive	28
VSS	Power	Digital Supply Ground	29
BD1	I	First Serial Input Data	30
B_ENA1	I	First Serial Input Frame Identification	31

Pin Name	I/O	Description	Pin No.
BCK1	I	First Serial Input Clock	32
GPIO4	I/O	General Purpose IO4 or Start-Up Configuration	33
GPIO3	I/O	General Purpose IO3 or Start-Up Configuration	34
GPIO2	I/O	General Purpose IO2 or Start-Up Configuration	35
GPIO1	I/O	General Purpose IO1 or Start-Up Configuration	36
GPIO0	I/O	General Purpose IO0 or Start-Up Configuration	37
MCLKO	O	Master Oversampling Clock Output for DAC	38
VSS	Power	Digital Supply Ground	39
PWRDWN_	I	Power Down Control	40
DSPRDY	O	Decoder Operation Ready	41
PVDD	Power	Digital Supply Positive for PLL	42
PVSS	Power	Digital Supply Ground for PLL	43
FILT	Passive	Connect to Capacitor 820pF.	44

Functional Description

System and Interface Description

PT8401 is capable of decoding MPEG audio bitstream through a serial data interface. With proper external A/D converter, it is capable of encoding audio signal by the ADPCM Method. The primary operating mode of PT8401 is divided into three sections: MP3 Decoder, ADPCM Encoder and ADPCM Decoder.

MP3 Decoding Mode: The bitstream input may either be from the first serial bitstream interface or parallel bitstream interface depending on the **SP_SEL** command. After processing, the audio data is outputted through the serial output interface. The controller can get bitstream information through GPIO or I^2C interface even while the process is still in operation.

ADPCM Encoding Mode: By connecting additional A/D to the second serial data interface and by issuing several basic commands like **SetMode** and **AdpcmMode** via I^2C or GPIO, PT8401 can start ADPCM encoding, bitstream output through GPIO. Please refer to the Start-up Configuration and GPIO Setting Section for detailed timing diagram.

ADPCM Decoding Mode : Same as MP3 Decoding Mode, except that the commands **SetMode** and **AdpcmMode** have to be set to ADPCM Decoding Mode.

The basic operation modes of PT8401 are Stop and Play. After all the necessary commands are set properly (like SP_SEL , PLL setting etc.), PT8401 will enter decoding/encoding process by issuing a **Play** command at address 0x40 through I^2C interface.

Besides, the MP3 decoding, PT8401 offers two additional modes, namely: Pause and Fast Forward . The Pause Mode will stop MP3 decoding, wait for the PLAY command set to the other mode. If PLAY=0x01 is issued, PT8401 will resume playing from the broken point. The Fast Forward Mode is achieved with the help of command Fward_Num(number of frame to play) and Skip_Num(number of frame to skip.

Serial Audio Interface

SERIAL OUTPUT INTERFACE

In the serial audio output interface, following signals are generated:

MCLK : Master Clock, configured as 256fs or 384fs according to **MclkSel** command.
ADQO: Serial Data Output
ACKQO: Bit Clock Output, derived from MCLK
ALRQO: Left/Right Channel Word Selection

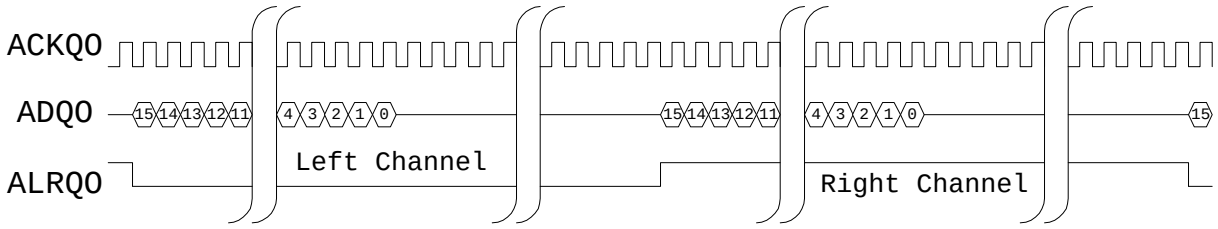
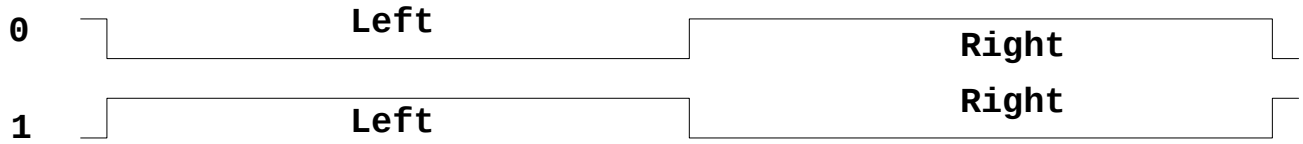


Figure 4: Serial Audio Output Timing

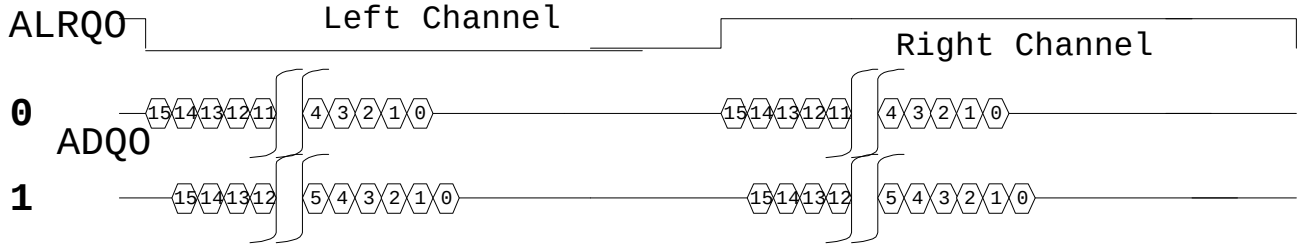
The default output waveform is show in *Figure 4*. Each PCM sample consists of a 2's complement 16-bit MSB-first data and another 16 bits of blank data forming 32 bits data in each channel. ADQO is valid at the rising edge of ACKQO and the last bit of a sample is aligned with the edges of ALRQO. However, PT8401 offers 3-bit, eight combinations to fit different kinds of audio DACs via the start-up configuration or command registers.

Bit 0 : 32/16 bits per sample selection. If 16-bit per sample is selected, each channel contains only 16-bit MSB first data.



Bit 1 : ALRQO Left Channel indicating Low/High selection.

Bit 2 : Delay Selection. When this bit is set, the transition of ALRQO is one clock cycle earlier. This is called I^2S format.



FIRST SERIAL BITSTREAM INPUT INTERFACE

Serial Bitstream (regardless of whether it is an MPEG audio or ADPCM speech bitstream) comes from this port. The following three signals are needed to make a complete transfer.

BD1: Serial Bitstream Data Input.
BCK1: Bit Clock Input.
B_ENA1: Serial Data Enable Signal, Active: Low
DATA_REQ : Data Request Signal.

Microcontroller can transmit bitstream via the following two types of connections. Please refer to the diagram below.

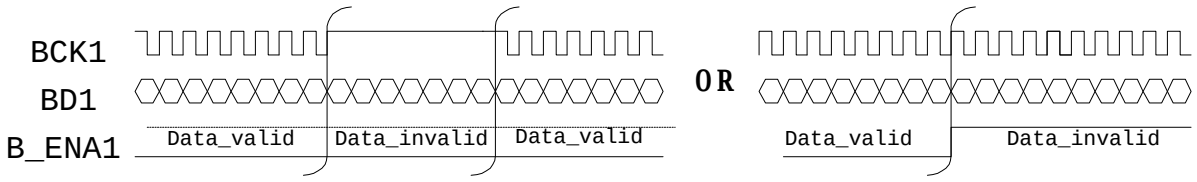


Figure 5: Timing of First Serial Bitstream Input Interface.

The maximum bit rate of MPEG is 448kbps. Basically, the speed of input bitstream clock must be greater than 448KHz. An input bitstream clock of 1MHz is recommended. Since the microcontroller doesn't know when to start the bitstream transmission, the DATA_REQ signal is needed to act as the bitstream transmission indicator. When DATA_REQ is "High", the microcontroller starts another new bitstream packet transmission. If the DATA_REQ is set to "Low" , bitstream transmission is terminated. Please refer to *Figure 6*.

Figure 6: Timing of DATA_REQ Signal

SECOND SERIAL DATA INPUT INTERFACE

This port is usually connected with the A/D Converter and is used for speech encoding. The timing of this port is the similar as that of the serial output interface, except that the signals of the Second Serial Data Input Interface are inputs. This port also can connect with various ADCs through the setting in the Start-up Configuration or command register **SetSAI2**. Two bits setting is described below :

Bit 0 : ALRQI2 Left Channel indicating Low/High Selection.
Bit 1 : Delay Selection. When this bit is set, the transition of ALRQI2 is one clock cycle earlier. This is called I^2S format.

PARALLEL BITSTREAM INPUT INTERFACE

In addition to the serial interface, the microcontroller can also transmit bitstreams via parallel interface. Parallel Mode is set via the Start-up Configuration or command register **SP_SEL**. Parallel data transmission consists of the following signals:

1. PD_REQ : Parallel Data Request. A bundle of data may be requested and this is sent from PT8401.
2. PD_ENA : Parallel Data Enable. This means that the data in the data bus is valid. This is sent from microcontroller.
3. PD_ACK : Parallel Data Acknowledge. This means that the decoder has received one byte successfully. This is sent from PT8401.
4. P_DATA : Parallel Data Bus is GPIO[15:8]. The GPIO15 is MSB and GPIO8 is LSB.

Due to some low speed transmission, the microcontroller may not be fast enough to know that PT8401 has closed communication. Please refer to the example described in Figure 6 wherein during the byte 7 transmission. In this example, PT8401 did not recognize an Acknowledge signal; thus, byte 7 was not transmitted correctly.

In order to avoid instability, it is better not to set **SP_SEL** frequently.

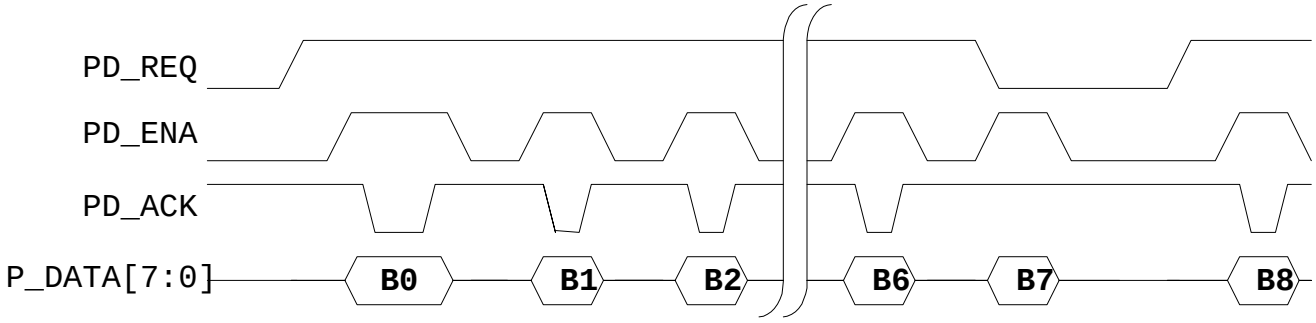


Figure 7 : Parallel Data Transmission Timing

PLL

PLL circuit provides two internal clocks, one for DSP and the other for the audio interface. The DSP clock rate is twice that of the external clock while the audio interface clock rate is dependent on the external audio clock. In order to satisfy different frequency settings, the PLL clock is divided into two sets.

PLLSet PLLfraction are used for all frequencies.

The default PLL setting assumes that the input frequency is 16.9344MHz. However, other frequency is acceptable, too. Please refer tables below for more information. If frequency is not on the list, please contact to PTC.

Table 1. Settings for input frequency 10 MHz.

Register Name	Value
PLLSet	0x3c20
PLLFraction	0x7f80

Table 2. Settings for input frequency 14.318MHz.

Register Name	Value
PLLSet	0x3b30
PLLFraction	0x7e88

Table 3. Settings for input frequency 14.725MHz.

Register Name	Value
PLLSet	0x3930
PLLFraction	0x7ed1

Table 4. Settings for input frequency 12.288MHz.

Register Name	Value
PLLSet	0x3b28
PLLFraction	0x7e5e

The sampling frequency of ADPCM encoding is controlled by Serial Input Port 2; however, the sampling frequency of ADPCM decoding is controlled via the setting of PLL. The microcontroller has to be set properly to get the right listening results. The default setting for ADPCM decoding assumes that sampling frequency is 8kHz; however, 11.025kHz and 12kHz are selectable, too.

Start-up Configuration and General Purpose IO

PT8401 offers another easy way to configure the basic start-up setting without using the external controller. It is called "Start-up" Configuration. GPIO pins are configured as input pins before RESET. After RESET, those values are latched to be the basic configuration of PT8401. After start-up, the GPIO pins are configured as output pins.

START-UP CONFIGURATION

GPIO	Name	Description
0	**SetMode**	"0" : MPEG Mode "1" : ADPCM Mode
1	**AdpcmMode**	"0" : Bitstream Decoding "1" : Sample Encoding.
2	**SP_SEL**	"0" : First Serial Port "1" : Parallel Input Port Selection (only in MPEG Decoding).
3	**Set_SAO[0]**	Set Serial Output Port. Same as Main Function Selection.
4	**Set_SAO[1]**	
5	**Set_SAO[2]**	
6	**Set_SAI2[0]**	Set Second Serial Input Port. Same as Main Function Selection.
7	**Set_SAI2[1]**	

GPIO PINS DURING MPEG DECODING

GPIO	Name	Description
0	**MPEG ID**	"0" : MPEG2 "1" : MPEG1
1	**Layer Info**	"0" : Layer III. "1" : Layer I or Layer II.
3,2	**Sampling Frequency**	"00" : 44.1/22.05 kHz "01" : 48/24 kHz "10" : 32/16 kHz "11" : reserved.
4	**FRAME SYNC_INFO**	An indicator for frame sync information. The period between two sync info is less than 72 ms. The controller can treat this pin as a new frame is decoded or if decoder is dead. Or every time this pin go high, new ancillary is update and can be download via I^2C interface.
5	**CRC ERROR**	"0" : no error. "1" : CRC_error or bitstream error.
6	**Half_second**	Half second indicator. The period between two high signal is half second
15	**Demand Signal**	(No effect during parallel mode). "0": no request. "1": Ask for bitstream input.

GPIO PINS DURING ADPCM ENCODING

GPIO	Name	Description
0	**Enc_Dat[0]**	LSB, 4-bit data during ADPCM Encoding.
1	**Enc_Dat[1]**	
2	**Enc_Dat[2]**	
3	**Enc_Dat[3]**	MSB
4	**Enc_ENA**	"0" : Disable Encoded Data Output "1" : Enable Encoded Data Output

SPEECH ADPCM ENCODING TIMING

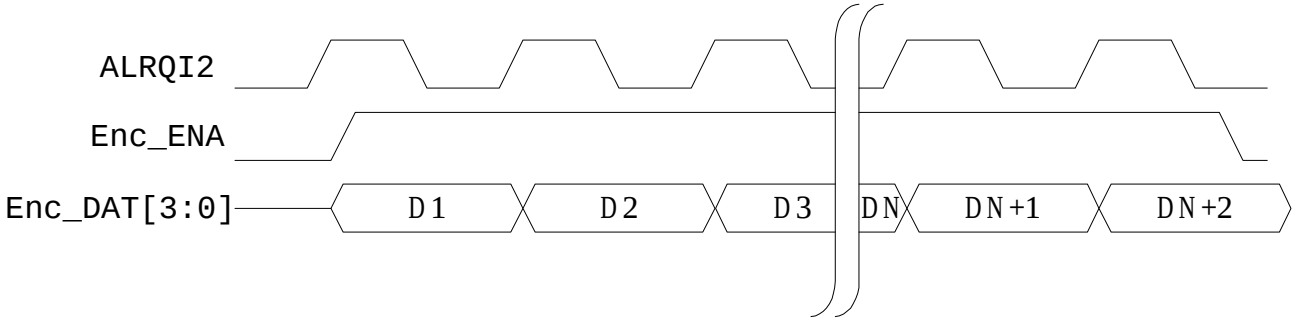


Figure 8: Speech ADPCM Encoding Timing.

In *Figure 8,* ALRQI2 assumes that the command register **Set_SAI2** bit 0 is"0". If Bit 0 is set to "1", the signal ALRQI2 in *Figure 8* should be inverted.

I²C Microprocessor Interface

PT8401 uses I²C interface for communication. I²C communicate with multi devices using only two lines; namely: IICD and IICC. The following control and status registers are accessible via I²C interface.

- **S** is a Start Bit (a start condition). Any transmission must start with it.
- **Dev_addr** is a 7-bit Device Address Identifier. Each device can only have one address. PT8401 is fixed at "0110100b".
- **R/W** issues a read or write operation
- **A/A** is an Acknowledge Bit. It is performed in the receiver and is used to inform the transmitter that the data is properly received or used to stop data transmission.
- **P** is a Stop Bit. Any sequence must end with it.

The I²C write operation is a word (two-byte) writing mode, as described in Figure 8. Multi-byte write is

allowable, but PT8401 only receives it and does nothing. PT8401 is capable of the following read operations: Word Read, Multi-byte Read and Repeat Address Read Modes. In the Repeat Address Read Mode, the last successful transmitted address is read again even if the decoder has not been informed of the address. This mode is usually used for the address 0x00, **FrameCount**, which maybe the most frequently requested address in all command registers. In PT8401, only the command **AncillaryData** is allowed to use the Multi-byte Read Mode. Since **A**, no acknowledge signal is controlled by the receiver (microcontroller) in the read mode, the microcontroller will receive repeated data after 3rd byte in other command registers in Multi-byte Read Mode.

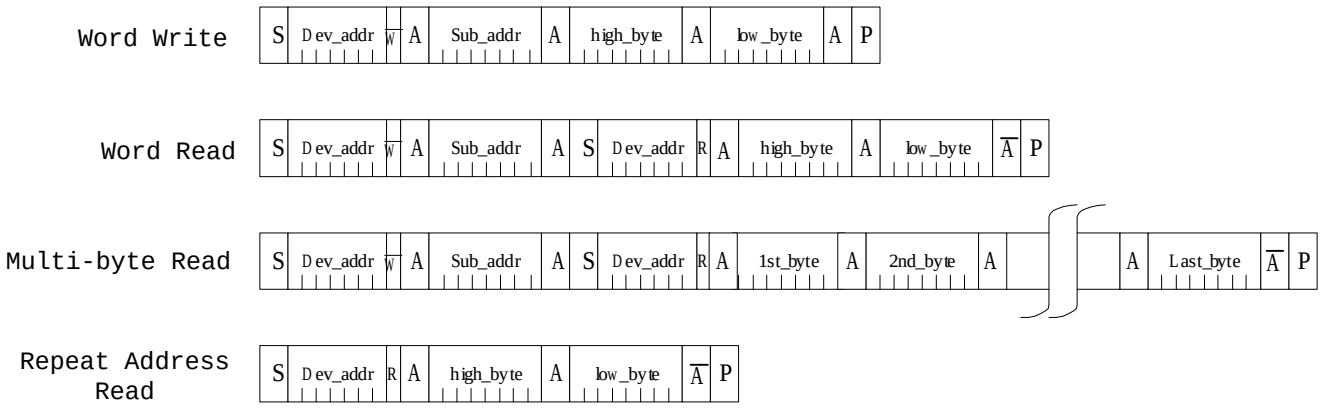


Figure 9: Read and Write Sequence for I^2C Protocol.

POWER DOWN SETTING

To enter the Power Down Mode, Pin 40 (PWRDWN_) must be set to "LOW'. The DSPRDY pin goes to low, this indicates that PT8401 is already been powered down. There are two types of Power Down Modes, namely: Sleep Mode and the Deep Sleep Mode. The Sleep Mode turns off the DSP clock and only preserves PLL clock. The Deep Sleep on the other hand turns off DSP and PLL clock. All the commands that have been previously set will preserved. PT8401's default is the sleep mode. With the command Pwr_Dwn_Reg set to 0x04 before power down, deep sleep is achieved.

Command Registers

MAIN FUNCTION COMMAND

Address	Register Name	Description	Default	R/W
0x40	**Play**	0/1: stop/run the current operation mode. After reset, the controller set necessary command, then set this bit to 1 to start decode. 2: Pause Mode. 3: Fast Forward Mode. 4: Second Fast Forward Mode *Note:2,3,4 only work on MPEG Decoding Mode.*	0x0	R/W
0x41	**SetMode**	0 : MPEG Decoding Mode. 1 : Start ADPCM Mode. 2 : PCM bypass from First Serial Port. 3 : PCM bypass from Second Serial Port.	0x0	R/W
0x42	**ADPCMMode**	0 : ADPCM Decoding Mode 1 : ADPCM Encoding Mode.	0x0	R/W
0x43	**Mute**	1 : Mute all output signals.	0x0	R/W
0x44	**Volume**	Output Volume Control. The range is between 0 dB and -96dB(0x60).	0x0	R/W
0x45	**SP_SEL**	Serial/Parallel Input Selection. 0 : First Input Serial Port Input is selected. 1 : Input Parallel Port Input is selected. *Note : After this bit is set, it is better to run Software Reset to prevent instability.*	0x0	R/W
0x46	**Set_SAO**	Serial Output Port Mode Setting.	0x0	R/W
		Bit 0: 0 : 32 bits per sample mode. 1 : 16 bits per sample mode.		
		Bit 1: 0 : ALRQ Signal. Left is "Low". 1 : ALRQ Signal. Left is "High".		
		Bit 2: 0 : Relative Timing No Delay to ALRQ. 1 : Relative Timing One Delay to ALRQ.		
		Bit 3: 0 : Data is Left Alignment. 1 : Data is Right Alignment		

0x46	**Set_SAO**	Bit 5:4	00 : ACQO is generated from the Internal Clock. 01 : ACQO is generated from the External Clock. 10 : MCLKO is generated from the External Clock.	0x0	R/W
0x47	**Set_SAI2**	Second Serial Input Port Mode Setting		0x0	R/W
		Bit 0	0 : ALRQ Signal. Left is "Low". 1 : ALRQ Signal. Left is "High".		
		Bit 1	0 : Relative Timing No Delay to ALRQ. 1 : Relative Timing One Delay to ALRQ.		

0x59	ADPCM_FS_SEL	ADPCM Decoding Mode Sampling Frequency Selection. 0 : 11.025kHz. 1 : 12kHz. 2 : 8kHz	0x0	R/W
0x5a	Soft_Reset	Set to 1 to software reset, but all the command registers keep the setting values.	0x0	W
0x5e	Pwr_Dwn_Reg	Power Down Control Register.	0x0	W
0x63	Fward_Num	Fast Foward Mode, number of frame to be play	0x6	W
0x64	Skip_Num	Fast Foward Mode, number of frame to be skip	0x6	W

PLL SETTING COMMAND

Address	Register Name	Description	Default	R/W
0x48	MclkSel	Master Oversampling Output Clock Selection. "0" : 256fs. "1" : 384fs.	0x0	R/W
0x4b	PllSet	PLL Control Parameter Setting.	0x3b28	R/W
0x4c	PllFraction	15-bit PLL Fraction Parameter Setting.	0x7e5e	R/W

TONE AND 3D CONTROL COMMANDS

Tone control is allowable. It ranges up to +-15 dB cut or enhancement for bass and treble filter with step size of 1.5 dB. Although overflow prevention is performed, under the Bass Enhancement Mode, the gain may be reduced so that overflow may be prevented in advance by issuing the **prescale** command. This would generate better listening results.

The cut off frequency for bass filter is about 250Hz for MPEG1, 125Hz for MPEG2.
The cut off frequency for treble filter is about 10kHz for MPEG1, 5kHz for MPEG2.

The 3D Mode controls the 3D effect function. Please take note that if the 3D Mode is enabled, the tone and balance controls are disabled.

Address	Register Name	Description	Default	R/W
0x50	**Tone3D**	"0" : Enable Tone Control. "1" : Enable 3D Control.	0x0	R/W
0x51	**Bass**	"0x1" to "0xa" with step size 1.5dB bass enhancement. Maximum up to 15 dB. "0xb" to "0x14" with step size 1.5dB bass attenuation.. Minimum down to –15 dB Default is" 0x0", no enhancement.	0x0	R/W
0x52	**Treble**	"0x1" to "0xa" with step size 1.5dB treble enhancement. Maximum up to 15 dB. "0xb" to "0x14" with step size 1.5dB treble attenuation. Minimum down to –15 dB. Default is "0x0", no enhancement.	0x0	R/W
0x53	**Prescale**	Prescale command to reduce overall gain. Range is between 0dB(0x0) and –96dB(0x60)	0x0	R/W
0x54	**3D_Effect**	Control the Depth of 3D's Effect. Range is between between 0dB(0x0) and –96dB(0x60)	0x3	R/W

BALANCE CONTROL COMMAND

Balance control is implemented through 4 coefficients setting as shown in Figure 9.

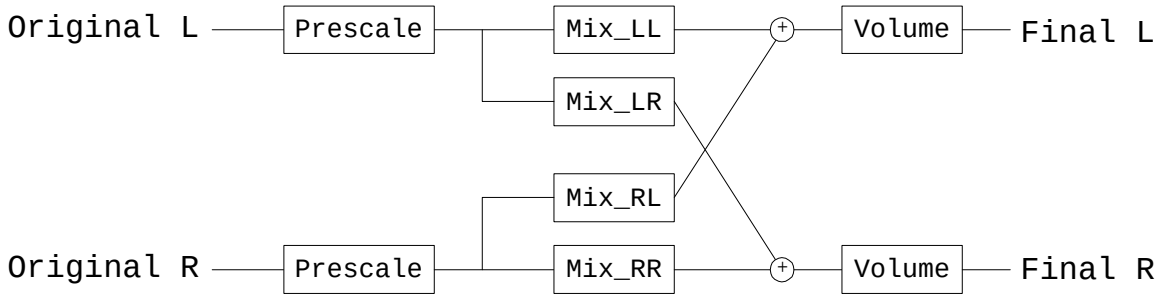


Figure 10: Balance Control Relation.

Address	Register Name	Description	Default	R/W
0x55	**Mix_LL**	Mix original left channel to output left channel with 0 dB to –96 dB(0x60). Default is 0x0.	0x0	R/W
0x56	**Mix_RL**	Mix original right channel to output left channel with 0 dB to –96 dB(0x60). Default is 0x60.	0x60	R/W
0x57	**Mix_LR**	Mix original left channel to output right channel with 0 dB to –96 dB(0x60). Default is 0x60	0x60	R/W
0x58	**Mix_RR**	Mix original right channel to output right channel with 0 dB to –96 dB(0x60). Default is 0x0.	0x0	R/W

STATUS REGISTER COMMANDS

Address	Register Name	Description							Default	R/W
0x00	**Frame Count**	Increase one every frame, but if the following condition happen, it clear to 0. 1.enter stop command , 2.crc check error. 3.bitstream error.							0x0	R
0x01	**MPEG Header Info1**	**Bit**	**Item**	**Description**					0x0	R
		4..15		Reserved						
		3	ID	1:MPEG1 0:MPEG2						
		1:2	Layer	11 : Layer I 10 : Layer II 01 : Layer III 00 : reserved						
		0	Protection	0 : protected by CRC, 1 : don't						
0x02	**MPEG Header Info2**	**Bit**	**Item**	**Description**					0x0	R
		12..15	Bit Rate Index(kbps)	mpeg1 layer I	mpeg1 Layer II	mpeg1 layer III	mpeg2 Layer I	mpeg2 Layer II Layer III		

			0000	Free	Free	Free	Free	Free		
			0001	32	32	32	32	8		
			0010	64	48	40	48	16		
			0011	96	56	48	56	24		
			0100	128	64	56	64	32		
			0101	160	80	64	80	40		
			0110	192	96	80	96	48		
			0111	224	112	96	112	56		
			1000	256	128	112	128	64		
			1001	288	160	128	144	80		
			1010	320	192	160	160	96		
			1011	352	224	192	176	112		
			1100	384	256	224	192	128		
			1101	416	320	256	224	144		
			1110	448	384	320	256	160		
			1111	forbidden	forbidden	forbidden	forbidden	forbidden		
		10..11	Sampling frequency	MPEG1		MPEG2				
			00	44.1kHz		22.05kHz				
			01	48kHz		24kHz				
			10	32kHz		16kHz				
			11	reserved		reserved				
		9	Padding_bit							
		8	Private bit							
		Bit	**Item**	**Description**					0xff	R
		6..7	mode							
			00	Stereo						
			01	Joint_stereo						
			10	Dual_channel						
			11	Single_channel						
		4..5	Mode_extension	Layer I,II		Layer III				
				mode=joint_stereo		Intensity_ Stereo	Ms_stereo			

			00	Subband=4-31	Off	Off		
			01	Subband=8-31	On	Off		
			10	Subband=12-31	Off	On		
			11	Subband=16-31	On	On		
		3	copyright	0:not protected, 1: protected				
		2	original	0:copy, 1:original				
		0..1	emphasis	Indicate which type of emphesis is used				
			00	None				
			01	50/15 microseconds				
			10	reserved				
			11	CCITT J.17				
0x03	**NumAncillaryBits**	Current frame contain number of ancillary bits contain in current frame. Update in every frame.					0x0	R
0x04.	**AncillaryData**	Current frame's ancillary data. Update in every frame. Maximum is 56 bytes.					0x0	R
0x05	**Error Status**	Bit 0 : Set to 1 : indicates CRC check error. Bit 1 : Set to 1 means bitstream error. The following several condition may cause error : 1). Information in MPEG header point to "reserved" condition.(layer to "00", sampling frequency to "11"). 2). Bit rate index point to free and forbidden condition.					0x0	R

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Digital supply voltage	V_{DD}	2.7	4	V
T_A	Ambient Operating Temperature		-10	85	?C

Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating			25		?C

	temperature					
V_{SUP}	Digital supply voltage	V_{DD}		3.3		V

INPUT LEVEL :

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	V_{DD}
V_{IH}	Input high voltage @ V_{DD} = 2.7V ~ 4V	/RST,PD_ENA, PWR_DWN, IICC, IICD, GPIO	1.7			V	2.7
			1.7				3.3
			1.9				4.0
V_{IL}	Input low voltage @ V_{DD} = 2.7V ~ 4V				0.6		2.7
					0.8		3.3
					1.0		4.0

OUTPUT LEVEL :

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	V_{DD}
V_{OH}	Output high voltage	ADQO,ALRQO, ACKQO,PD_REQ, PD_ACK,DSP_RDY			V_{DD}-0.1	V	2.7
					V_{DD}-0.1		3.3
					V_{DD}-0.1		4.0
V_{OL}	Output low voltage	ADQO,ALRQO, ACKQO,PD_REQ, PD_ACK,DSP_RDY	V_{SS}+0.1				2.7
			V_{SS}+0.1				3.3
			V_{SS}+0.1				4.0

Current consumption

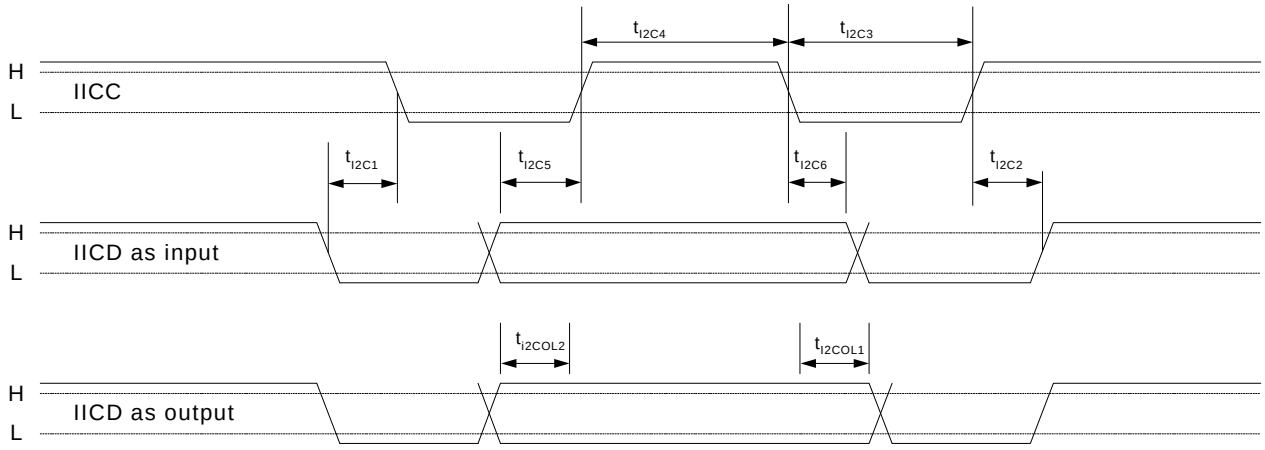
At T_a = 0 to 70 ,

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Current consumption	All supply pins		85		mA	V_{DD} = 4V
I_{DD}				64		mA	V_{DD} = 3.3V
I_{DD}				45		mA	V_{DD} = 2.7V

I^2C Bus Characteristics

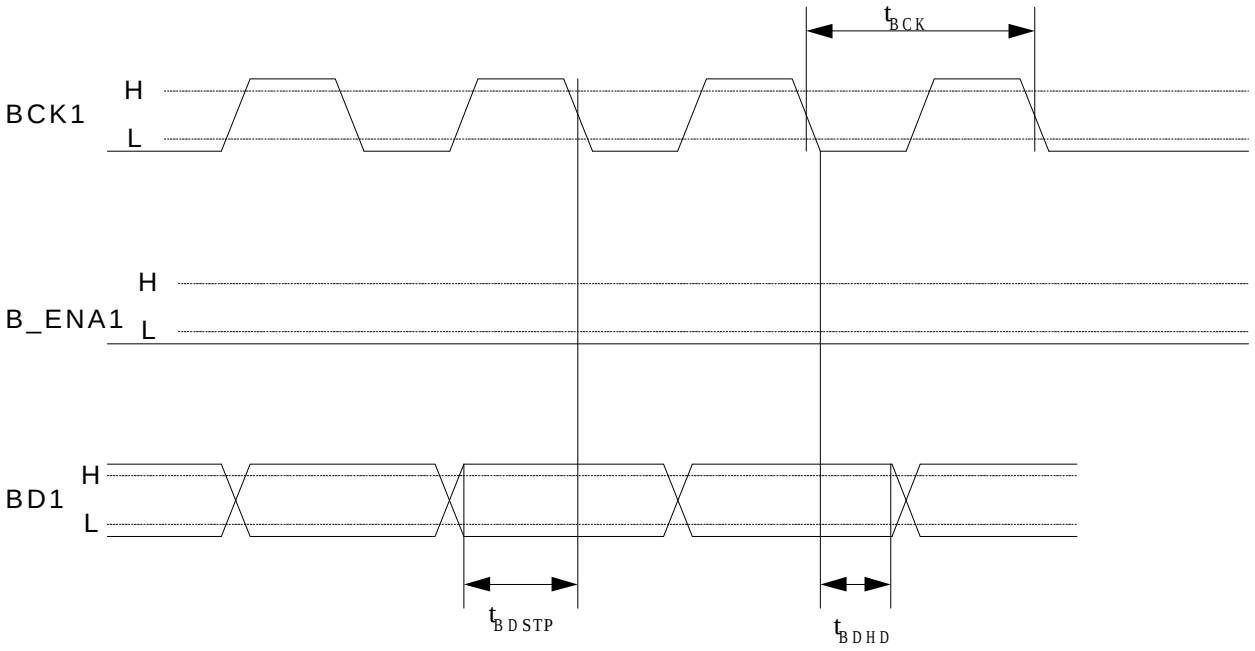
Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit	Test Condition

		Name					
F_{I2C}	I^2C bus frequency	IICC			400	Khz	@CLKI = 8Mhz
T_{I2C1}	I^2C start condition setup time	IICC, IICD	250			ns	@CLKI = 8Mhz
T_{I2C2}	I^2C stop condition setup time	IICC, IICD	250			ns	@CLKI = 8Mhz
T_{I2C3}	I^2C Clock low pulse time	IICC	600			ns	@CLKI = 8Mhz
T_{I2C4}	I^2C Clock high pulse time	IICC	600			ns	@CLKI = 8Mhz
T_{I2C5}	I^2C data hold time before rising edge of clock	IICC	80			ns	@CLKI = 8Mhz
T_{I2C6}	I^2C data hold time after falling edge of clock	IICC	80			ns	@CLKI = 8Mhz
T_{I2COL1}	I^2C data output hold time after falling edge of clock	IICC, IICD	30			ns	@CLKI = 8Mhz, F_{I2C}= 400Khz
T_{I2COL2}	I^2C data output setup time before rising edge of clock	IICC, IICD	0			ns	@CLKI = 8Mhz



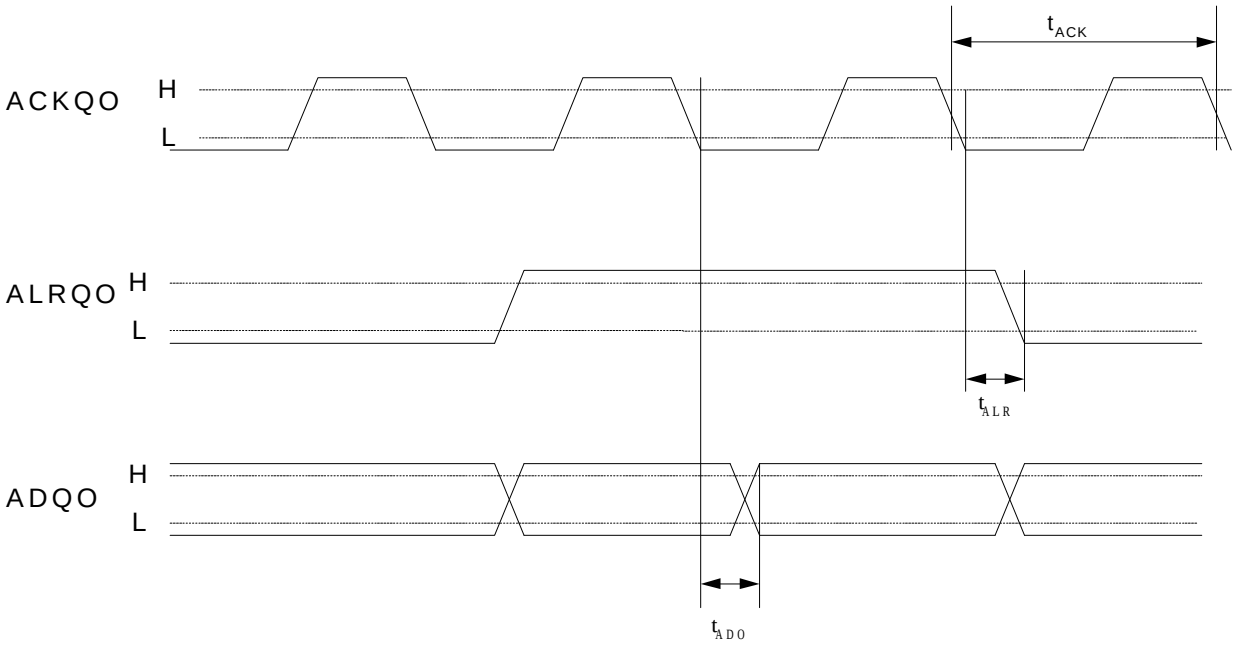
I^2S Characteristics - Serial input

Symbol	Parameter	Pin Name	Min	Typ.	Max.	Unit	Test Conditions
t_{BCK}	I^2S clock input clockperiod	BCK1				ns	
t_{BDSTP}	I^2S data setup time before falling edge clock	BCK1, BD1	10		3	ns	@ CLKI = 16.9344MHz, 44.1Khz/Stereo, 32 bits
t_{BDHD}	I^2S data hold time after falling edge of clock	BCK1, BD1	10		3	ns	



I²S Characteristics - Serial output

Symbol	Parameter	Pin Name	Min	Typ.	Max.	Unit	Test Conditions
t_{ACK}	I²S clock output frequency	ACKQO		354		ns	@ CLKI = 16.9344MHz, 44.1Khz/Stereo, 32 bits
t_{ALR}	I²S worst strobe hold time after falling edge of clock	ACKQO, ALRQO	1		3	ns	
t_{ADQ}	I²S data hold time after falling edge of clock	ACKQO, ADQO	1		3	ns	



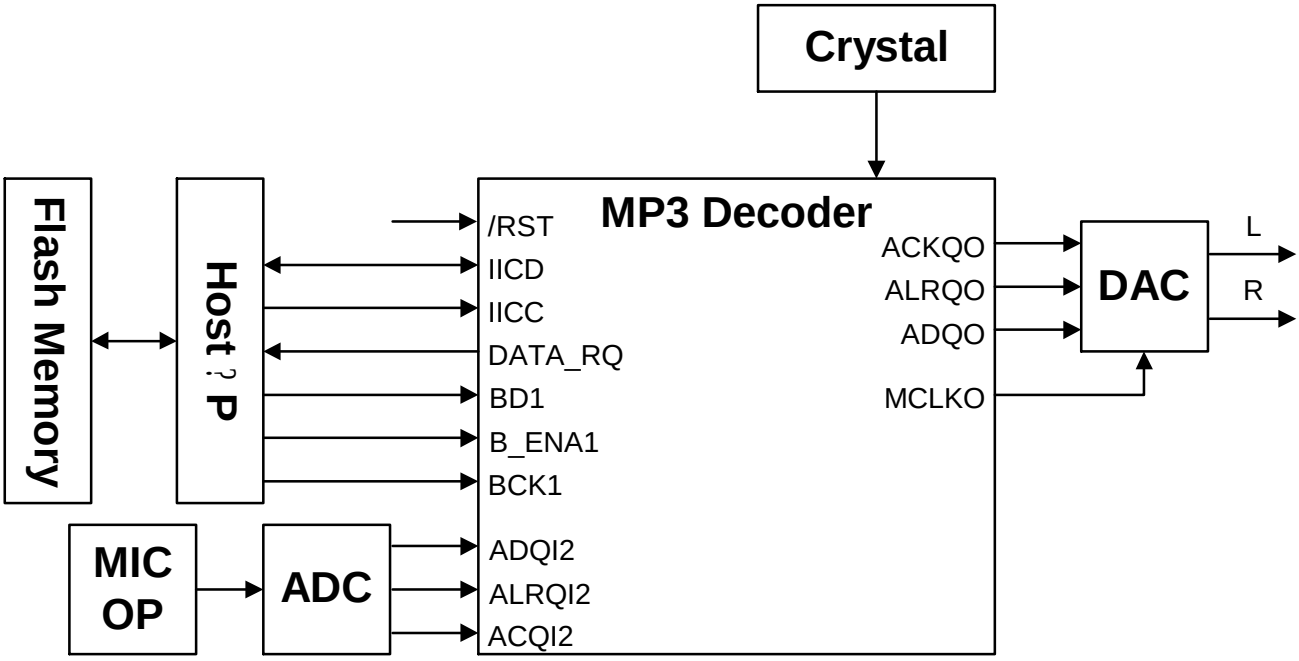
Firmware Characteristics

Symbol	Parameter	Pin Name	Min	Typ.	Max.	Unit	Test Conditions
Synchronization Times							
$t_{mpgsync}$	Synchronization on MPEG bitstreams			24	72	ms	MPEG1 layer 3, 44.1Khz, 128Kbits/sec

Order Information

Valid Part Number	Package Type
PT8401	44-pins, LQFP Package

Application Circuit



Package Information

44 -Pin, LQFP Package (Body Size: 10x10 mm, Pitch: 0.80mm, THK Body: 1.40mm)