LCK4953
Low-Voltage PLL Clock Driver

Features

- Fully integrated PLL
- Output frequency up to 130 MHz in PLL mode
- Nine outputs with high-impedance disable
- 32-lead TQFP
- 50 ps cycle-to-cycle jitter
- Pin compatible with the *Motorola*® MPC953 clock driver

Description

The LCK4953 is a PLL-based clock driver device intended for high-performance clock tree designs. The LCK4953 is 3.3 V compatible with output frequencies of up to 130 MHz and output skews of 75 ps. The LCK4953 can meet the most demanding timing requirements and employs on-chip voltage regulators to minimize cycle-to-cycle jitter and phase jitter.

The LCK4953 is ideal for use as a zero delay, low skew, fan-out buffer due to its differential LVPECL reference input along with an external feedback input. The MROEB pin of the LCK4953, when driven high, will reset the internal counters and 3-state the output buffers. The LCK4953 has been optimized for zero delay performance.

The LCK4953 is fully 3.3 V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50 Ω transmission lines. For series-terminated 50 Ω lines, each of the LCK4953 outputs can drive two traces giving the device an effective fan-out of 1:18. For the optimum combination of board density and performance, the device is packaged in a 7 mm × 7 mm 32-lead TQFP package.

Table 1. Function Table

BYPASSB	Function
1	PLL Enabled
0	PLL Bypass
MROEB	**Function**
1	Outputs Disabled
0	Outputs Enabled
VCOSEL	**Function**
1	÷ 8
0	÷ 4
PLLEN	**Function**
1	Select VCO
0	Select PELCLK

Description (continued)

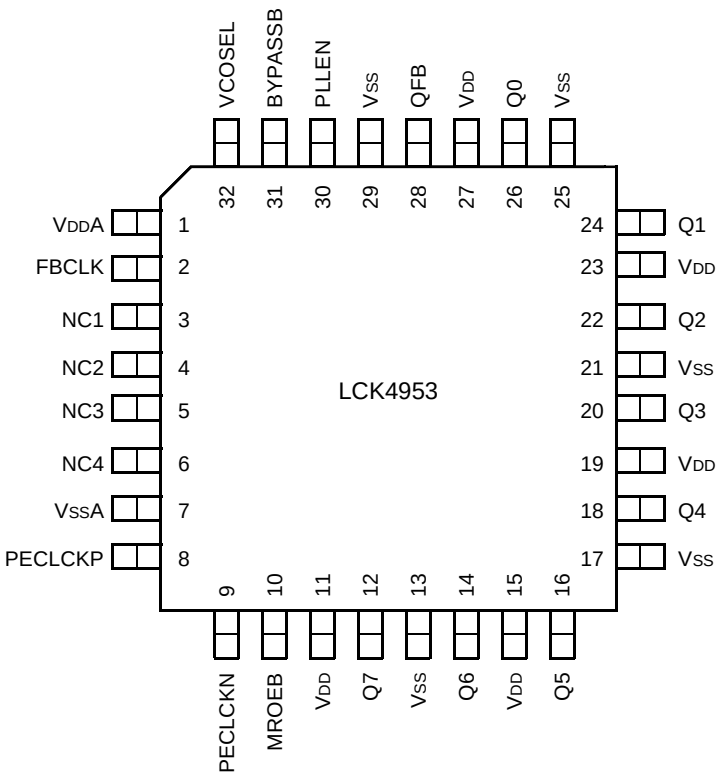

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Figure 1. 32-Lead Pinout (Top View)

Absolute Maximum Ratings

Stresses which exceed the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods of time can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	–0.3	4.2	V
Input Voltage	V_{IN}	–0.3	V_{DD} + 0.3	V
Input Current	I_{IN}	—	±20	mA
Storage Temperature Range	T_{stg}	–40	125	°C

Absolute Maximum Ratings (continued)

Table 3. dc Characteristics (T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input High-voltage LVCMOS Inputs	V_{IH}	2.0	—	3.6	V	—
Input Low-voltage LVCMOS Inputs	V_{IL}	—	—	0.8	V	—
Peak-to-peak Input Voltage PECL_CLK	Vp-p	300	—	1000	mV	—
Common-mode Range PECL_CLK	V_{CMR}	V_{DD} – 1.5	—	V_{DD} – 0.6	mV	—*
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –30 mA†
Output Low Voltage	V_{OL}	—	—	0.6	V	I_{OL} = 30 mA†
Input Current	I_{IN}	—	—	±120	µA	—
Input Capacitance	C_{IN}	—	—	4	pF	—
Power Dissipation Capacitance	Cpd	—	12	—	pF	Per output
Maximum Quiescent Supply Current Non-PLL	I_{DDQ}	—	—	1	mA	All V_{DD} pins except V_{DDA}‡
Maximum PLL Supply Current	I_{DDPLL}	—	—	45	mA	V_{DD}A pin only

* V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the high input is within the V_{CMR} range and the input swing lies within the Vp-p specification.
† The LCK4953 outputs can drive series- or parallel-terminated 50 Ω (or 50 Ω to V_{CC}/2) transmission lines on the incident edge.
‡ Total Power = (I_{DDPLL} + I_{DDQ} + fCV) * V; where f = fref, V = V_{DDD}, C = total load capacitance on all outputs.

Table 4. PLL Input Reference Characteristics (T_A = 0 °C to 70 °C)

Parameter	Symbol	Min	Max	Unit	Condition
Reference Input Frequency	fref	25	130	MHz	—
Reference Input Duty Cycle	trefdc	25	75	%	—

Table 5. ac Characteristics (T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Rise/Fall Time	tr, tf	0.10	—	1.0	ns	0.8 V to 2.0 V
Output Duty Cycle	tpw	47	50	53	%	—
Output-to-output Skews	tsk(O)	—	—	75	ps	—
PLL V_{CO} Lock Range	fV_{CO}	200	—	520	MHz	—
Frequency Output: Frequency PLL Bypass Mode	fout	25 50 —	— — —	65 130 250	MHz MHz MHz	VCOSEL = 1 VCOSEL = 0 —
Input to Ext_FB Delay (with PLL locked)	tpd (lock)	–75	—	125	ps	tref = 75 MHz
Input to Q Delay	tpd(bypass)	3	—	7	ns	PLL bypassed
Part to Part Delay				1.5		
Output Disable Time	tPLZHZ	—	—	7	ns	—
Output Enable Time	tPZL	—	—	6	ns	—
Cycle-to-cycle Jitter (peak-to-peak)	tjitter	—	—	50	ps	fout > 75 MHz

Electrical Characteristics

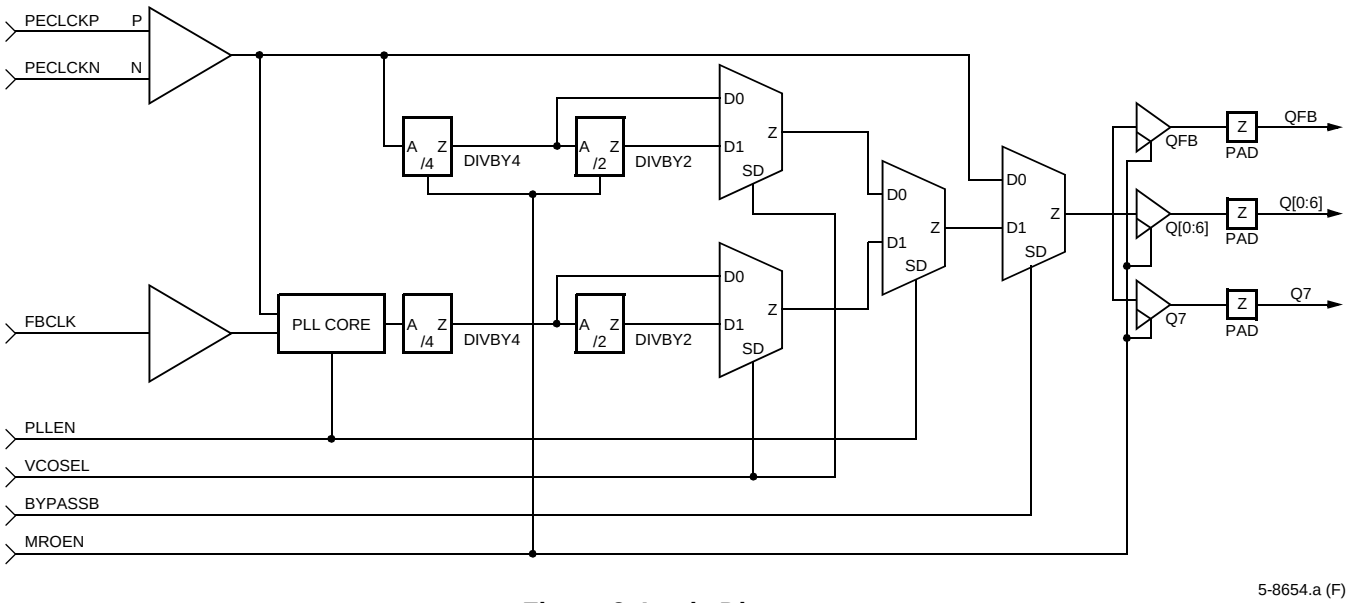

Figure 2. Logic Diagram

Power Supply Filtering

The LCK4953 is a mixed-signal product which is susceptible to random noise, especially when this noise is on the power supply pins. To isolate the output buffer switching from the internal phase-locked loop, the LCK4953 provides separate power supplies for the phase-locked loop ($V_{DD}A$) and for the output buffers (V_{DD}). In a digital system environment, besides this isolation technique, it is highly recommended that both V_{DDA} and V_{DD} power supplies be filtered to reduce the random noise as much as possible.

Figure 3 illustrates a typical power supply filter scheme. A filter for the LCK4953 should be designed to target noise in the 100 kHz to 10 MHz range, due to its susceptibility to noise with spectral content in this range. The RC filter in Figure 3 will provide a broadband filter with approximately –40 dB attenuation for noise with spectral content above 20 kHz. More elaborate power supply schemes may be used to achieve increased power supply noise filtering.

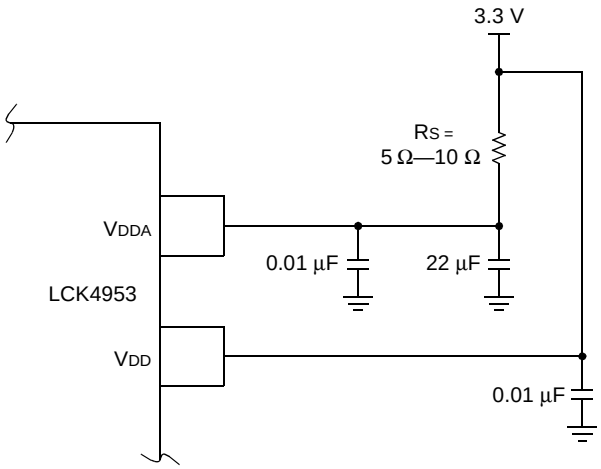

Figure 3. Power Supply Filter

Electrical Characteristics (continued)

Driving Transmission Lines

The LCK4953 clock driver was designed to drive high-speed clock terminals in a terminated transmission line environment. Point-to-point distribution of signals is a common method in most high-performance clock networks. Either series-terminated or parallel-terminated transmission lines can be used in a point-to-point scheme. The parallel technique terminates the signal at the end of a line with a 50 Ω resistance to VDD/2. This draws a fairly high level of dc current. Due to this aspect, only a single terminated line can be driven by each output of the LCK4953 clock driver. For the series-terminated case, however, there is no dc current draw; in turn, the outputs are capable of driving multiple series-terminated lines.

Figure 4 illustrates an output driving a single series-terminated line.

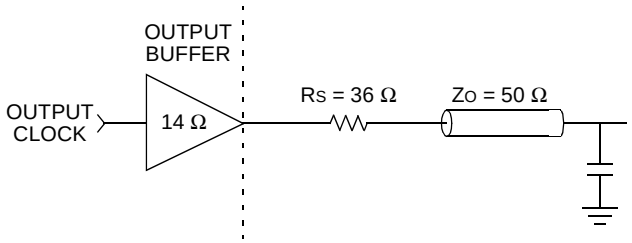

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Figure 4. Single Transmission Line

In Figure 4, because the output buffer has an impedance of 14 Ω, the series resistance (Rs) is set at 36 Ω. This ensures that the total impedance is matched with the 50 Ω transmission line.

Figure 5 illustrates an output driving two series-terminated lines.

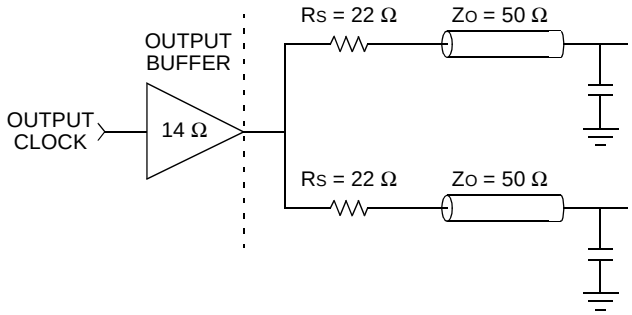

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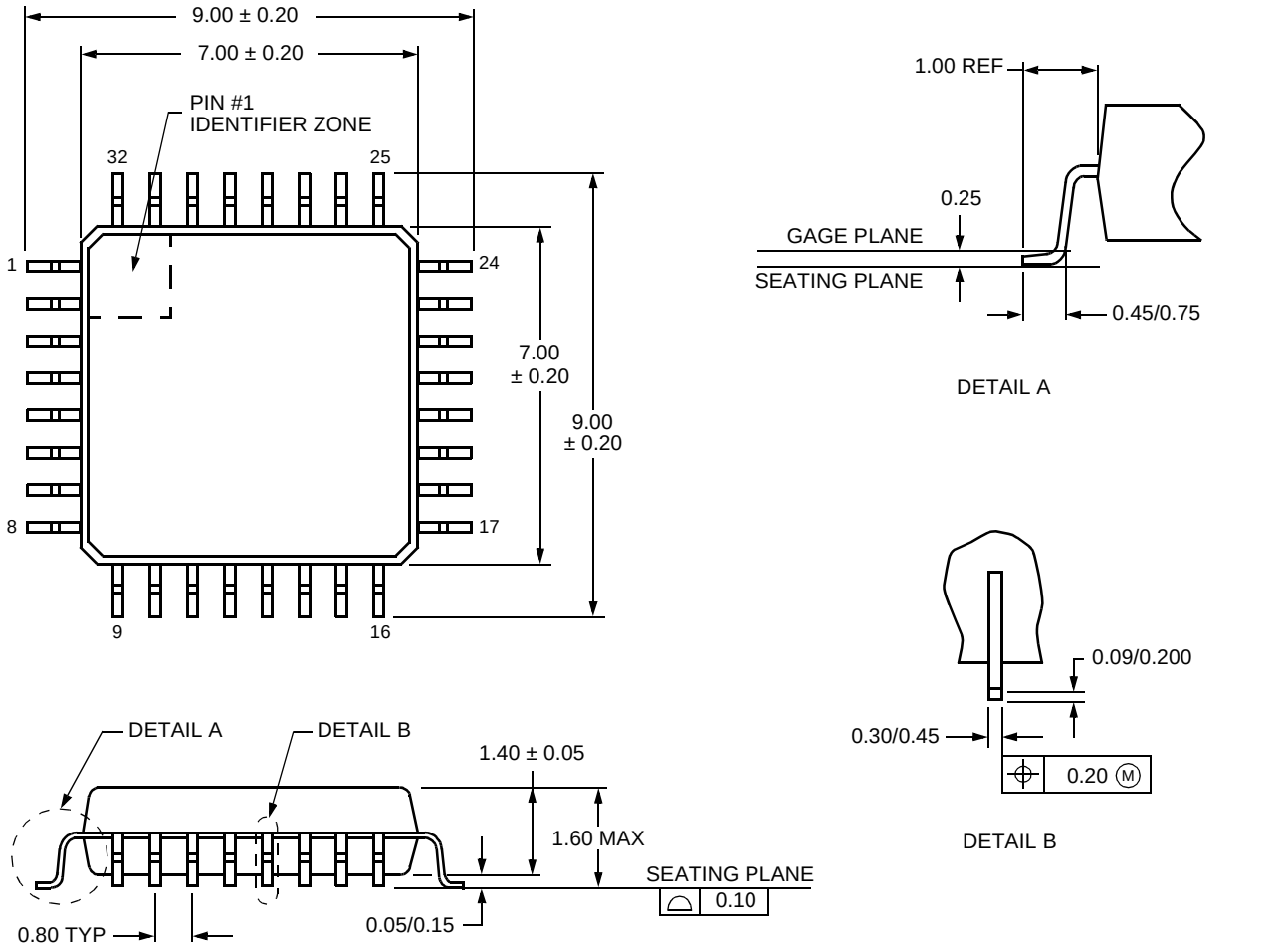
Figure 5. Dual Transmission Lines

In Figure 5, the two series resistors (Rs) are set at 22 Ω because the 14 Ω output buffer can be viewed as two 28 Ω resistors in parallel. Accordingly, for each transmission line, the impedance is well matched.

Outline Diagram

32-Pin TQFP

Dimensions are in millimeters.



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