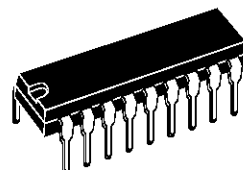


**5 CHANNELS VIDEO SWITCH**

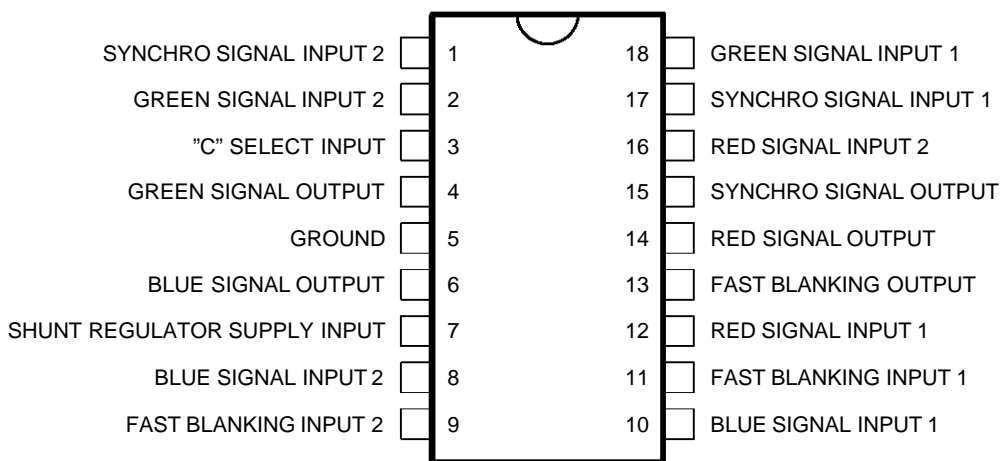
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6dB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30MHz BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7V SHUNT REGULATOR FOR :
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- THE FIVE CHANNELS ARE SIMULTANEOUSLY SWITCHED BY ONLY ONE SELECT INPUT



**DIP18**  
(Plastic Package)

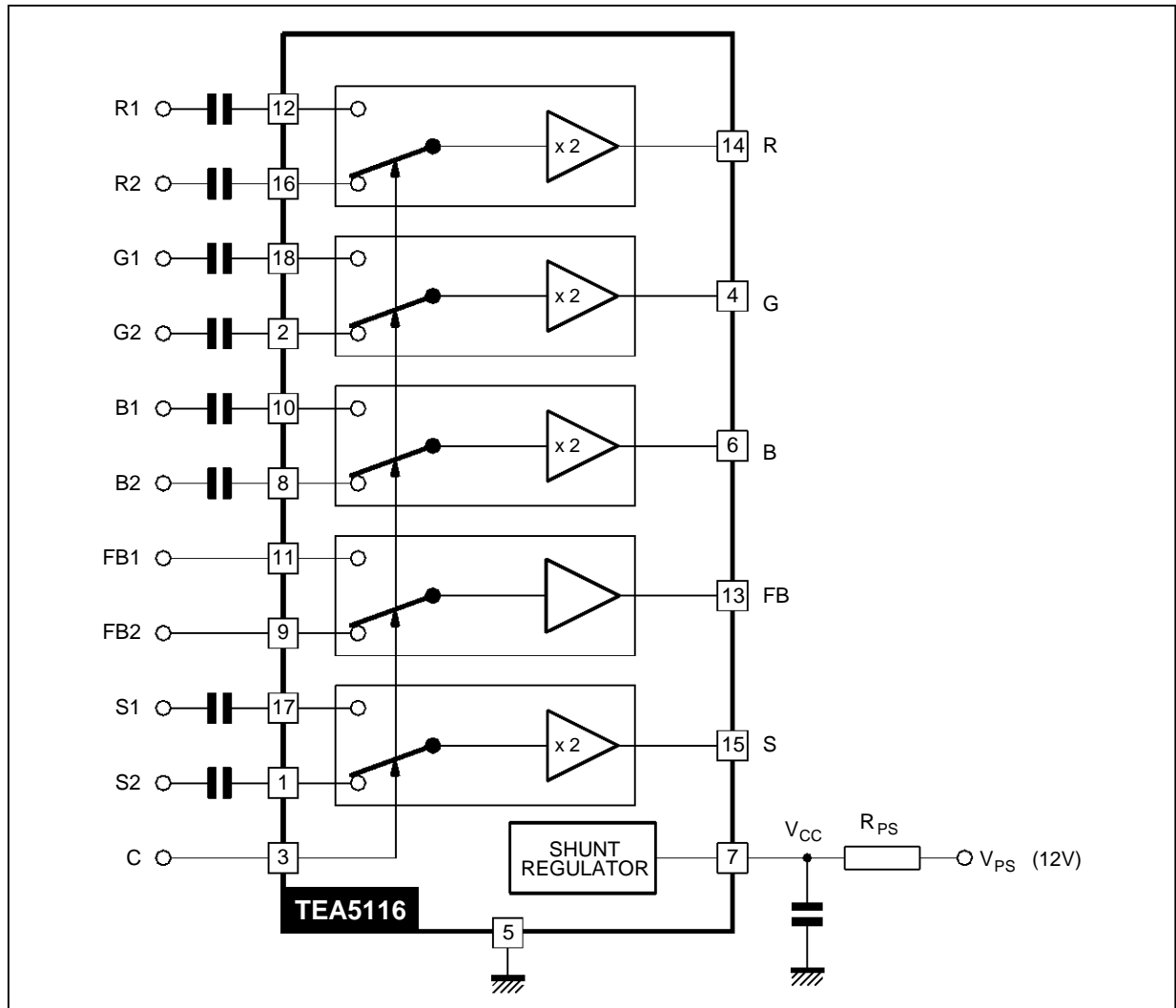
**ORDER CODE : TEA5116**

**PIN CONNECTIONS**



5116-01.EPS

**BLOCK DIAGRAM**



5116-02.EPS

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$I_{CC}$	Supply Current (see note)	150	mA
$V_{in}$	Input Voltage (all inputs)	- 0.5 to $V_{CC}$ + 0.5	V
$T_{oper}$	Operating Temperature Range	0, 70	°C
$T_j$	Junction Temperature	- 40, + 150	°C
$T_{stg}$	Storage Temperature	- 40, + 150	°C

Note : Minimum output load is 300  $\Omega$  in case of all outputs loaded.

5116-01.TBL

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

5116-01.TBL

**ELECTRICAL CHARACTERISTICS**

$T_{amb} = + 25\text{ }^{\circ}\text{C}$ ,  $I_{CC} = 120\text{ mA}$  ; Load value =  $150\text{ }\Omega$

(sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit	
$V_{CC}$	Internal Shunt Regulator	$I_{CC} = 120\text{ mA}$	6.3	6.7	7.2	V
		$I_{CC} = 90\text{ mA}$	6.2		7.3	V
		$I_{CC} = 150\text{ mA}$	6.2		7.3	V

**R, G, B Switches** (pins 4, 6, 14) (Time Measurement Conditions :  $\Delta$  inputs RGB =  $0.7\text{ V}_{pp}$  ; C pulse amplitude =  $3\text{ V}$ )

$V_C$	DC Output Voltage (no input voltage)	$T_{junction} = 25\text{ }^{\circ}\text{C}$ $T_{junction}$ stabilized		0.9 1.2	1.25	V
$V_{AC}$	Max Output Swing Voltage		2	4		$V_{pp}$
B	Bandwidth ( $-3\text{ dB}$ ) (input voltage $0.7\text{ V}_{pp}$ )		20	30		MHz
$A_v$	Gain of Each Channel (input voltage $0.7\text{ V}_{pp}$ ; $f = 1\text{ MHz}$ )		5.5	6	6.5	dB
$A_{dc}$	Gain Difference between any two R, G, B Channels (input voltage $0.7\text{ V}_{pp}$ ; $f = 1\text{ MHz}$ )			0.1	0.5	dB
	Input Swing			$0.7\text{ V} \pm 3\text{ dB}$		
$Z_{ic}$	DC Input Impedance			10		$\text{k}\Omega$
$Z_{oc}$	Dynamic Output Impedance (input voltage $0.7\text{ V}_{pp}$ ; $f = 1\text{ MHz}$ ) with $R_{load} = 300\Omega$			10		$\Omega$
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage $0.7\text{ V}_{pp}$ ; $f = 1\text{ MHz}$ ).		45	55		dB
	Crosstalk between any outputs (input voltage $0.7\text{ V}_{pp}$ ; $f = 1\text{ MHz}$ )		40	55		dB
$t_{dc}$	Delay time between R, G, B inputs and RGB outputs.			10		ns
$t_{sr1}$	Switching Rise Time between FB1 Input Signal and R, G, B Output Signal (input signal on RGB1)			45		ns
$t_{sf1}$	Switching Fall Time between FB1 Input Signal and R, G, B Output Signal (input signal on RGB1)			25		ns
$t_{sr2}$	Switching Rise Time between FB2 Input Signal and R, G, B Output Signal (input signal on RGB2)			55		ns
$t_{sf2}$	Switching Fall Time between FB2 Input Signal and R, G, B Output Signal (input signal on RGB2)			25		ns

**Fast Blanking Switch** (pin 13)

(time measurement conditions : FB input pulse amplitude =  $2\text{ V}$ , C pulse amplitude =  $3\text{ V}$ )

$V_{IL}$	Low Level Input Voltage	$T_{junction} = 25\text{ }^{\circ}\text{C}$ $T_{junction}$ stabilized	-0.5		0.4	V
$V_{IH}$	High Level Input Voltage		1		$V_{CC}+0.5$	V
$V_{OL}$	Low Level Output Voltage				$V_{CC}+0.5$	V
$V_{OH}$	High Level Output Voltage		1.4 1.5	1.7 1.9	3.5	V V
	Dynamic Output Impedance : with $R_{load} = 300\Omega$			10		$\Omega$
$t_{FB1r}$	Delay Rise Time between FB1 Input and FB Output			60	110	ns
$t_{FB1f}$	Delay Fall Time between FB1 Input and FB Output			40	60	ns
$t_{FB2r}$	Delay Rise Time between FB2 Input and FB Output			60		ns
$t_{FB2f}$	Delay Fall Time between FB2 input and FB Output			40		ns
$t_{SFB1r}$	Switching Rise Time between C Input and FB Output (input signal on FB1 input)			75		ns
$t_{SFB1f}$	Switching Fall Time between C Input and FB Output (input signal on FB1 input)			50		ns
$t_{SFB2r}$	Switching Rise Time between C Input and FB Output (input signal on FB2 input)			85		ns
$t_{SFB2f}$	Switching Fall Time between C Input and FB Output (input signal on FB2 input)			50		ns

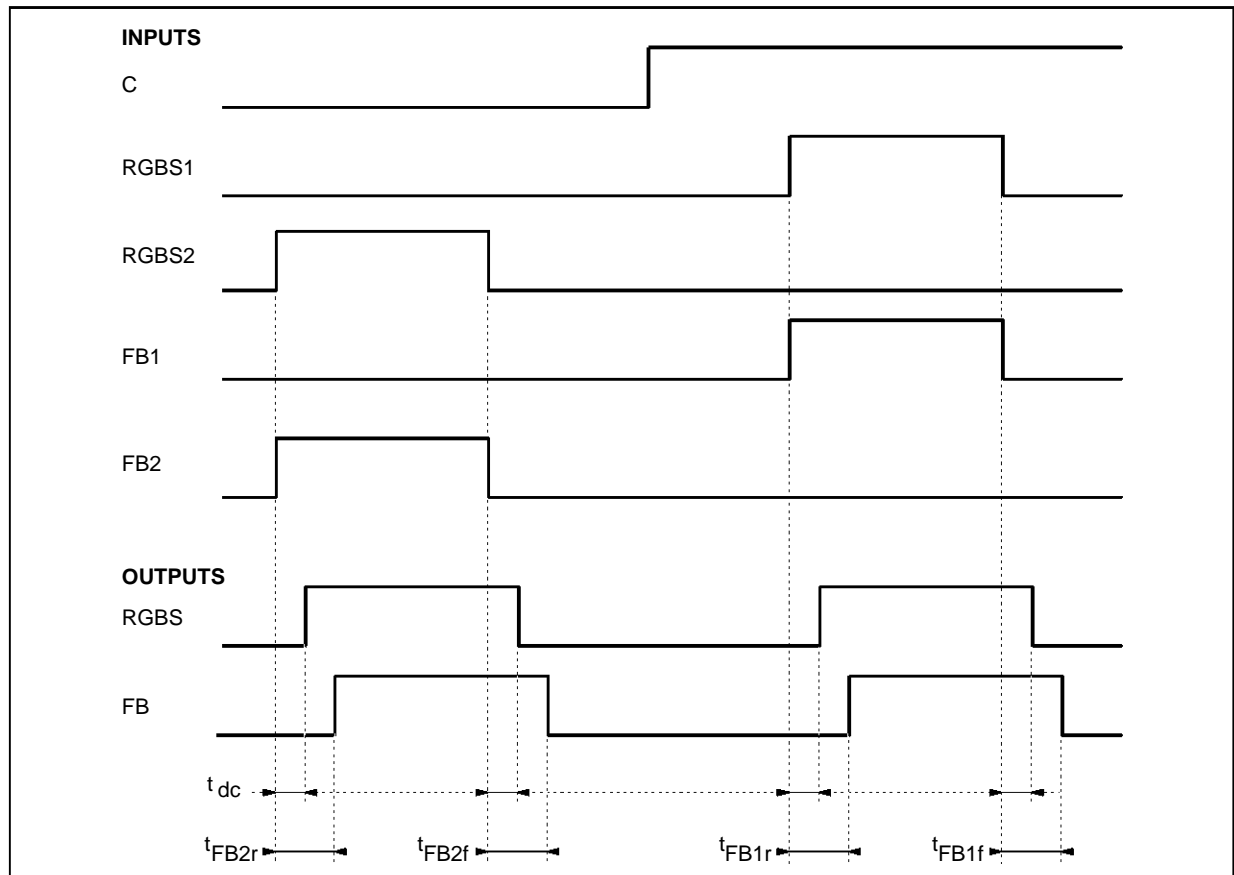
5116-03.TBL

**ELECTRICAL CHARACTERISTICS** (continued)

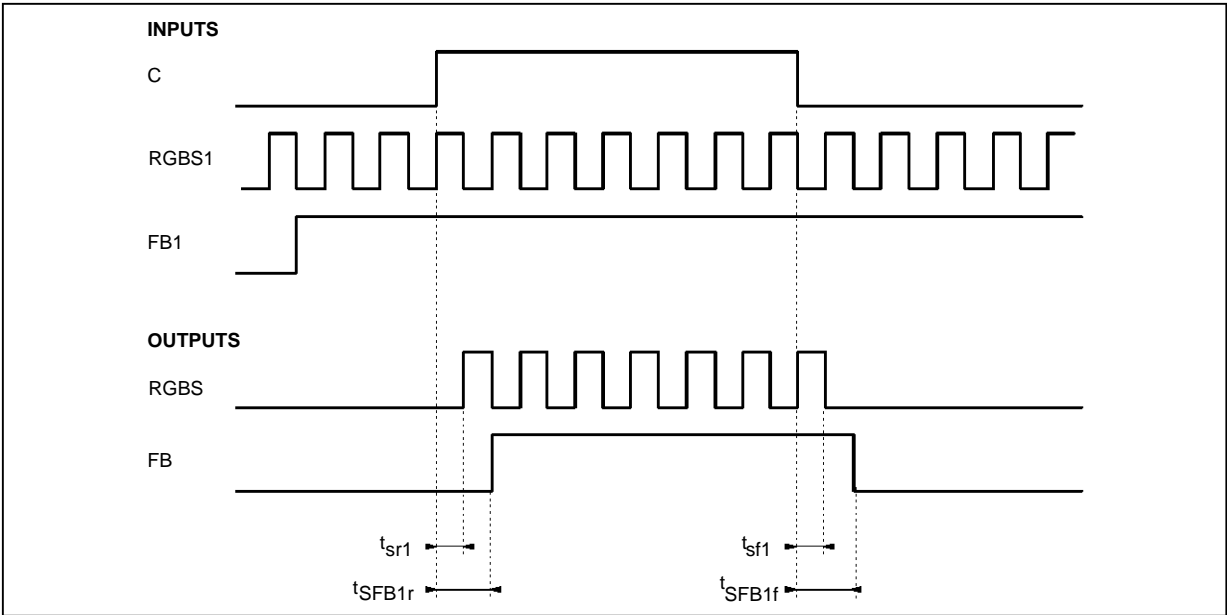
Symbol	Parameter	Min.	Typ.	Max.	Unit
<b>Video (or synchro) Signal Switch</b> (pin 15) - time measurement conditions : (C pulse amplitude = 3V)					
V <sub>S</sub>	DC Output Voltage (no input voltage)		0.9	1.25	V
V <sub>as</sub>	Max Output Swing Voltage		1.2		V
Z <sub>ic</sub>	DC Input Impedance	2.6	10		V <sub>pp</sub> kΩ
Z <sub>cc</sub>	Dynamic Output Impedance (input voltage 1V <sub>pp</sub> ; f = 1MHz) with R <sub>load</sub> = 300 Ω		10		Ω
A <sub>V</sub>	Gain (input voltage 1 V <sub>pp</sub> ; f = 1MHz)	5.5	6	6.5	dB
B	Bandwidth ( - 3 dB) (input voltage 1 V <sub>pp</sub> )	15	20		MHz
	Input Swing		1V ± 3 dB		
t <sub>dc</sub>	Delay Time between S Input and S Output (Δ input : 0.7V <sub>PP</sub> )		10		ns
t <sub>sr1</sub>	Switching rise time between C input signal and S output signal (input signal on S1)		45		ns
t <sub>sf1</sub>	Switching fall time between C input signal and S output signal (input signal on S1)		25		ns
t <sub>sr2</sub>	Switching Rise time between C input signal and S output signal (input signal on S2)		55		
t <sub>sf2</sub>	Switching fall time between C input signal and S output signal (input signal on S2)		25		

**Select Input "C"** (pin 3)

V <sub>IL</sub>	Low Level Input Voltage	- 0.5		1	V
V <sub>IH</sub>	High Level Input Voltage	2		V <sub>CC</sub> +0.5	V
I <sub>IL</sub>	Low Level Input Current (V <sub>IL</sub> = 1 V)	- 0.6		- 0.1	mA
I <sub>IH</sub>	High Level Input Current (V <sub>IH</sub> = 3 V)			0.5	mA

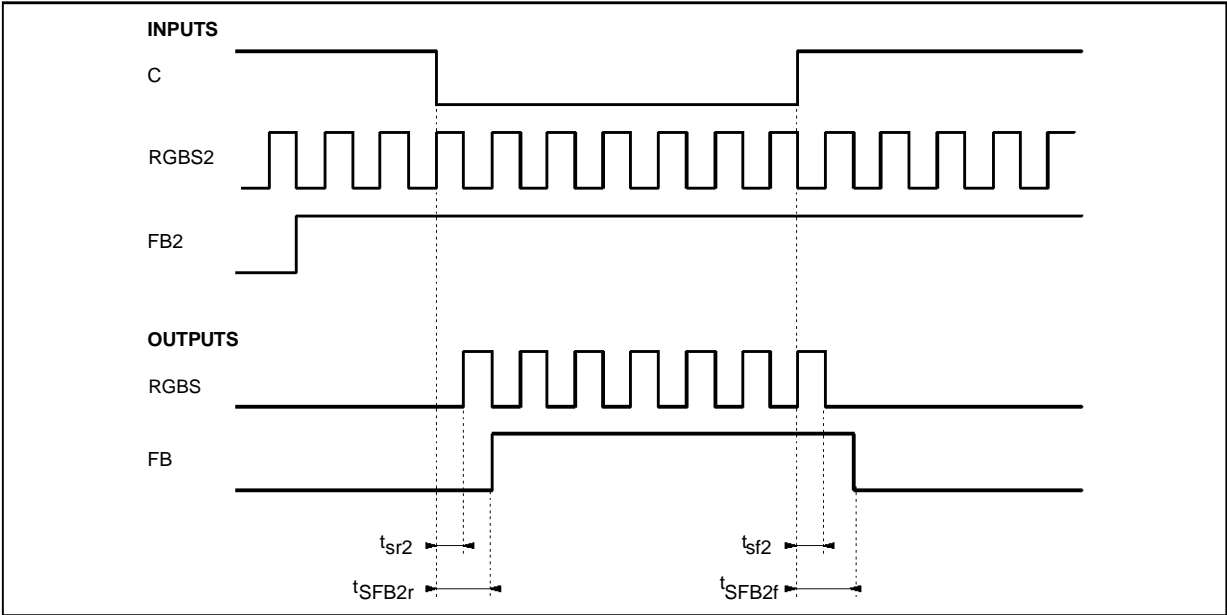


RGBS2 = 0, FB2 = 0



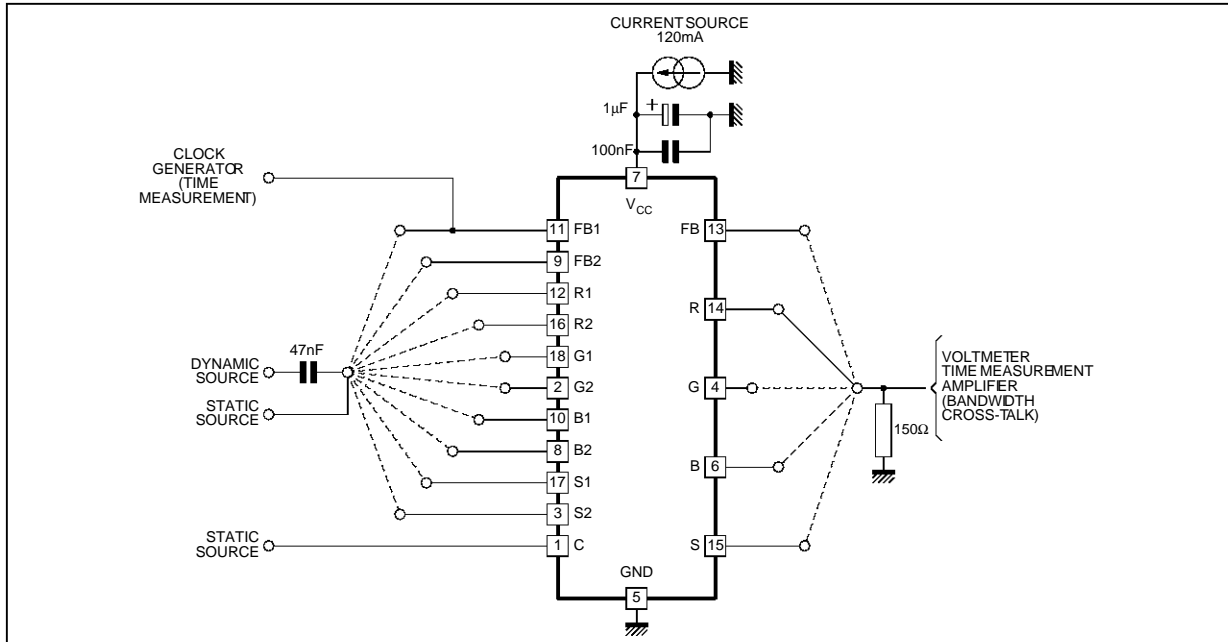
5116-04.EPS

RGBS1 = 0, FB1 = 0



5116-05.EPS

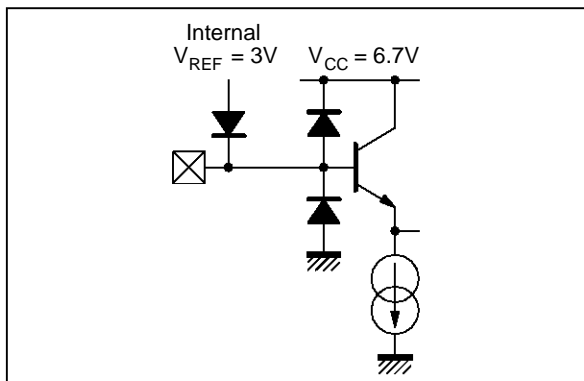
TEST CIRCUIT



5116-06.EPS

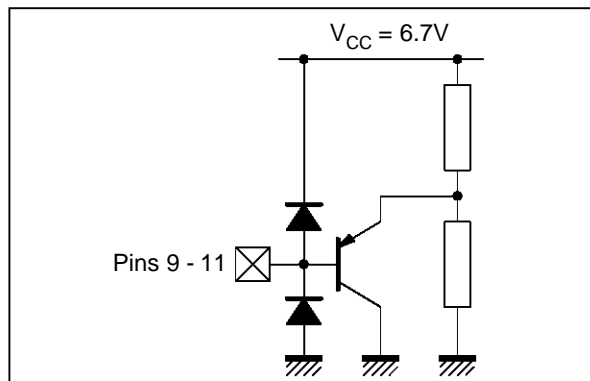
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



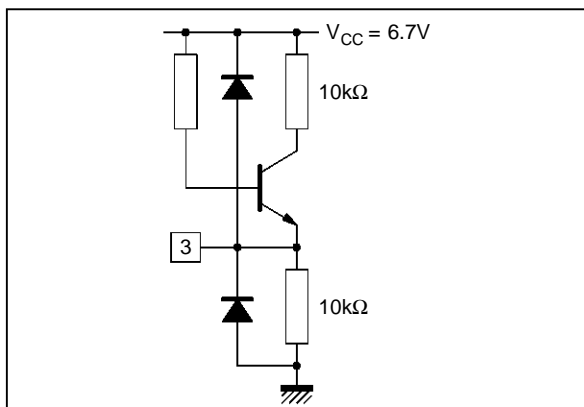
5116-07.EPS

FB inputs (pins 9, 11)



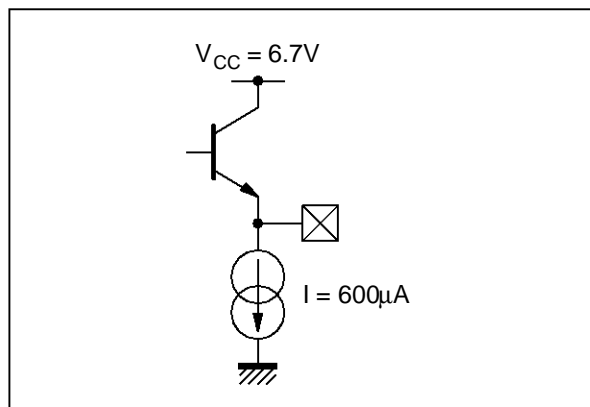
5116-08.EPS

C input (pin 3)



5116-09.EPS

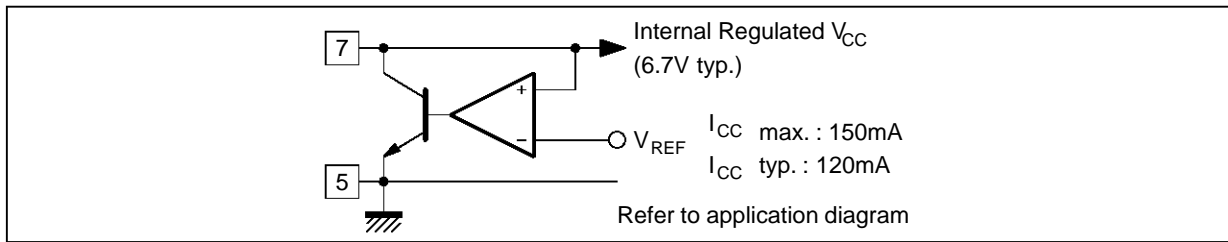
All Outputs (pins 4, 6, 13, 14, 15)



5116-10.EPS

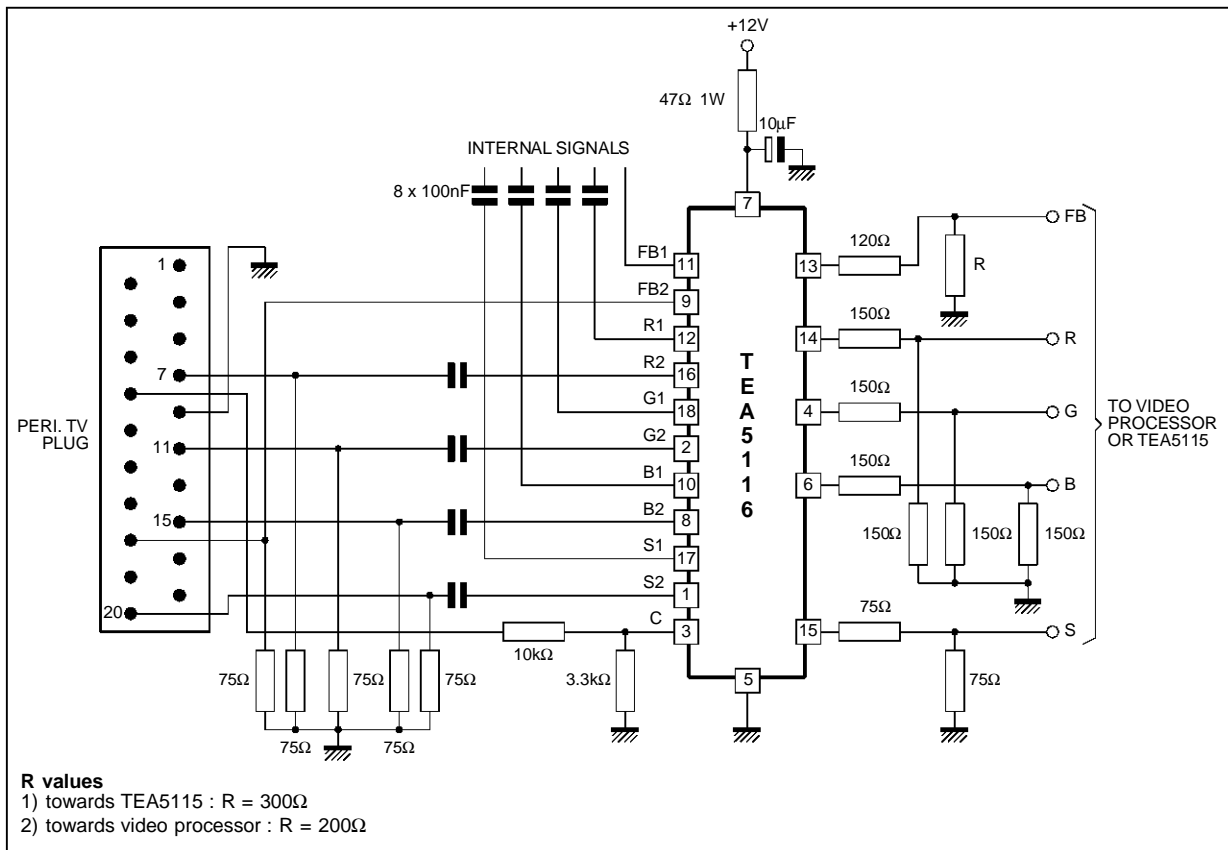
**INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)**

I<sub>CC</sub> Supply (shunt transistor regulation system) (Pin 7)



5116-11.EPS

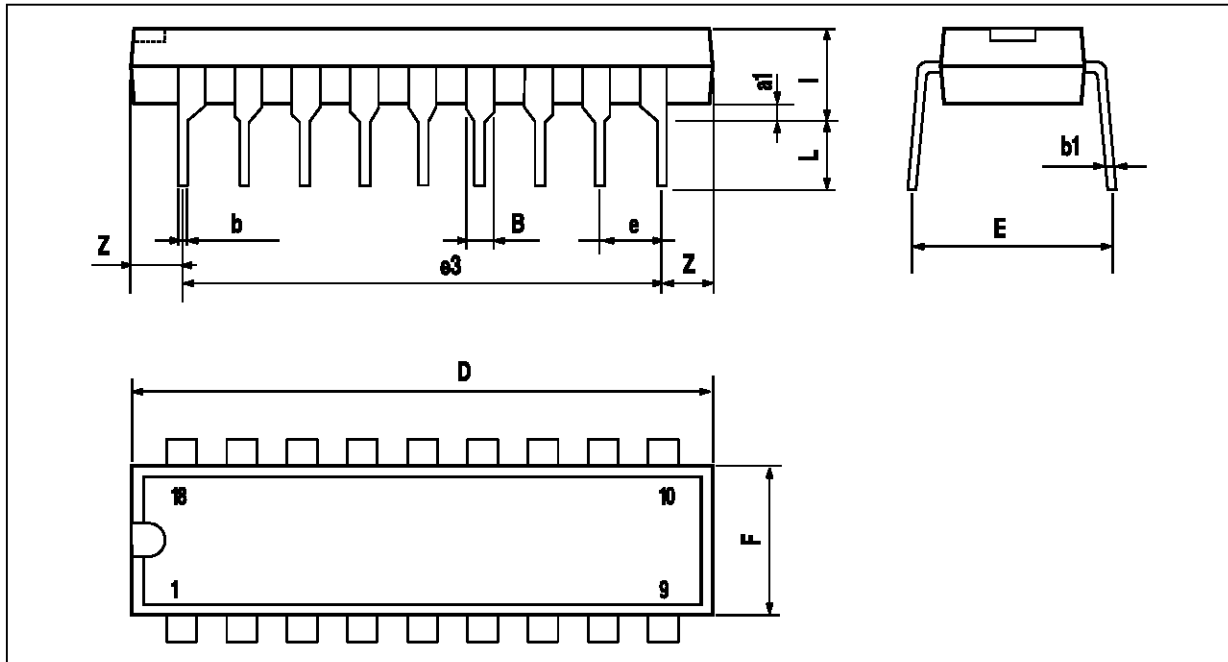
**TYPICAL APPLICATION DIAGRAM**



5116-12.EPS

- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

**PACKAGE MECHANICAL DATA**  
18 PINS – PLASTIC DIP



PM-DIP18.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.915
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
l			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.063

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