

# Si4963DY

## Dual P-Channel 2.5V Specified PowerTrench<sup>®</sup> MOSFET

### General Description

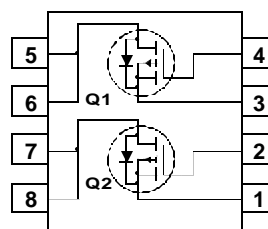
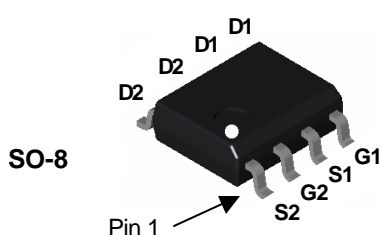
This P-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V).

### Applications

- Load switch
- Motor drive
- DC/DC conversion
- Power management

### Features

- -6.2 A, -20 V,  $R_{DS(ON)} = 33\text{ m}\Omega$  @  $V_{GS} = -4.5\text{ V}$   
 $R_{DS(ON)} = 50\text{ m}\Omega$  @  $V_{GS} = -2.5\text{ V}$
- Extended  $V_{GSS}$  range ( $\pm 12\text{V}$ ) for battery applications
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a)	-6.2	A
		-40	
$P_D$	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
4963	Si4963DY	13"	12mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_b = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_b = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-16		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = -250\ \mu\text{A}$	-0.6	-1.0	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_b = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		3		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_b = -6.2\text{ A}$ $V_{GS} = -2.5\text{ V}, I_b = -5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_b = -6.2\text{ A}$ , $T_J = 125^\circ\text{C}$		23 34 45	33 50 56	$\text{m}\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-15			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_b = -6.2\text{ A}$		19		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1456		$\text{pF}$
$C_{oss}$	Output Capacitance			300		$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance			150		$\text{pF}$

### Switching Characteristics (Note 2)

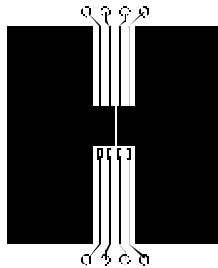
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10\text{ V}, I_b = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		15	27	ns
$t_r$	Turn–On Rise Time			11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			57	91	ns
$t_f$	Turn–Off Fall Time			37	59	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_b = -6.2\text{ A},$ $V_{GS} = -4.5\text{ V}$		14	20	nC
$Q_{gs}$	Gate–Source Charge			3		nC
$Q_{gd}$	Gate–Drain Charge			5		nC

### Drain–Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			-1.3		A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.7	-1.2	V

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C}/\text{W}$  when mounted on a  $0.5\text{ in}^2$  pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz copper



c)  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%

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