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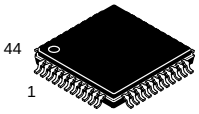
MC143416

Advance Information

Dual 16-Bit Linear Codec-Filter



PB SUFFIX
TQFP
CASE 824D

ORDERING INFORMATION

MC143416PB TQFP

The MC143416 Dual 16–Bit Linear Codec–Filter is a single–chip implementation of the data conversion interface required to design high–speed modems meeting a wide range of standards such as ITU–T V.34 and PCM modem. It includes two high performance Analog–to–Digital (A/D) and Digital–to–Analog (D/A) data converters. The device performs all filtering operations related to the conditioning and sample rate conversion of signals to and from the data interface. Output from both codecs (COder/DECoder) is in 16–bit 2s complement format.

The MC143416 includes the necessary logic needed to generate all clocks (oversampling, intermediate frequency, and baud rate) required to perform the data processing operations involved in the oversampling conversion of voice and data signals. Sample rates are fully programmable in the range of 8 kilosamples/second (ks/s) to 16 ks/s, including 8000, 9600, 11025, 12000, and 16000 samples/second. The bandwidth of the MC143416 is 0.425 * Sample Frequency (FS).

The MC143416 includes two Synchronous Serial Interfaces (SSIs) through which an external Digital Signal Processor (DSP) can configure and monitor the operation of the device. Digital sample data is transferred to and from the codecs through the serial ports. In addition, information can be written and read to the control and status registers of the device via the serial port, transparent to the flow of sample data. When used in a high–speed modem application, the MC143416 provides the analog front end interface required to support modem and voice features.

MC143416 Features

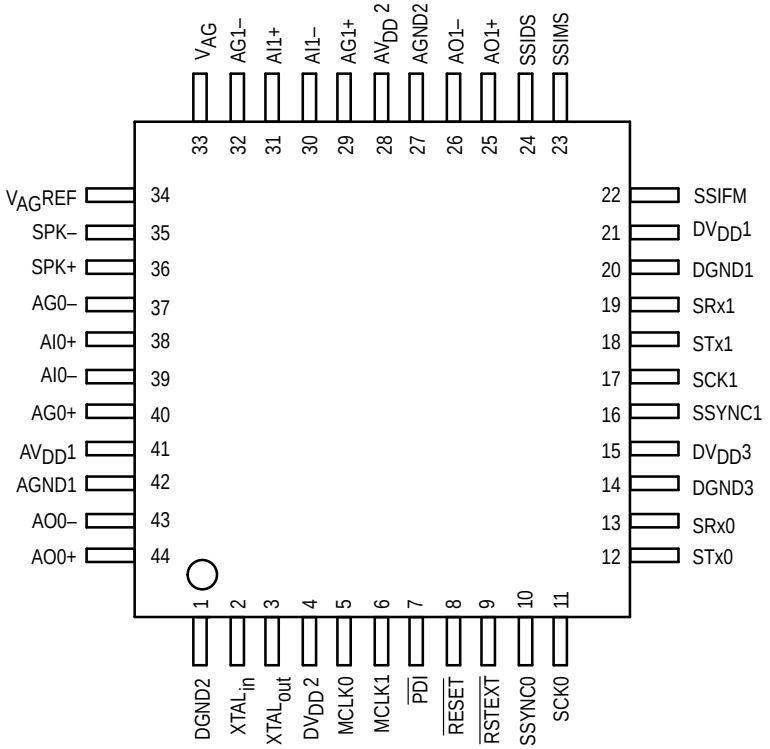
- Fully–Differential Analog Circuit Design for Lowest Noise
- Two High Performance 16–Bit Sigma–Delta A/D and D/A Converters
- Band–Pass and Low–Pass Filtering for Both Codecs is Performed On–Chip
- Power Monitor Circuit
- Single 5 V ± 5% Power Supply
- Two Configurable Serial Ports
- On–Chip Precision Reference Voltage
- On–Chip Speaker Driver and Mixer with Programmable Gain — Capable of Delivering 15 mW of Power into a Small Speaker (32 Ω)
- Bandwidth is 0.425 * FS
- No External Filtering Required Because of Flat Response Over Passband
- Capable of Providing the Analog Front End for Wide Range of Modem Standards

This document contains information on a new product. Specifications and information herein are subject to change without notice.

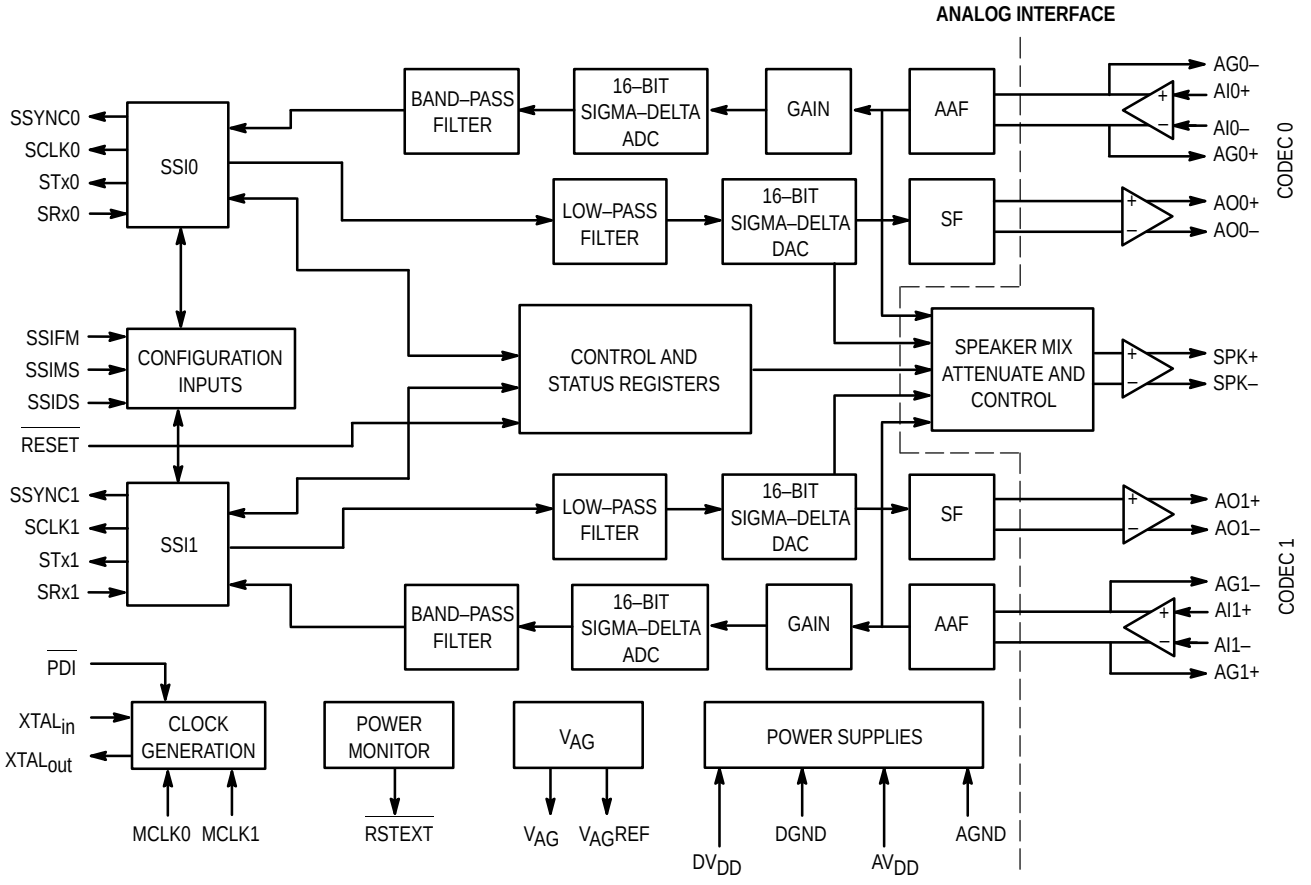
REV 2
11/97 TN97112000

MOTOROLA

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages Referenced to DGND or AGND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 6.0	V
	Voltage on Any Analog Input or Output Pin	AGND – 0.3 to V_{DD} + 0.3	V
	Voltage on Any Digital Input or Output Pin	DGND – 0.3 to V_{DD} + 0.3	V
T_A	Operating Temperature Range	– 40 to 85	°C
T_{stg}	Storage Temperature Range	– 85 to 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

POWER SUPPLY (T_A = – 40 to 85°C)

Characteristics		Min	Typ	Max	Unit
DC Supply Voltage		4.75	5.0	5.25	V
Active Current Dissipation (V_{DD} = 5 V) 2 Codecs @ 9.6 kHz and XTAL @ 21.504 MHz with OSR = 2.104 MHz	Analog Digital	— —	18 28	— —	mA
Power–Down Current (V_{IH} for Logic Levels Must be V_{DD} – 0.5 V)	Analog Digital	— —	60 60	100 100	μA

DIGITAL LEVELS (V_{DD} = 4.75 to 5.25 V, DGND = 0 V, T_A = – 40 to 85°C)

Symbol	Characteristics	Min	Max	Unit
V_{IL}	Input Low Voltage	—	0.8	V
V_{IH}	Input High Voltage	2.4	—	V
V_{OL}	Output Low Voltage (STx Pin, I_{OL}= 5 mA)	—	DGND + 0.4	V
V_{OH}	Output High Voltage (STx Pin, I_{OH} = – 5 mA)	V_{DD} – 0.4	—	V
I_L	Input Low Current (DGND ≤ V_{in} ≤ V_{DD})	– 10	10	μA
I_H	Input High Current (DGND ≤ V_{in} ≤ V_{DD})	– 10	10	μA
I_{OZ}	Output Current in High Impedance State (DGND ≤ STx0,1 ≤ V_{DD})	– 10	10	μA
C_{in}	Input Capacitance of Digital Pins	—	10	pF
C_{out}	Output Capacitance of STx0 and STx1 Pin when High–Z	—	10	pF

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 4.75 to 5.25 V, AGND = 0 V, T_A = – 40 to 85°C)

Characteristics		Min	Typ	Max	Unit
Differential Mode Input Resistance		—	65	—	kΩ
Input Current	AI+, AI–	—	± 10	—	μA
Input Resistance to V_{AG} (V_{AG} – 0.5 V ≤ V_{in} ≤ V_{AG} + 0.5 V)	AI+, AI–	10	—	—	MΩ
Input Capacitance	AI+, AI–	—	10	—	pF
Input Offset Voltage of AG Op Amp	AI+, AI–	—	20	—	mV
Input Common Mode Voltage Range	AI+, AI–	—	2.5	—	V
Input Common Mode Rejection Ratio (Input Amp Only) (Complete A/D Path)	AI+, AI– 60 Hz 0 – 4 kHz 0 – 20 kHz 60 Hz 0 – 4 kHz	 — — — — —	 120 72 68 106 75	 — — — — —	dB
Gain Bandwidth Product (10 kHz) of AG Op Amp (R_L ≥ 10 kΩ)		—	1000	—	kHz
DC Open Loop Gain of AG Op Amp (R_L ≥ 10 kΩ)		—	110	—	dB
Input Amplifier Signal to Noise + Distortion (Between AI+ and AI–, 1.5 Vrms, 0.2 – 3.4 kHz)		—	95	—	dB
Output Load Capacitance for AG Op Amp		—	—	220	pF
Output Voltage Range for AG	(R_L = 2 kΩ to V_{AG})	V_{SS} + 1	—	V_{DD} – 1	V
Output Current (0.5 V ≤ V_{out} ≤ V_{DD} – 0.5 V)	AG+, AG–	250	—	—	μA
Output Load Resistance to V_{AG}	AG+, AG–	10	—	—	kΩ
Output Current (0.5 V ≤ V_{out} ≤ V_{DD} – 0.5 V)	AO+, AO–	—	2	—	mA
Output Load Resistance to V_{AG}	AO+, AO–	1.0	1.2	—	kΩ
Differential Output Impedance Series Resistor Inductor @ 53 mA rms from 60 Hz to 100 kHz	AO+, AO– R L	 — —	 0.7 5.7	 3 10	 Ω μH
Speaker Driver Output Impedance Series Resistor Inductor @ 85 mA rms from 60 Hz to 100 kHz	SPK+, SPK– R L	 — —	 1.75 6.4	 7.0 12.0	 Ω μH
Output Load Capacitance	AO–	—	—	0.1	μF
Differential Output Offset Voltage of AO+ and AO–		—	—	20	mV
V_{AG} Output Voltage Referenced to V_{SS} (No Load)		—	$AV_{DD}/2$	—	V
V_{AG} Output Current with ± 25 mV Change in Output Voltage		—	± 44	—	mA
Power Supply Rejection Ratio (0 to 4 kHz @0.1 Vrms Applied to V_{DD})	Transmit Receive	— —	60 60	— —	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = 4.75 to 5.25 V, AGND = 0 V, All Analog Signals Referenced to V_{AG}, 0.775 Vrms = 0 dBm into 600 Ω, FSR = 8 kHz, Measurement Band = 200 to 0.425 * FS, MCLK = 2.048 MHz Synchronous Operation, T_A = – 40 to 85°C, Unless Otherwise Noted)

Characteristics	A/D			D/A			Unit
	Min	Typ	Max	Min	Typ	Max	
Dynamic Range	—	78	—	—	80	—	dB
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5.0 V)	—	– 3.8	—	—	9.0	—	dB
Total Signal to Noise + Distortion							
– 3 dBm0	—	75	—	—	75	—	dB
– 10 dBm0	—	70	—	—	71	—	
– 20 dBm0	—	60	—	—	63	—	
Idle Channel Noise (dBrn0)	—	12	—	—	13	—	dBrn0
Frequency Response (Relative to 1.02 kHz @ 0 dBm0) (HB = 0)							
60 Hz	—	– 20	—	—	± 0.15	—	dB
300 to 3000 Hz	—	0.15	—	—	± 0.15	—	
3400 Hz	—	– 0.15	—	—	– 0.10	—	
4000 Hz	—	– 35	—	—	– 20	—	
≥ 4600 Hz	—	– 70	—	—	– 32	—	
Absolute Delay (1600 Hz) (HB = 0)	—	318	—	—	214	—	µs
Group Delay Referenced to 1600 Hz (HB = 0) 500 to 600 Hz	—	96	—	—	– 26	—	µs
600 to 800 Hz	—	46	—	—	– 24	—	
800 to 1000 Hz	—	2	—	—	– 20	—	
1000 to 1600 Hz	—	0	—	—	– 18	—	
1600 to 2600 Hz	—	22	—	—	86	—	
2600 to 2800 Hz	—	189	—	—	120	—	
2800 to 3000 Hz	—	290	—	—	169	—	
Crosstalk (Within Channels) of 1020 Hz @ 0 dBm0 from A/D or D/A*	—	– 86	—	—	– 93	—	dB

* Selectively measured while stimulated with 2667 Hz @ – 50 dBm0.

Table 1. Pin Descriptions

Pin No.	Pin Name	Pin Description
1	DGND2	Digital Ground #2
2	$XTAL_{in}$	Input — Crystal Oscillator Input
3	$XTAL_{out}$	Output — Crystal Oscillator Output
4	$DV_{DD}2$	Digital Positive Power Supply #2
5	MCLK0	Input — Master Clock for Codec 0
6	MCLK1	Input — Master Clock for Codec 1
7	PDI	Input — Power Down Input
8	RESET	Input — System Reset
9	RSTEXT	Output — External Reset from Power Monitor Circuit
10	SSYNC0	Output — Serial Sync for Port 0
11	SCLK0	Output — Serial Clock for Port 0
12	STx0	Output — Serial Output for Port 0
13	SRx0	Input — Serial Input for Port 0
14	DGND3	Digital Ground #3
15	$DV_{DD}3$	Digital Positive Power Supply #3
16	SSYNC1	Output — Serial Sync for Port 1
17	SCLK1	Output — Serial Clock for Port 1
18	STx1	Output — Serial Output for Port 1
19	SRx1	Input — Serial Input for Port 1
20	DGND1	Digital Ground #1
21	$DV_{DD}1$	Digital Positive Power Supply #1
22	SSIFM	Input — SSI Framing Mode
23	SSIMS	Input — SSI Mode Select
24	SSIDS	Input — SSI Data Size
25	AO1+	Output — Codec 1 Non–Inverting Analog Output
26	AO1–	Output — Codec 1 Inverting Analog Output
27	AGND2	Analog Ground #2
28	$AV_{DD}2$	Analog Positive Power Supply #2
29	AG1+	Output — Codec 1 Input Op Amp Non–Inverting Output
30	AI1–	Input — Codec 1 Input Op Amp Inverting Input
31	AI1+	Input — Codec 1 Input Op Amp Non–Inverting Input
32	AG1–	Output — Codec 1 Input Op Amp Inverting Output
33	V_{AG}	Output — Analog Ground Voltage
34	$V_{AG}REF$	Output — Analog Ground Reference
35	SPK–	Output — Speaker Driver Inverting
36	SPK+	Output — Speaker Driver Non–Inverting
37	AG0–	Output — Codec 0 Input Op Amp Inverting Output
38	AI0+	Input — Codec 0 Input Op Amp Non–Inverting Input
39	AI0–	Input — Codec 0 Input Op Amp Inverting Input
40	AG0+	Output — Codec 0 Input Op Amp Non–Inverting Output

Continued on next page

Table 1. Pin Descriptions (continued)

Pin No.	Pin Name	Pin Description
41	$AV_{DD}1$	Analog Positive Power Supply #1
42	AGND1	Analog Ground #1
43	AO0–	Output — Codec 0 Inverting Analog Output
44	AO0+	Output — Codec 0 Non–Inverting Analog Output

PIN DESCRIPTIONS

ANALOG POWER SUPPLY

$V_{AG}REF$
Analog Ground Reference (Pin 34)

This pin is used to capacitively bypass the on–chip circuitry that generates the mid–supply voltage for the V_{AG} output pin. This pin should be bypassed to AGND with a 0.01 μF and 10 μF capacitor using short, low inductance traces. The $V_{AG}REF$ pin is only used for generating the reference voltage for the V_{AG} pin. This pin can be overridden by an external voltage source, such as a resistor divider, using two 2K resistors. No more than 100 na should be required to override this circuit. All analog signal processing within this device is referenced to the V_{AG} pin. If the audio signals to be processed are referenced to AGND, then special precautions must be utilized to avoid noise between AGND and the V_{AG} pin (such as adding coupling capacitors). When this device is in power–down mode, the $V_{AG}REF$ pin is pulled to the AV_{DD} power supply with a non–linear, high–impedance circuit.

V_{AG}
Analog Common Mode Voltage (Pin 33)

This output pin provides a mid–supply analog ground. This pin should be decoupled to AGND with a 0.01 μF ceramic capacitor. All analog signal processing within this device is referenced to this pin. If the audio signals to be processed are referenced to AGND, then special precautions must be utilized to avoid noise between AGND and the V_{AG} pin. The V_{AG} pin becomes high impedance when this device is in power–down mode.

AGND1 and AGND2
Analog Ground Pad (Pins 42 and 27, Respectively)

These pins provide the ground reference for the internal analog circuitry.

$AV_{DD}1$ and $AV_{DD}2$
Analog Supply Pad (Pins 41 and 28, Respectively)

These pins are the positive power supplies for the analog circuitry and are internally tied together.

DIGITAL POWER SUPPLY

DGND1, DGND2, and DGND3
Digital Ground Pad (Pins 20, 1, and 14, Respectively)

These pins provide the ground reference for the internal digital circuitry.

$DV_{DD}1$, $DV_{DD}2$, and $DV_{DD}3$
Digital Supply Pad (Pins 21, 4, and 15, Respectively)

These pins are the positive power supplies for the digital circuitry and are internally tied together.

CONFIGURATION INPUTS

SSIMS
Mode Select (Pin 23)

This pin selects whether the chip is operating in Dual SSI, logic 0, or in Single SSI, logic 1. In dual mode, each codec is operated from independent serial interfaces. The timing of each interface is dictated by the associated codec timing. In single serial mode, the timing of the interface is derived from the timing of the faster of the two codecs. The faster codec is defined by bit SSI_SEL in control register 4.

SSIDS
SSI Data Size (Pin 24)

When this pin is logic 0, the 24–bit word length of the SSI is enabled. When it is logic 1, the serial data format is adjusted to accommodate 16–bit word length.

SSIFM
SSI Framing Mode (Pin 22)

When this pin is logic 0, Short Frame mode is selected. This is defined as a 1–bit–wide clock pulse occurring before the first bit (MSB) of the data stream. When the pin is logic 1, Long Frame mode is selected. In long framing, the pulse rises simultaneously with the first data bit (MSB) and falls after the last data bit (LSB) has been shifted out.

SPEAKER INTERFACE

SPK+ and SPK–
Speaker Positive and Negative Signal Outputs (Pins 36 and 35, Respectively)

These pins are the outputs of the speaker driver and can deliver 15 mW of power into a small 32 Ω speaker. The external speaker can be dc–coupled to the SPK+ and SPK– pins.

CODEC INTERFACE

AI0+, AI1+, AI0–, and AI1–
Analog Inputs for Codec 0 and Codec 1 (Pins 38, 31, 39, and 30, Respectively)

These pins are the non–inverting and inverting inputs of the analog input gain setting amplifier. This fully–differential amplifier is the first stage of the A/D modulator portion of the codec. A low to moderate gain (up to 20 dB) can be obtained from this amplifier using external components. There is an internal 2 pF feedback capacitor to provide high frequency roll–off above 500 kHz.

AG0+, AG1+, AG0–, and AG1–
Outputs of Input Amplifier for Codec 0 and Codec 1
(Pins 40, 29, 37, and 32, Respectively)

These pins are the differential outputs of the input gain setting amplifiers.

AO0+, AO1+, AO0–, and AO1–
Analog Outputs for Codec 0 and Codec 1
(Pins 44 ,25, 43, and 26, Respectively)

These pins are the non–inverting and inverting outputs of the analog output amplifier. This unity gain line driver represents the final stage of the D/A section of the codec. This amplifier provides a differential output that can be dc–coupled with a hybrid circuit and is able to drive a telephone line.

SSI PORT 0 and PORT 1

SCLK0 and SCLK1
Serial Port 0 and Serial Port 1 Clock Signal Output Pins
(Pins 11 and 17, Respectively)

These pins are the timing reference for the transmission of data through the STx and SRx pins. Data transfer can only happen if the synchronization frame begins.

SSYNC0 and SSYNC1
Serial Port 0 and Serial Port 1 Sync Signal Output Pins
(Pins 10 and 16, Respectively)

These pins output the synchronization frame. The sync signal defines the beginning of each word transmitted through the STx and SRx pins.

STx0 and STx1
Serial Port 0 and Serial Port 1 Output Pins
(Pins 12 and 18, Respectively)

These pins are used to transmit data from serial ports 0 and 1. Serial transmission data is shifted on the rising edge of the serial clock (SCLK).

SRx0 and SRx1
Serial Port 0 and Serial Port 1 Input Pins
(Pins 13 and 19, Respectively)

These pins are used to receive data from serial ports 0 and 1. Serial receive data is sampled internally on the falling edge of the serial clock.

RESET

$\overline{\text{RESET}}$
System Reset Input (Pin 8)

This pin is used to force a hardware reset of the MC143416. Note: This is ineffective when the device is in general power down.

$\overline{\text{RSTEXT}}$
External Reset Output to Board Functions from Power Monitor (Pin 9)

The MC143416 provides a voltage level sensing circuit which generates an active low external reset when the power supply voltage drops below a nominal 4.5 V. The power on reset (POR) does not reset the internal circuitry, but provides an external reset signal for board use. The minimum duration of the external reset is 140 ms.

CLOCKING

$XTAL_{in}$, $XTAL_{out}$
Crystal Oscillator Input and Output
(Pins 2 and 3, Respectively)

These pins are used to provide a clock signal from a crystal oscillator. The crystal oscillator is always used for the internal logic clock timing. If the MCLK is not used for codec timing, the crystal is used (i.e., OSR, SSI, etc.). (See Figure 1 for a block diagram of the clock generation scheme.) A crystal between 20 and 30 MHz may be used. Alternatively, any external clock can be used at the $XTAL_{in}$ pin as long as the conditions found in the **Clock Generation** section are met.

MCLK0 and MCLK1
Master Clock Inputs for Codec 0 and Codec 1
(Pins 5 and 6, Respectively)

These pins are the master clock inputs for the codecs when the timing is not derived from the crystal. The master clock is equal to the oversampling clock.

$\overline{\text{PDI}}$
Absolute Power–Down Input (Pin 7)

This pin turns off any activity in the MC143416 except the power monitor function by stopping the oscillator. After any assertion of the PDI pin, a 10 ms period is required to resume functional operation. This time constraint is needed for the crystal oscillator to start up and stabilize to its defined operating point. It is mandatory to apply a hardware reset after this oscillator startup phase. Alternatively, a software reset can be applied after this startup phase and after making sure the serial interface framing logic has synced up to the host control/data frame.

FUNCTIONAL DESCRIPTION

CLOCK GENERATION

Introduction

The clock generation block generates all timing signals necessary for the operation of the device from a crystal input or alternatively from the oversampling clock (OSR CLK) supplied through the MCLK input. The selection between these two modes is controlled by the MCLK_SEL register.

The clock generation block generates the oversampling clocks, the intermediate sampling clock (for internal use), and the clocking signals for the SSI ports. The ratio of the oversampling clock to the sampling clock defines the decimation/interpolation rate. When the MCLK input is used, this clock is the OSR clock. The bit clock for the Synchronous Serial Interfaces (SSIs) is equal to the oversampling clock frequency.

Note that the MCLK and $XTAL_{in}$ frequency need to be integer multiples of the codecs' sampling rates.

Oversampling Clock Selection

The practical maximum and minimum oversampling ratio at which the device will operate is determined by the hardware implementation. At all times, the following six conditions need to be met for proper operation:

- Second order sigma–delta modulation is performed and the oversampling ratio has to be kept in the range of 102 to 254 (LSDIV values 51 to 127).
- Oversampling frequency has to be kept below 4 MHz.
- The ratio of the oversampling clock to the system clock should be greater than or equal to 7 when the oversampling clock is derived from the crystal input, and greater than or equal to 8 when derived from the MCLK input.
- The system clock should provide a minimum of 580 cycles per sampling period per codec. For example, the Fmin value of two codecs running at 8 ks/s would be:

  Fmin = FS * 580 * 2 = 8000 * 580 * 2 = 9.28 MHz

- Crystal frequency must not exceed 30 MHz.
- The maximum operating system clock frequency is 30 MHz.

Clock Generation and Divide Ratios

The functional block diagram is shown in Figure 1.

HSDIV and LSDIV Ratios. The clock generation block contains separate programmable divisors for each codec. The relationship of $XTAL_{in}$ frequency, the dividers, and the sampling frequency (FS) is:

$$XTAL_{in} = 2 * FS * (HSDIV * LSDIV)$$

where HSDIV = 7, 8, ..., 63, and LSDIV = 51, ..., 127.

When the signal is a MCLK input only, the LSDIV value applies; the HSDIV setting is a don't care. Higher settings will positively impact (reduce) power consumption.

Table 2 and Table 3 provide examples of the divisor values to derive the OSR and FS from a 28.224 MHz crystal and a 21.504 MHz crystal, respectively.

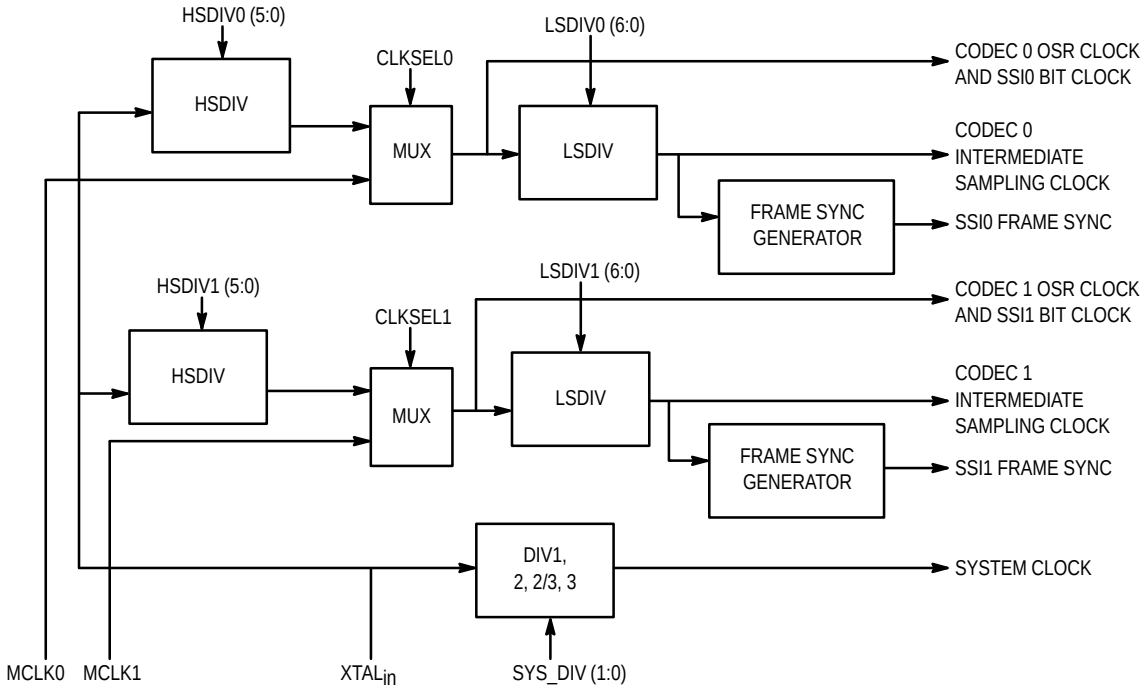


Figure 1. Block Diagram of the Clock Generation Scheme

Table 2. Suggested Sample Rate Table with a 28.224 MHz Crystal

FS (Hz)	LSDIV	HSDIV	OSR = 2X LSDIV	FOSR (MHz)
8000	126	14	252	2.016
9600	105	14	210	2.016
11025	80	16	160	1.764
12000	98	12	196	2.352
16000	126	7	252	4.032

Table 3. Suggested Sample Rate Table with a 21.504 MHz Crystal

FS (Hz)	LSDIV	HSDIV	OSR = 2X LSDIV	FOSR (MHz)
8000	112	12	224	1.792
9600	112	10	224	2.104
11025	Integer Ratio From Crystal Not Possible			
12000	64	14	128	1.536
16000	96	7	192	3.072

NOTES:

1. FS ─ desired sample rate.
2. LSDIV and HSDIV are the values loaded into the control registers in decimal format.
3. Values shown try to maximize oversampling rate.

System Divide Ratios. The system clock frequency has to be set to a minimum of seven times the oversampling frequency of the codec running the maximum OSR. This is accomplished when clocking is derived from the crystal when the HSDIV0 and HSDIV1 values are set to 7 or more. When clocking is derived from MCLK0 and/or MCLK1, a minimum ratio of 8 has to be guaranteed between any MCLK and the $XTAL_{in}$ frequency.

REGISTER PROGRAMMING

REGISTER PROGRAMMING MODEL

Table 4 is the register map of the MC143416's control and status registers. Registers labeled with a 0 suffix are associated with SSI Port 0, and those with a 1 suffix are associated with SSI Port 1. For example, register CNTL0_0 is associated with SSI Port 0, and CNTL0_1 is associated with SSI Port 1.

CONTROL AND STATUS REGISTERS

The MC143416 provides ten 8–bit control/status registers that are available to use. The MSB of all these registers is always 0 as a safety feature against desynchronization (address/data swap). Each register is doubled to serve one associated codec, with the exception of register CNTL4, CNTL5, CNTL6, and CNTL7, which carry global chip controls. These registers are accessible by either SSI port.

In the following paragraphs, the contents of each register are discussed in detail. In the description of each individual bit, two parameters are included: access and reset value. Access indicates whether the bit is read only, write only, or both; reset value indicates the value upon reset. All register bits are static except SWRESET in CNTL4.

CNTL0_0: Power Control Register — Codec 0

ANARSVD0 (R/W, 0): This bit is reserved for future use and must be kept 0.

ALOOP (R/W, 0): This bit controls the remote loopback function at the analog/digital interface. Setting this bit to 1 will force the single bit modulated output from Rx in the codec to loopback into the single bit input of the D/A. See Figure 2.

DLOOP (R/W, 0): Setting this bit to 1 will force a digital loopback in the codec. This occurs at a point between the output of digital interpolator filter and the input of the digital decimator filter. See Figure 2.

RST (R/W, 1): Setting this bit to 1 will force a value of 0x00 to all digital processing stages.

PWDN (R/W, 1): Setting this bit to 1 will disable all data processing for this codec and power down the associated analog circuitry.

TxEN (R/W, 0): Setting this bit to 1 will enable the transmitter on the codec. The transmitter is a differential mode power stage. When disabled, the amplifier maintains a zero differential output voltage (AO0+ = AO0– = V_{AG}).

ALOCAL LOOP (R/W, 0): As opposed to the ALOOP bit of this register, ALOCAL LOOP closes a local loopback at the analog interface. When this bit is set active (1), the analog output signal on pins AO0+ and AO0– is fed back into the input amplifier stage on pins AI0+ and AI0–. See Figure 2.

Table 4. Register Map

Register	Addr	7	6	5	4	3	2	1	0	Mode
CNTL0_0	0x0	0	ANARSVD0	ALOOP0	DLOOP0	PWDN0	RST0	TxEN0	ALOCAL LOOP	R/W
CNTL0_1	0x1	0	ANARSVD1	ALOOP1	DLOOP1	PWDN1	RST1	TxEN1	ALOCAL LOOP	R/W
CNTL1_0	0x2	0	HPF_EN0	IN_GAIN0(1:0)		SPK_Rx0(1:0)		SPK_Tx0(1:0)		R/W
CNTL1_1	0x3	0	HPF_EN1	IN_GAIN1(1:0)		SPK_Rx1(1:0)		SPK_Tx1(1:0)		R/W
CNTL2_0	0x4	0	MCLK0_SEL	HSDIV0(5:0)						R/W
CNTL2_1	0x5	0	MCLK1_SEL	HSDIV1(5:0)						R/W
CNTL3_0	0x6	0	LSDIV0(6:0)							R/W
CNTL3_1	0x7	0	LSDIV1(6:0)							R/W
CNTL4	0x8	0			SWRESET	RSVD	SSI_SEL	SYS_DIV(1:0)		R/W
CNTL5	0x9	0					SELF_CHECK (2:0)			RO
					TEST_RSVD (1:0)		SERIAL LOOP	TEST_MODE (1:0)		WO
CNTL6		0		RSVD (5:0)						WO
										RO
CNTL7		0	RSVD (6:0)							WO
										RO
SYNC	0xF	0	SEE DESCRIPTION							R/W

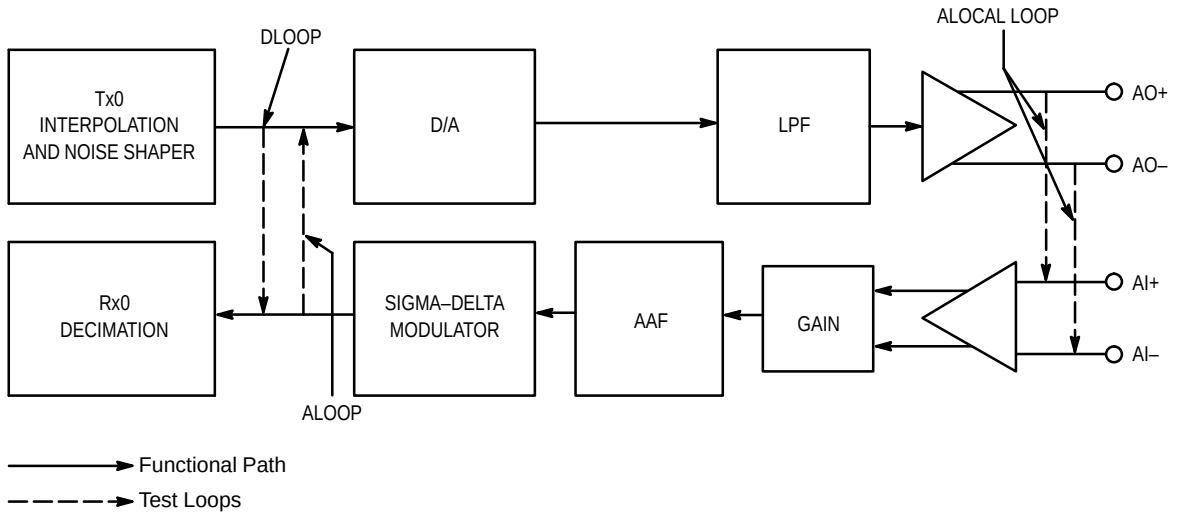


Figure 2. Digital and Analog Loopback Features

CNTL0_1: Power Control Register — Codec 1

For Codec 1, refer to **Power Control Register — Codec 0**. The power control register address for Codec 1 is 0x1. Pins AO0+, AO0–, AI0+, and AI0– for Codec 0 correspond to pins AO1+, AO1–, AI1+, and AI1– for Codec 1, respectively.

CNTL1_0: Speaker Mixer Control and Other Analog Control — Codec 0

HPF_EN (R/W, 0): This bit can be set to 1 when the codec is processing voice data. It is used to perform an additional high–pass filtering step on the voice D/A path to remove frequencies below 0.005 * FS. (40 Hz @ 8 kHz, 60 Hz @ 12 kHz, etc.)

IN_GAIN (1:0) (R/W, 0x0): These bits define a software controlled gain on the input amplifier to the codec as defined in Table 5.

Table 5. Input Signal Gain Control

IN_GAIN (1:0)	Signal Gain
00	0 dB
01	12 dB
10	24 dB
11	36 dB

SPK_Rx (1:0) and SPK_Tx (1:0) (R/W, 0x0): These register bits provide control to the analog mixer. The mixer combines four separate signal sources (AG0+, AO0+, AG1+, and AO1+, which correspond to Rx0, Tx0, Rx1, and Tx1) and provides a selection of four different amplification levels. The combined and amplified signal is then fed into the speaker driver. Two of these signal sources are from Codec 0 and the other two are from Codec 1. The signal source from the output amplifier is unaffected when the speaker driver amplifier is turned off or by the settings of these control bits.

See the **Speaker Driver and Mixer** section for more detail.

Each of the four channels (Rx0, Tx0, Rx1, and Tx1) can provide one of the four attenuation levels to the signals that source the analog mixer. Table 6 defines the levels for a given channel.

Table 6. Multiplexed Signal Gain Control

SPK_Rx (1:0), SPK_Tx (1:0)	Gain		Effect on the Signal	
	Rx	Tx	Rx	Tx
00	0	0	Disconnected	
01	1.5	0.5	3.5 dB	– 6 dB
10	3	1	9.5 dB	0 dB
11	6	2	15.6 dB	+ 6 dB

Note that it is possible to process more than one channel at the same time; this feature provides some flexibility to the user. Setting the amplification level of all the channels to zero (0x0), has the effect of powering down the speaker driver/multiplexer.

CNTL1_1: Speaker Mixer Control and Other Analog Control — Codec 1

For Codec 1, refer to **Speaker Mixer Control and Other Analog Control — Codec 0**. The speaker mixer control and other analog control register address for Codec 1 is 0x3. Pins AI0+, AI0–, AG0+, and AG0– for Codec 0 correspond to pins AI1+, AI1–, AG1+, and AG1– for Codec 1, respectively.

CNTL2_0: OSR Clock Generation Control Register — Codec 0

HSDIV (5:0) (R/W, 0x8): This field is used to program the crystal frequency divide value that will determine the frequency of the oversampling converters. See **Clock Generation** for a detailed description of the generation of clocks inside this device.

MCLK0_SEL (WO, 0): When set to 0, the clock generation block is sourced by the signal applied to $XTAL_{in}$. When set to 1, the source of the clocking for Codec 0 is defined to be MCLK0.

CNTL2_1: OSR Clock Generation Control Register — Codec 1

For Codec 1, refer to **OSR Clock Generation Control Register — Codec 0**. The OSR clock generation control register address for Codec 1 is 0x5. MCLK0 for Codec 0 corresponds to MCLK1 for Codec 1.

CNTL3_0: Sampling Clock Generation Control Register — Codec 0

LSDIV (6:0) (R/W, 0x33): This field is used to program the sampling clock divide value. See **Clock Generation** for a detailed description of the generation of clocks inside this device. The reset value of 0x33 (decimal = 51 = 0.5 min OSR) is the minimum value for this register. Any attempt to write a lower value will result in writing 0x33.

CNTL3_1: Sampling Clock Generation Control Register — Codec 1

For Codec 1, refer to **Sampling Clock Generation Control Register — Codec 0**. The sampling clock generation control register address for Codec 1 is 0x7.

CNTL4: Control Register 4

SWRESET (WO, 1): When set to 1 this bit has the same effect as a hardware reset to be applied to the chip. All control, data, and internal registers are reset, including the serial port. This bit auto resets to zero to restore functional operation.

SSI_SEL (WO, 0): This bit is used to select the timing generation path for the SSI port when running a single SSI supporting two codecs. This bit is ignored when running in dual SSI mode(SSIMS = 0). Value 0 selects timing from Codec 0, while value 1 selects timing from Codec 1. The codec running the highest rate must be selected as the SSI timing driver to guarantee enough bandwidth for data sampling.

SYS_DIV (1:0) (WO, 0x1): These bits control the operating frequency of the system clock through a programmable clock divider. The operating frequency has to be set to a minimum of eight times the oversampling frequency of the codec running the maximum OSR. Refer to **Clock Generation** for a more detailed description.

Table 7. System Clock Divider Setting

SYS_DIV (1:0)	Divide Ratio
00	1
01	2/3
10	2
11	3

CNTL5: Control Register 5

This register is primarily reserved for test purposes and should be left to its reset value, with the exception of the serial loop bit.

SELF_CHECK (2:0) (RO, 0): This field returns the results of a self test which occurs 1 ms after a hardware or software reset. Any bit other than zero indicates a failure has been detected.

TEST_MODE (1:0) (WO, 0): This bit is reserved for the test and should be kept at 0 for functional operation.

SerialLoop (WO, 0): When set to 1, this bit enables a serial loop mode. In this mode, data samples received from the serial port are retransmitted back to the serial output after a processing delay. Control and register data behavior is unchanged.

CNTL6: Control Register 6

This register is reserved and the reset value should not be changed.

CNTL7: Control Register 7

This register is reserved and the reset value should not be changed.

SYNC: Control Register F

This register is not a functional register in the sense that it is only used to guarantee/verify the framing on the serial interface. This is a mandatory requirement when running in single serial mode to make sure that control/data and sample frames are processed as such. For a more detailed description on the use of this register see **Synchronization of the Serial Ports**.

Requests for synchronization are identified as reads or writes performed to this register. This allows the internal framing hardware to “lock” on to the bit stream sent by the host.

A read to this register returns the value 0x55 when the internal state machine is synchronized to the incoming stream. It returns either 0x00 or indeterminate if the internal hardware is not properly aligned to the incoming data. The write value is ignored.

SERIAL TIMING DESCRIPTION

Synchronous Serial Interface Ports

Digital data and control information is transmitted and received through the Synchronous Serial Interface (SSI) ports. The ports and their modes of operation can be configured by hardware pins and software controls. This offers greater flexibility to accommodate different hosts, data formats, and data lengths (size).

The MC143416 uses two synchronous serial interfaces. These interfaces consist of four pins each: SCLK, STx, SRx, and SSYNC. The timing relationship of these pins can be seen in Figure 3. The output serial data is registered on the rising edge of SCLK so that each input bit can be sampled on the falling edge of SCLK. The SSIs can be operated in four different modes: 24–Bit Dual SSI, 16–Bit Dual SSI, 24–Bit Single SSI, and 16–Bit Single SSI. The primary difference between these modes is the number of frames per sampling period and the organization of the words. The serial ports can be configured through three independent pins: SSIDS (data size), SSIFM (framing mode), and SSIMS (mode select). These pins need to be permanently tied to either DGND or DV_{DD}. The pins are global controls applied on both serial ports according to Table 8.

Table 8. SSI Configuration Pins

Pin	Level	Configuration
SSIDS	0	24 Bits per Frame
	1	16 Bits per Frame
SSIMS	0	Dual Serial Mode: Each codec is operated from an independent serial interface. The timing of each interface is dictated by the associated codec timing.
	1	Single Serial Mode: Utilizes only SSI0. The timing of SSI0 is derived from the timing of the faster of the two codecs. The faster codec is defined by bit SSI_SEL in control register 4.
SSIFM	0	Short Frame Mode
	1	Long Frame Mode

Data Size — 16–Bit Mode and 24–Bit Mode: The data size can be selected by the state of the pin SSIDS. When the pin is tied low, the 24–bit data format is effective. In 24–bit operation, the control data and register data (bits 23:16) alternately precede the data sample (bits 15:0) in each frame. When this pin is set high, the serial data format is adjusted to accommodate 16–bit data. In 16–bit operation, the control data and register data are coupled in one frame, and the data sample is contained in a separate frame. The ordering of the data words depends on whether the device is in Dual SSI or Single SSI mode.

Data Mode — Dual SSI Mode and Single SSI Mode: The SSIMS pin is used to select either Dual SSI mode or Single SSI mode. When SSIMS is low, the device operates in Dual SSI mode, and when SSIMS is high, the device operates in Single SSI mode. In Dual SSI mode, each codec operates through an independent serial interface (Codec 0 operates through SSI0, and Codec 1 operates through SSI1). The timing of each serial interface is directly related to the timing of its associated codec (bit clock has the same frequency as the oversampling clock). In Single SSI mode, both codecs operate from a single SSI interface (SSI0), and the serial interface timing is dictated by the faster of the two codecs. When in this mode, the SRx1 input should be tied to ground, and the SSI1 port is not functional.

Frame Mode — Long Frame Sync Mode and Short Frame Sync Mode: This device is able to generate both long and short framing signals depending on the state of the pin SSIFM. When SSIFM is low, the device operates in Short Frame mode, which is defined as a one–bit–wide clock pulse occurring before the first bit of the data stream (MSB). When SSIFM is high, the device operates in Long Frame mode. In this mode, the framing pulse rises simultaneously with the first data bit (MSB) and falls after the last data bit (LSB) has been shifted out. The different framing modes are shown in Figure 3.

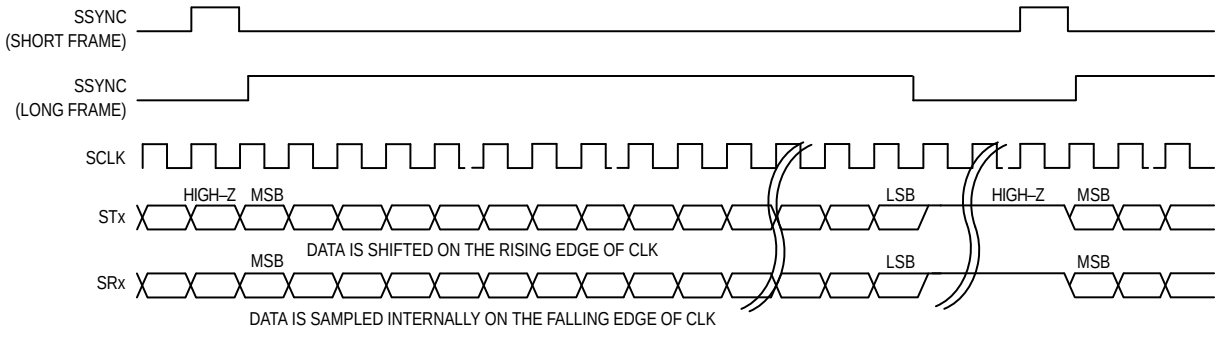


Figure 3. Serial Interface Timing

Serial Port Data Format

The serial port is used to transport three classes of data — the control word, the register data, and the data sample. The control word contains eight bits that are used for register addressing, validity, and synchronization. The register data contains eight bits, one of which is a synchronization bit. The data sample is composed of sixteen bits and contains the data to and from the codec. The serial port data format varies depending on which mode the device is operating in. Diagrams of each mode can be seen in Figures 4, 5, 6, and 7.

Figure 4 describes the data format for 24–Bit Dual SSI mode. The STx channel control field of frame ‘N’ always echoes the control field of the SRx channel with a delay equal to the repetition sequence of the framing. For 24–bit dual mode, this repetition is equal to two frames, and the sampling period is one frame. A control word issued in frame ‘N’ will be echoed in frame ‘N+2’. A data read requested through control channel at frame ‘N’ will therefore be available in frame ‘N+3’. (Note: This only applies for 24–bit dual mode.)

Figure 5 describes the data format for 16–Bit Dual SSI mode. Note that the repetition sequence and the sampling period in this mode are equal to two frames.

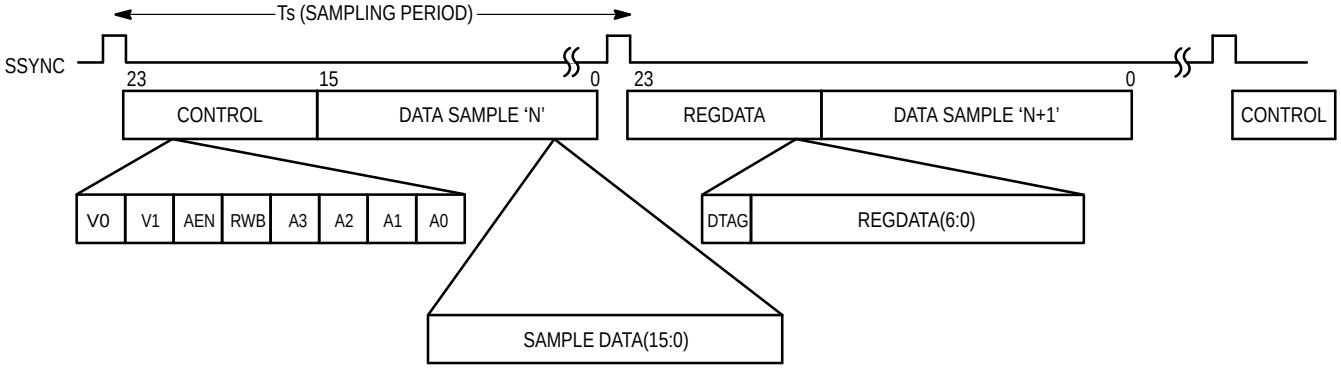


Figure 4. Dual SSI 24–Bit Format

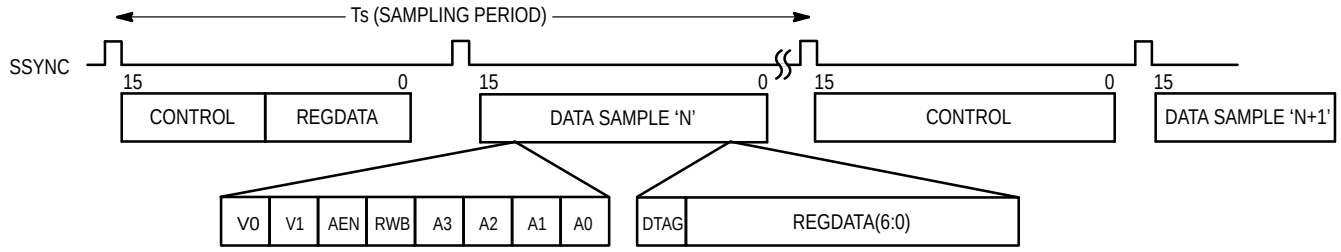


Figure 5. Dual SSI 16–Bit Format

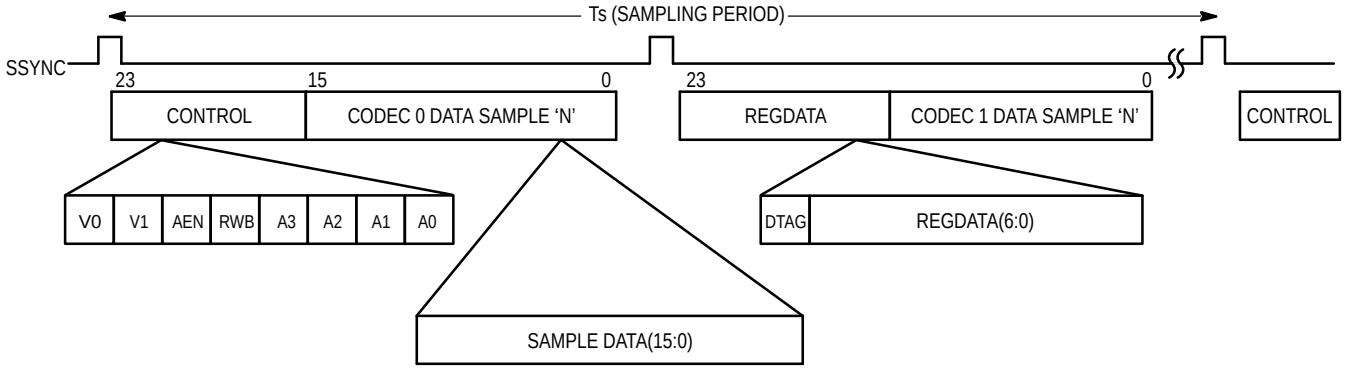


Figure 6. Single SSI 24–Bit Format

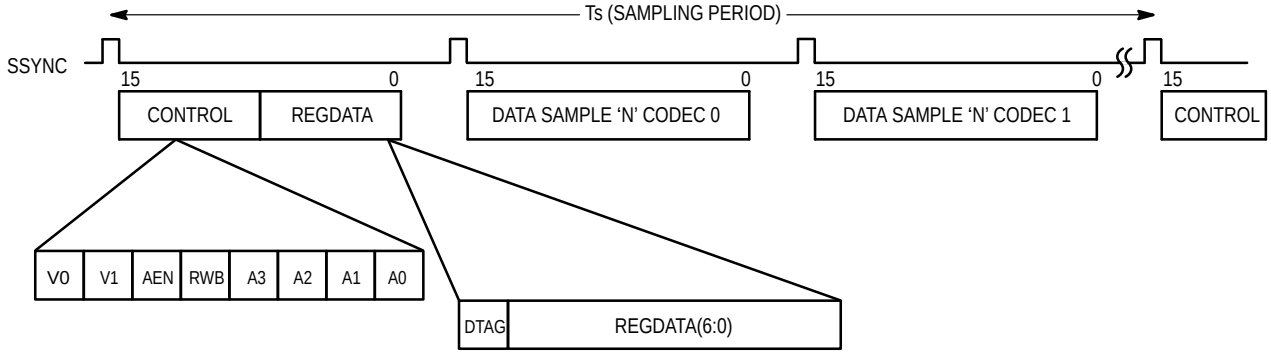


Figure 7. Single SSI 16–Bit Format

Figure 6 describes the data format for 24–Bit Single SSI mode. Note that the control word and register data alternate between frames, as well as the data for Codec 0 and Codec 1. The repetition sequence and the sampling period are equal to two frames.

Figure 7 describes the data format for 16–Bit Single SSI mode data. Note that the repetition sequence and the sampling period are equal to three frames.

Control Word

The control word consists of eight bits: V0, V1, AEN, RWB, and A(3:0). Bits V0, V1, and A0 take on slightly different meanings depending upon which mode the device is operating.

Control(7) = V0: This bit indicates the validity of the data sample following the control byte. If it is set high, the subsequent data sample is valid. If it is set low, the subsequent data sample is not valid. This bit will always read 0 when Codec 0 is powered down.

Single SSI Mode: This bit is primarily intended to support Single SSI mode with codecs operating at different rates. Since the timing for the serial interface is based on the faster codec in this mode, there will be frames when the data associated with the slower codec is not valid. During these frames, this bit will be low to indicate the data is invalid.

Dual SSI Mode: In Dual SSI mode, the sample data will always be valid as the serial interface is operating at the same rate as the associated codec.

Control(6) = V1: This bit is used either as a synchronizing bit (Dual SSI mode) or a data validity bit for Codec 1.

Single SSI Mode: In Single SSI mode, this bit acts as a validity bit for the subsequent data sample of Codec 1. The clocking is modified to generate two frames per sampling interval (three frames in 16–bit mode) and the data from both codecs is time multiplexed onto two successive syncs as described in Figures 6 and 7. The sampling interval is defined by the rate of the faster codec. This information is provided to the chip through the SSI_SEL bit in register CNTL4. The validity bit in the control field may take a logic 0 or logic 1 value depending on the operational rate of the associated codec.

Dual SSI Mode: In Dual SSI mode, this bit is always set to1 as an identifier for the control byte. If read as a 0, the device will assume desynchronization and ignore the frame. See **Synchronization of the Serial Ports** for additional information.

Control(5) = AEN (Access Enable): This bit acts like a chip select. When set to logic 0, this bit prevents access to the internal control registers. Bits 0 through 4 of the control word and associated register data are ignored.

Control(4) = RWB: This bit indicates the access mode of the register addressed by bits A(3:0). A logic 1 indicates read, and a logic 0 indicates write.

Control(3:0) = A(3:0): This is the address of the register for which access is requested. The bit A0 (LSB) is always used in Single SSI mode and conditionally used in Dual SSI mode.

Single SSI Mode: In Single SSI mode, A0 is always valid and either codec can be accessed given the proper register address.

Dual SSI Mode: In Dual SSI mode, information related to a given codec must be transmitted or received through the associated SSI port. For example, if information related to Codec 0 is required, then it must be accessed through SSI Port 0. This means that for the codec specific registers (addresses 0x0 through 0x7), the A0 bit must a zero for Codec 0, and a one for Codec 1. The other registers are global and do not apply to a specific codec, so A0 should be used as needed to access the desired register from either serial port.

Register Data

The MSB of the register data is called the 'DTAG' bit and must be set to logic 0 as a frame identifier. If read as a 1, the device will assume desynchronization and ignore the frame. See **Synchronization of the Serial Ports** for additional information. The remaining bits of this word are used to contain the register data.

Synchronization of the Serial Ports

Although serial port master, special internal hardware will slave the MC143416 framing sequence to the host processor incoming stream of data based on the known value of bits V1 (logic 1) and DTAG (logic 0). These bits alone are not enough to guarantee correct frame identification because the register value and/or the data sample may imitate the pattern created by those bits. Moreover, in Single SSI mode, only DTAG (MSB of register data) is available. The internal state machine will shift the framing identification every time the value of the above–mentioned bits are violated, thus performing a resync on the next frame. If the sample(s) imitate the control and/or the register data in Single SSI mode, locking cannot be performed securely. To protect against false locking, the host processor should perform a minimum of two accesses to the SYNC register in Single SSI 24–bit mode and three accesses in Single SSI 16–bit mode. Typically, the host will perform two write accesses to the SYNC register, followed by a read. A read value of 0x55 indicates that the internal state machine has locked on the incoming frame and full operation can begin. The internal state machine, if "unlocked", will use the register address and AEN bit as locking information. Any value other than 0x55 read from the sync register indicates the internal state machine is not ready to perform register access. Note that once synchronized, the timing of the Rx channel (MC143416 to host) is mapped onto the Tx channel (host to MC143416).

ANALOG DESCRIPTION

Codec Structure

The digital–to–analog (D/A) section is independent of the analog–to–digital (A/D) modulator section although it receives the same clocking controls. There are six package pins that externally interact with each codec. The analog section of one codec is represented in Figure 8.

The D/A takes a sampling clock and a one–bit modulated stream into a switched–capacitor low–pass filter that uses a temperature stable reference in the D/A conversion. The bandwidth for this filter is:

$$f_{3dB} = f_{OSR} / 58.74$$

Then a second order lowpass Butterworth smoothing filter follows. This filter has a cutoff frequency of 64 kHz and a Q of 1.0; the overall D/A filtering is that of a third order filter. The D/A converter ends with a unity gain line driver that is able to drive the telephone line. The complete D/A path is differential, except for the output amplifier which is pseudo–differential. This amplifier could be dc–coupled to an analog modem hybrid circuit using the transmitter pair AO+ and AO– pins.

The A/D modulator has an input amplifier that can be used to complete the hybrid circuit; a low–to–moderate gain (up to 20 dB) can be obtained from this amplifier using the four receiver stage pins: AI–, AI+, AG+, and AG–. In addition, this input amplifier is used in a stage that provides four software controlled gain steps (0, 12, 24, and 36 dB). The overall amplifier is kept with a constant unity gain frequency regardless of the particular gain settings; this helps to maintain the overall amplifier bandwidth defined by the external components attached to the AI+, AI–, AG+, and AG– pins. The input stage amplifier has an internal 2 pF feedback capacitor to provide high frequency roll–off above 500 kHz. The anti–aliasing filter (AAF) is a replica of the smoothing filter of the D/A section. It is recommended that the input amplifier portion of the application be designed with a low–pass filter with a f_{3db} of 64 kHz. This will result in an overall effect of a three–pole system. After the AAF, a second order sigma–delta modulator completes the A/D converter section. This modulator is based on a switched–capacitor approach, which uses a temperature–stable voltage reference and is able to accept a dither frequency to eliminate low frequency tone generation. The complete A/D section is fully differential.

Frequency Response

The overall bandpass width of the MC143416 is defined as 0.425 * FS, where FS is the sampling frequency. For example, at a sample rate of 8 ks/s, the bandwidth is 0.425 * 8000 = 3400 kHz. At 16 ks/s, the bandwidth increases to 0.425 * 16000 = 6800 kHz.

The high–pass filter option, which is used in voice processing to reduce dc and 60 Hz levels, is actually a notch filter with a zero at 0.005 * FS.

Speaker Driver and Multiplexer

An analog output to drive a low level speaker is provided though a four–channel mixer. Signals may come from both input (Rx) and output (Tx) paths according to Figure 9.

The output driver is able to deliver 15 mW of power into a small 32 Ω speaker for a 1.1 Vrms signal from the Tx paths (equivalent to the output level at the phone line). The circuit performs a current summation at the inputs of a differential power amplifier to emulate the action of a signal mixer. Setting the amplification level of all the channels to 0x0 has the effect of powering down the power amplifier, thus reducing software overhead.

The external speaker can be dc–coupled to the pair of pins SPK+ and SPK–, using a resistor in series to, and a bypass capacitor in parallel to, the speaker. The values of these external components are a function of the particular speaker. The capacitor is used to reduce the impedance of the speaker circuit at high frequencies one decade above the voice bandwidth. Typical values are 0.1 μF.

Note that no special hardware is included to guarantee immunity to switching noise when modifying the gain setting of the different channels.

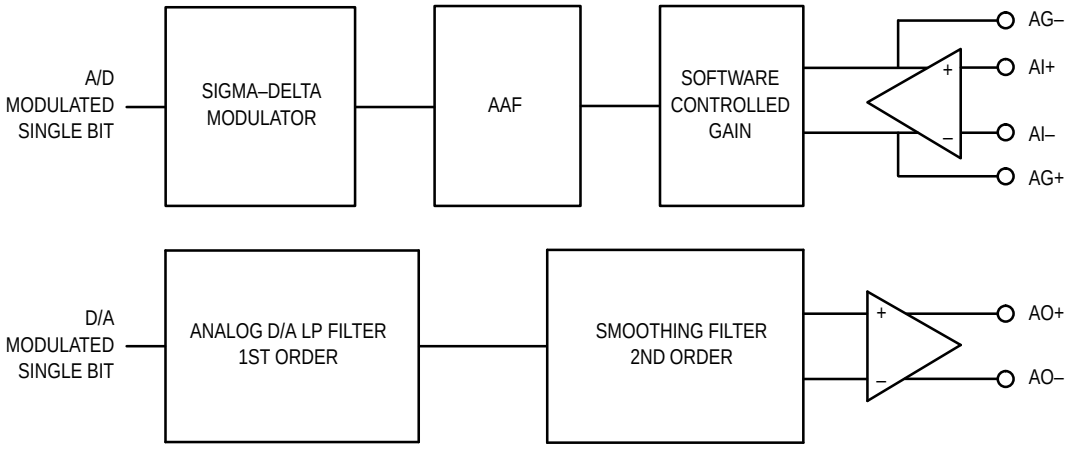


Figure 8. Codec Structure

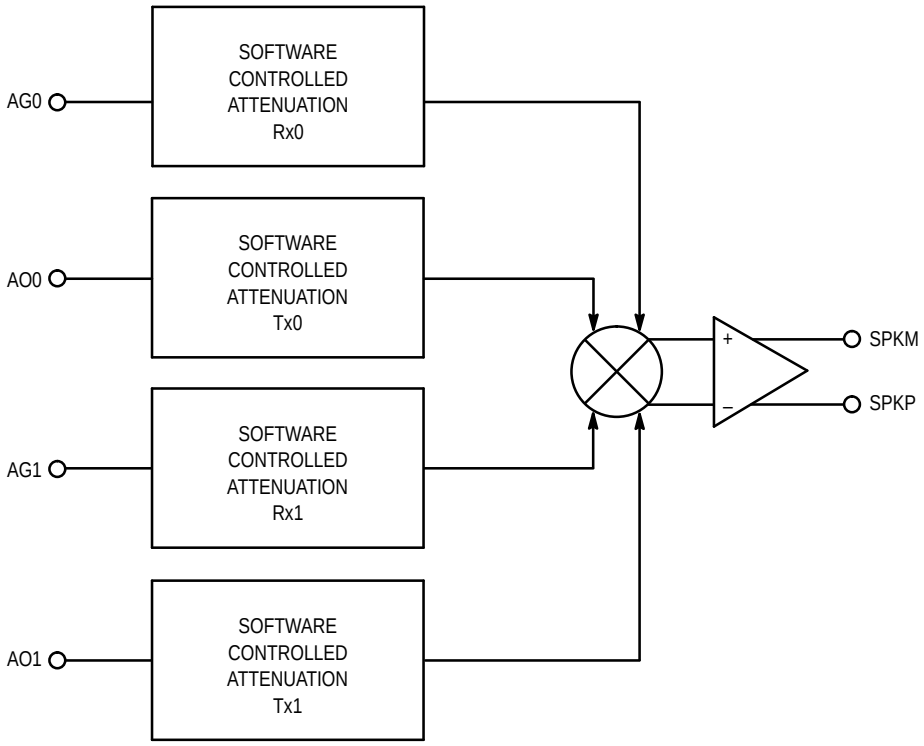


Figure 9. Speaker Mixer

LAYOUT CONSIDERATIONS

Printed Circuit Board Layout Considerations

The MC143416 is manufactured using high–speed CMOS VLSI technology to implement the complex analog signal processing functions of a PCM Codec–Filter. The fully–differential analog circuit design techniques used for this device result in superior performance for the switched capacitor filters, the analog–to–digital converter (ADC) and the digital–to–analog converter (DAC). Special attention was given to the design of this device to reduce the sensitivities of noise, including power supply rejection and susceptibility to radio frequency noise.

This device was designed for ease of implementation, but due to the large dynamic range and the noisy nature of the environment for this device (digital switches, radio telephones, DSP front–end, etc.), special care must be taken to assure optimum analog transmission performance.

PC Board Mounting

It is recommended that the device be soldered to the PC board for optimum noise performance. If the device is to be used in a socket, it should be placed in a low parasitic pin inductance (generally, low–profile) socket.

Power Supply, Ground, and Noise Considerations

This device is intended to be used in switching applications which often require plugging the PC board into a rack with power applied. This is known as “hot–rack insertion”. In these applications, care should be taken to limit the voltage on any pin from going positive of the V_{DD} pins, or negative of the GND pins. One method is to extend the ground and power contacts of the PCB connector. The device has input protection on all pins and may source or sink a limited amount of current without damage. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and cross–coupling digital or radio frequency signals into the audio signals of this device. The best way to prevent noise is to:

- Keep digital signals as far away from audio signals as possible.
- Keep radio frequency signals as far away from the audio signals as possible.
- Use short, low inductance traces for the audio circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
- Use short, low inductance traces for digital and RF circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
- Bypass capacitors should be connected from DV_{DD} to DGND, and $V_{AG}REF$ and V_{AG} to AGND with minimal trace length. Ceramic monolithic capacitors of about 0.1 μF are acceptable for the DV_{DD} and $V_{AG}REF$ pins to decouple the device from its own noise. The DV_{DD} capacitor helps supply the instantaneous currents of the digital circuitry in addition to decoupling the noise which may be generated by other sections of the device or other circuitry on the power supply. The $V_{AG}REF$ decoupling capacitor is effecting a low–pass filter to isolate the mid–supply voltage from the power supply noise generated on–chip, as well as external to the device. The V_{AG} decoupling capacitor should be about 0.01 μF. This helps to reduce the impedance of the V_{AG} pin to AGND at frequencies above the bandwidth of the V_{AG} generator, which reduces the susceptibility to RF noise.
- Use a short, wide, low inductance trace to connect the DGND ground pin to the power supply ground. The DGND pin is the digital ground and the most negative power supply pin for the analog circuitry. All analog signal processing is referenced to the V_{AG} pin, but because digital and RF circuitry will probably be powered by this same ground, care must be taken to minimize high frequency noise in the AGND trace. Depending on the application, a double–sided PCB with a ground plane connecting all of the digital and analog GND pins together would be a good grounding method. A multilayer PC board with a ground plane connecting all of the digital and analog GND pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high–speed digital current spikes. The magnitude of digitally–induced voltage spikes may be hundreds of times larger than the analog signal the device is required to digitize.
- Use a short, wide, low inductance trace to connect the V_{DD} power supply pin to the 5 V power supply. Depending on the application, a double–sided PCB with V_{DD} bypass capacitors to the ground plane, as described above, may complete the low impedance coupling for the power supply. For a multilayer PC board with a power plane, connecting all of the V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5 V V_{DD} power circuit are essentially the same as for the ground circuit.

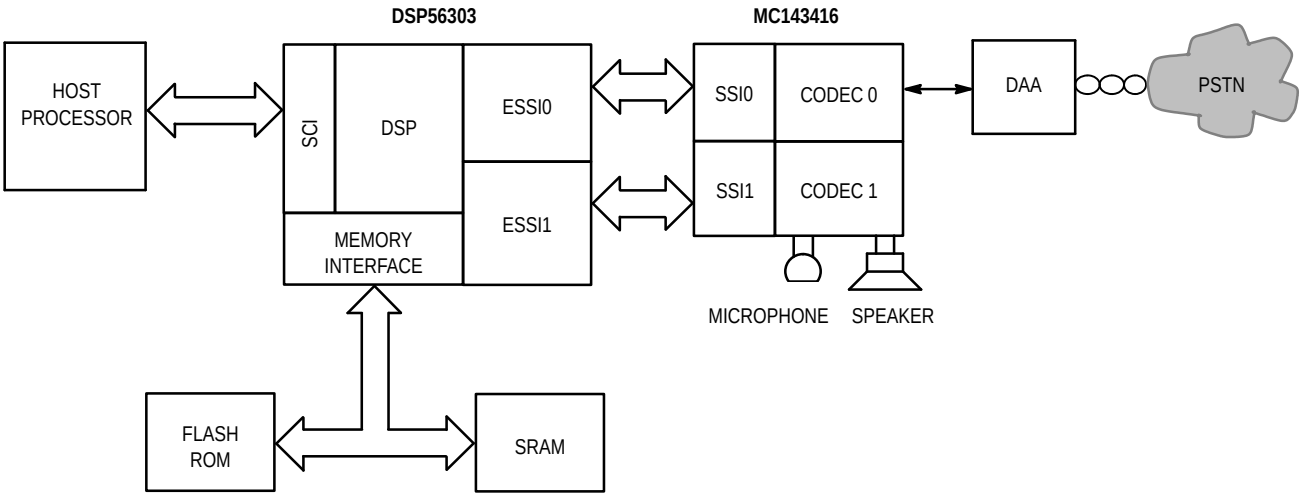
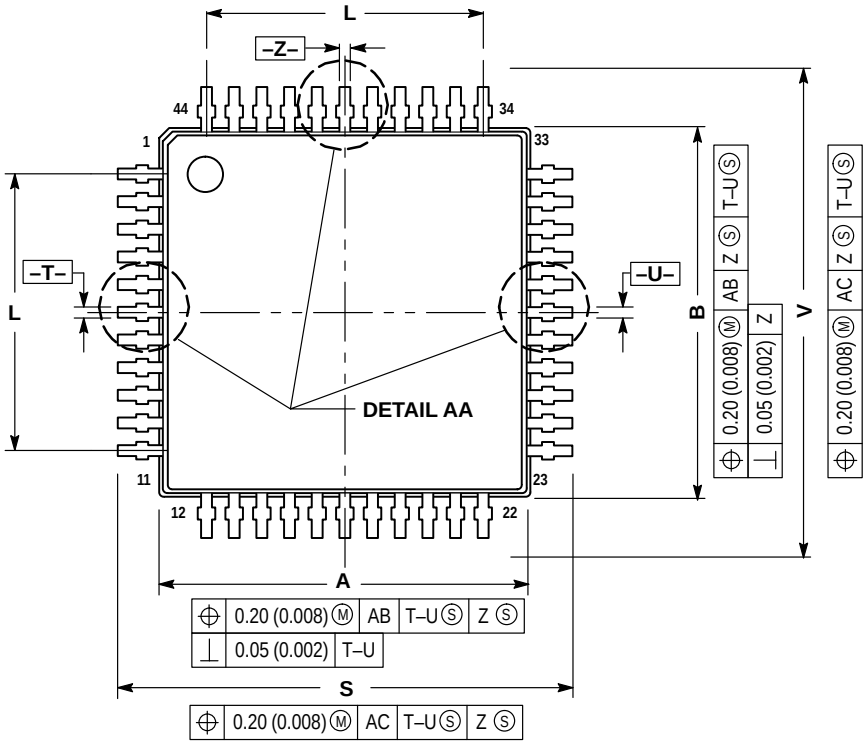
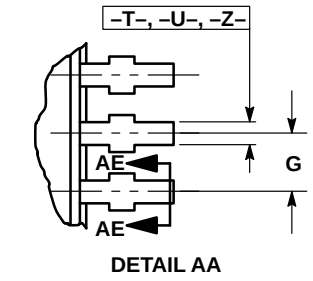


Figure 10. Active DSP–Based Modem Application

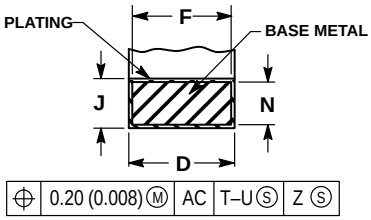
PACKAGE DIMENSIONS

PB SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 824D–01

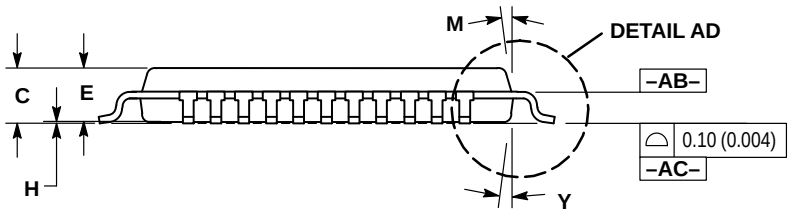


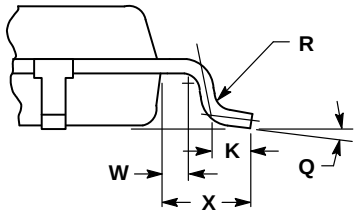


DETAIL AA



SECTION AE–AE





VIEW AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	8.000 BSC		0.315 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

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