

**MCM67A518**

**32K x 18 Bit Asynchronous/  
Latched Address Fast Static RAM**

The MCM67A518 is a 589,824 bit latched address static random access memory organized as 32,768 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates a 32K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high, the device can be used as an asynchronous SRAM. When latch enables are low, the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data-in hold time in a simple fashion.

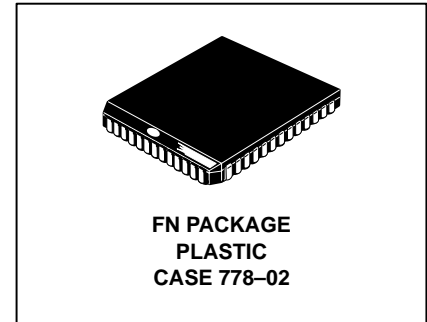
Dual write enables ( $\overline{LW}$  and  $\overline{UW}$ ) are provided to allow individually writeable bytes.  $\overline{LW}$  controls DQ0 – DQ8 (the lower bits) while  $\overline{UW}$  controls DQ9 – DQ17 (the upper bits).

Additional power supply pins have been utilized and placed on the package for maximum performance.

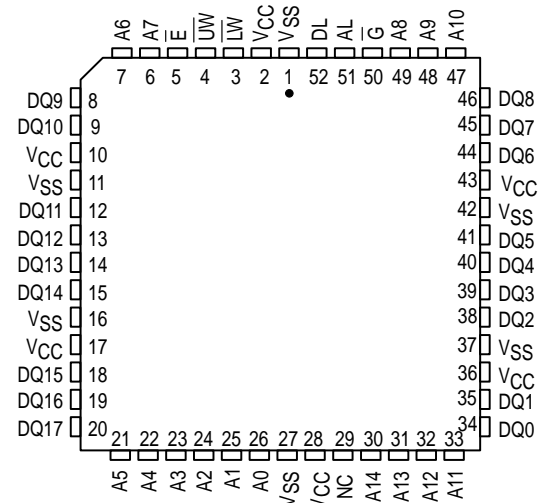
The MCM67A518 will be available in a 52-pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V  $\pm$  10% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package



**PIN ASSIGNMENT**



**PIN NAMES**

A0 – A14	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.



## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.5	V
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	$-0.5^*$	0.8	V

\*  $V_{IL}(\text{min}) = -0.5\text{ V dc}$ ;  $V_{IL}(\text{min}) = -2.0\text{ V ac}$  (pulse width  $\leq 20\text{ ns}$ ) for  $I \leq 20.0\text{ mA}$ .

\*\*  $V_{IH}(\text{max}) = V_{CC} + 0.3\text{ V dc}$ ;  $V_{IH}(\text{max}) = V_{CC} + 2.0\text{ V ac}$  (pulse width  $\leq 20\text{ ns}$ ) for  $I \leq 20.0\text{ mA}$ .

### DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0\text{ to } V_{CC}$ )	$I_{kg(I)}$	—	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $\bar{G} = V_{IH}$ )	$I_{kg(O)}$	—	$\pm 1.0$	$\mu\text{A}$
AC Supply Current ( $\bar{G} = V_{IH}$ , $I_{out} = 0\text{ mA}$ , All Inputs = $V_{IL}$ or $V_{IH}$ , $V_{IL} = 0.0\text{ V}$ and $V_{IH} \geq 3.0$ , Cycle Time $\geq t_{AVAV}$ min)	$I_{CCA10}$ $I_{CCA12}$ $I_{CCA15}$	—	290 275 260	mA
AC Standby Current ( $\bar{E} = V_{IH}$ , $I_{out} = 0\text{ mA}$ , All Inputs = $V_{IL}$ and $V_{IH}$ , $V_{IL} = 0.0\text{ V}$ and $V_{IH} \geq 3.0\text{ V}$ , $f = f_{max}$ )	$I_{SB1}$	—	75	mA
CMOS Standby Current ( $\bar{E} \geq V_{CC} - 0.2$ , All Inputs $\geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$ , $f = f_{max}$ )	$I_{SB2}$	—	30	mA
Output Low Voltage ( $I_{OL} = +8.0\text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = -4.0\text{ mA}$ )	$V_{OH}$	2.4	3.3	V

### CAPACITANCE ( $f = 1.0\text{ MHz}$ , $dV = 3.0\text{ V}$ , $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	$C_{in}$	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V      Output Timing Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V      Output Load ..... Figure 1 Unless Otherwise Noted  
 Input Rise/Fall Time ..... 3 ns

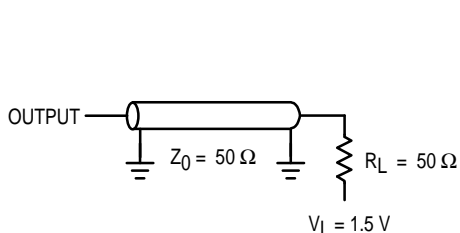
### ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A518-10		MCM67A518-12		MCM67A518-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	$t_{AVAV}$	10	—	12	—	15	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	$t_{AVQV}$	—	10	—	12	—	15		
$\bar{E}$ Low to Output Valid	$t_{ELQV}$	—	10	—	12	—	15		
Output Enable Low to Output Valid	$t_{GLQV}$	—	5	—	6	—	7		
Output Hold from Address Change	$t_{AXQX}$	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\bar{E}$ Low to Output Active	$t_{ELQX}$	3	—	3	—	2	—		
$\bar{G}$ Low to Output Active	$t_{GLQX}$	1	—	1	—	1	—		
$\bar{E}$ High to Output High-Z	$t_{EHQZ}$	2	5	2	6	2	9		
$\bar{G}$ High to Output High-Z	$t_{GHQZ}$	2	5	2	6	2	7		
Power Up Time	$t_{ELICCA}$	0	—	0	—	0	—	ns	

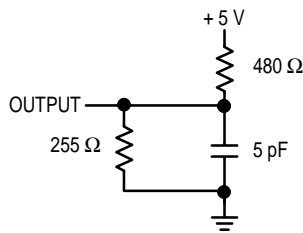
**NOTES:**

1. AL and DL are equal to  $V_{IH}$  for all asynchronous cycles.
2. Both Write Enable signals ( $\bar{LW}$ ,  $\bar{UW}$ ) are equal to  $V_{IH}$  for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with  $\bar{E}$  going low.
5. Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature,  $t_{EHQZ}$  is less than  $t_{ELQX}$  and  $t_{GHQZ}$  is less than  $t_{GLQX}$  for a given device.

### AC TEST LOADS

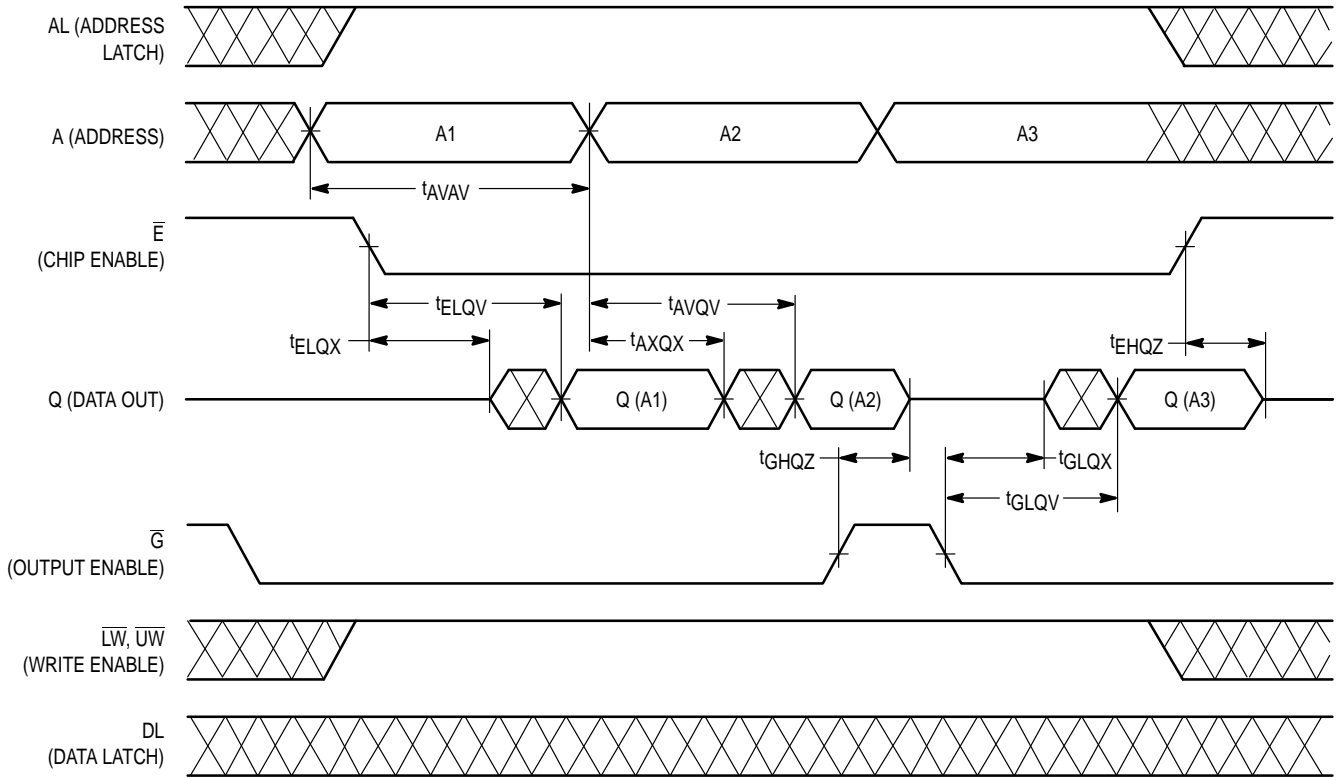


**Figure 1A**



**Figure 1B**

### ASYNCHRONOUS READ CYCLES



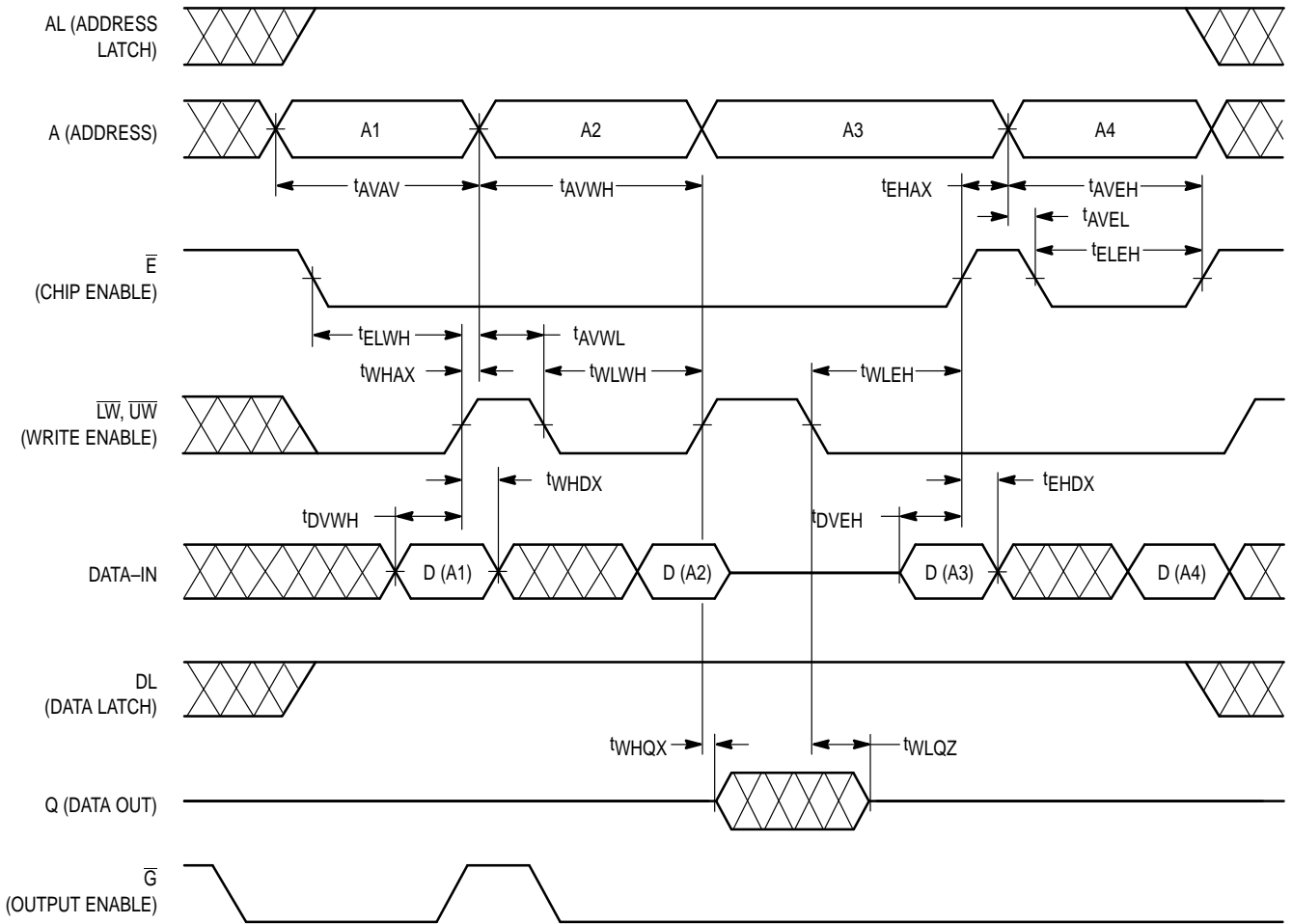
**ASYNCHRONOUS WRITE CYCLE TIMING** (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A518-10		MCM67A518-12		MCM67A518-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	$t_{AVAV}$	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	$t_{AVWH}$	9	—	10	—	13	—		
Address Valid to $\bar{E}$ High	$t_{AVEH}$	9	—	10	—	13	—		
Address Valid to $\bar{W}$ Low	$t_{AVWL}$	0	—	0	—	0	—		
Address Valid to $\bar{E}$ Low	$t_{AVEL}$	0	—	0	—	0	—		
Address Valid to $\bar{W}$ High	$t_{DVWH}$	5	—	6	—	7	—		
Data Valid $\bar{E}$ High	$t_{DVEH}$	5	—	6	—	7	—		
Hold Times:								ns	
$\bar{W}$ High to Address Invalid	$t_{WHAX}$	0	—	0	—	0	—		
$\bar{E}$ High to Address Invalid	$t_{EHAX}$	0	—	0	—	0	—		
$\bar{W}$ High to Data Invalid	$t_{WHDX}$	0	—	0	—	0	—		
$\bar{E}$ High to Data Invalid	$t_{EHDX}$	0	—	0	—	0	—		
Write Pulse Width:								ns	
Write Pulse Width ( $\bar{G}$ Low)	$t_{WLWH}$	9	—	10	—	13	—		
Write Pulse Width ( $\bar{G}$ High)	$t_{WLWH}$	8	—	9	—	12	—		
Write Pulse Width	$t_{WLEF}$	9	—	10	—	13	—		5
Enable to End of Write	$t_{ELWH}$	9	—	10	—	13	—		6
Enable to End of Write	$t_{ELEH}$	9	—	10	—	13	—		5, 6
Output Buffer Control:								ns	
$\bar{W}$ High to Output Valid	$t_{WHQV}$	10	—	12	—	15	—		
$\bar{W}$ High to Output Active	$t_{WHQX}$	3	—	3	—	5	—		7
$\bar{W}$ Low to Output High-Z	$t_{WLQZ}$	0	5	0	6	0	9		7, 8

**NOTES:**

1. W (write) refers to either one or both byte write enables  $\bar{LW}$  and  $\bar{UW}$ .
2. AL and DL are equal to  $V_{IH}$  for all asynchronous cycles.
3. Both Write Enables must be equal to  $V_{IH}$  for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high the output will remain in a high impedance state.
6. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low the output will remain in a high impedance state.
7. Transition is measured  $\pm 500$  mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested.  
At any given voltage and temperature,  $t_{WLQZ}$  is less than  $t_{WHQX}$  for a given device.
8. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low the output will remain in a high impedance state.

### ASYNCHRONOUS WRITE CYCLE



**LATCHED READ CYCLE TIMING** (See Notes 1 and 2)

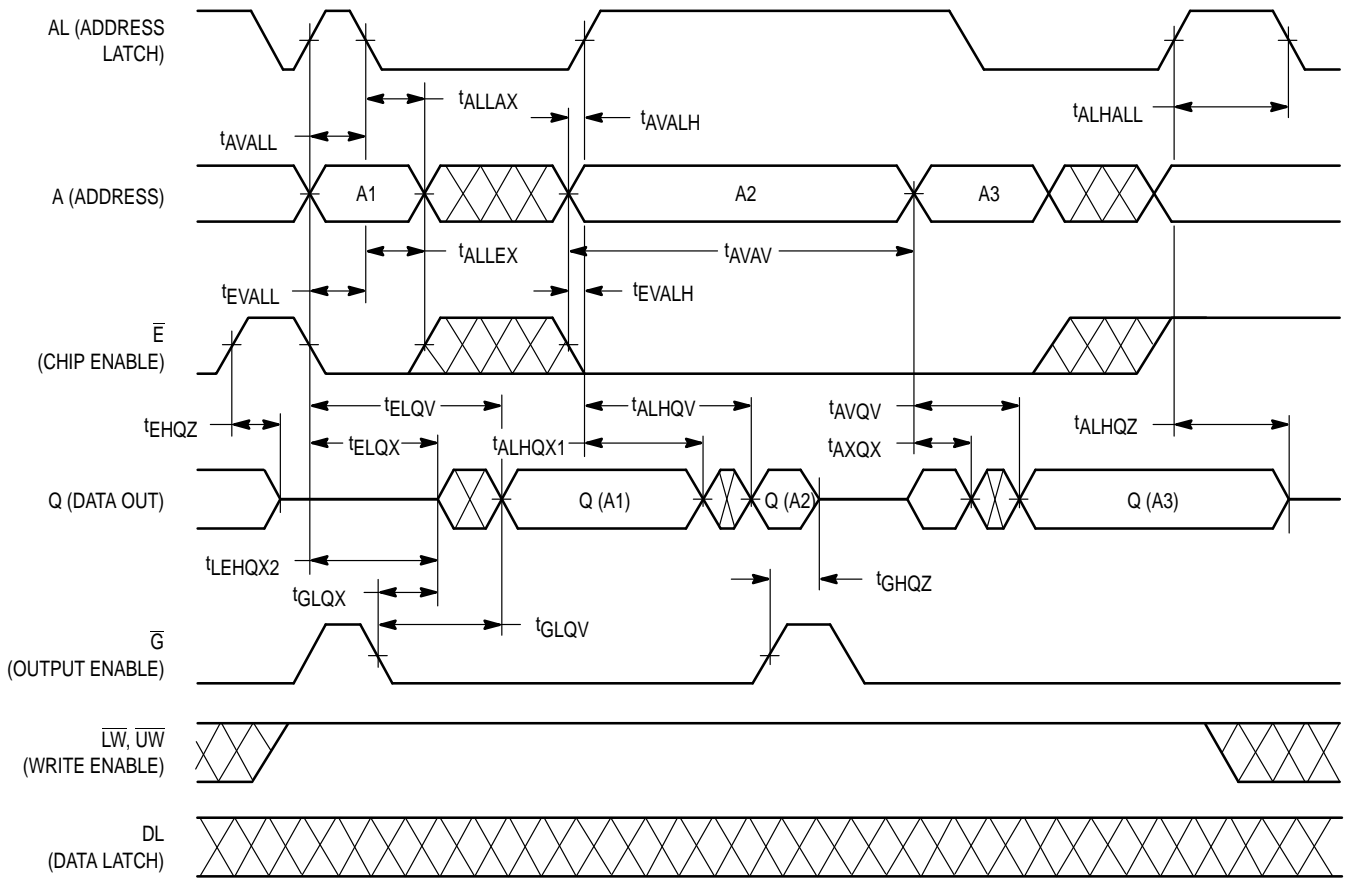
Parameter	Symbol	MCM67A518-10		MCM67A518-12		MCM67A518-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	$t_{AVAV}$	10	—	12	—	15	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	$t_{AVQV}$	—	10	—	12	—	15		3
$\bar{E}$ Low to Output Valid	$t_{ELQV}$	—	10	—	12	—	15		4
AL High to Output Valid	$t_{ALHQV}$	—	10	—	12	—	15		
Output Enable Low to Output Valid	$t_{GLQV}$	—	5	—	6	—	7		
Setup Times:								ns	
Address Valid to AL Low	$t_{AVALL}$	2	—	2	—	2	—		4
$\bar{E}$ Valid to AL Low	$t_{EVALL}$	2	—	2	—	2	—		4
Address Valid to AL High	$t_{AVALH}$	0	—	0	—	0	—		
$\bar{E}$ Valid to AL High	$t_{EVALH}$	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	$t_{ALLAX}$	2	—	2	—	3	—		
AL Low to $\bar{E}$ Invalid	$t_{ALLEX}$	2	—	2	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	$t_{AXQX}$	4	—	4	—	4	—		
AL High to Output Invalid	$t_{ALHQX1}$	4	—	4	—	4	—		
Address Latch Pulse Width	$t_{ALHALL}$	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\bar{E}$ Low to Output Active	$t_{ELQX}$	3	—	3	—	2	—		
$\bar{G}$ Low to Output Active	$t_{GLQZ}$	1	—	1	—	1	—		
AL High to Output Active	$t_{ALHQX2}$	3	—	3	—	2	—		
$\bar{E}$ High to Output High-Z	$t_{EHQZ}$	2	5	2	6	2	9		
AL High to Output High-Z	$t_{ALHQZ}$	2	5	2	6	2	9		
$\bar{G}$ High to Output High-Z	$t_{GHQZ}$	2	5	2	6	2	7		

**NOTES:**

- Both Write Enable Signals ( $\overline{LW}$ ,  $\overline{UW}$ ) are equal to  $V_{IH}$  for all read cycles.
- All read cycle timing is referenced from the last valid address to the first transitioning address.
- Addresses valid prior to or coincident with  $\bar{E}$  going low.
- All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
- Transition is measured  $\pm 500$  mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature,  $t_{EHQZ}$  is less than  $t_{ELQX}$  and  $t_{LEHQZ}$  is less than  $t_{LEHQX2}$  and  $t_{GHQZ}$  is less than  $t_{GLQX}$  for a given device.



### LATCHED READ CYCLES



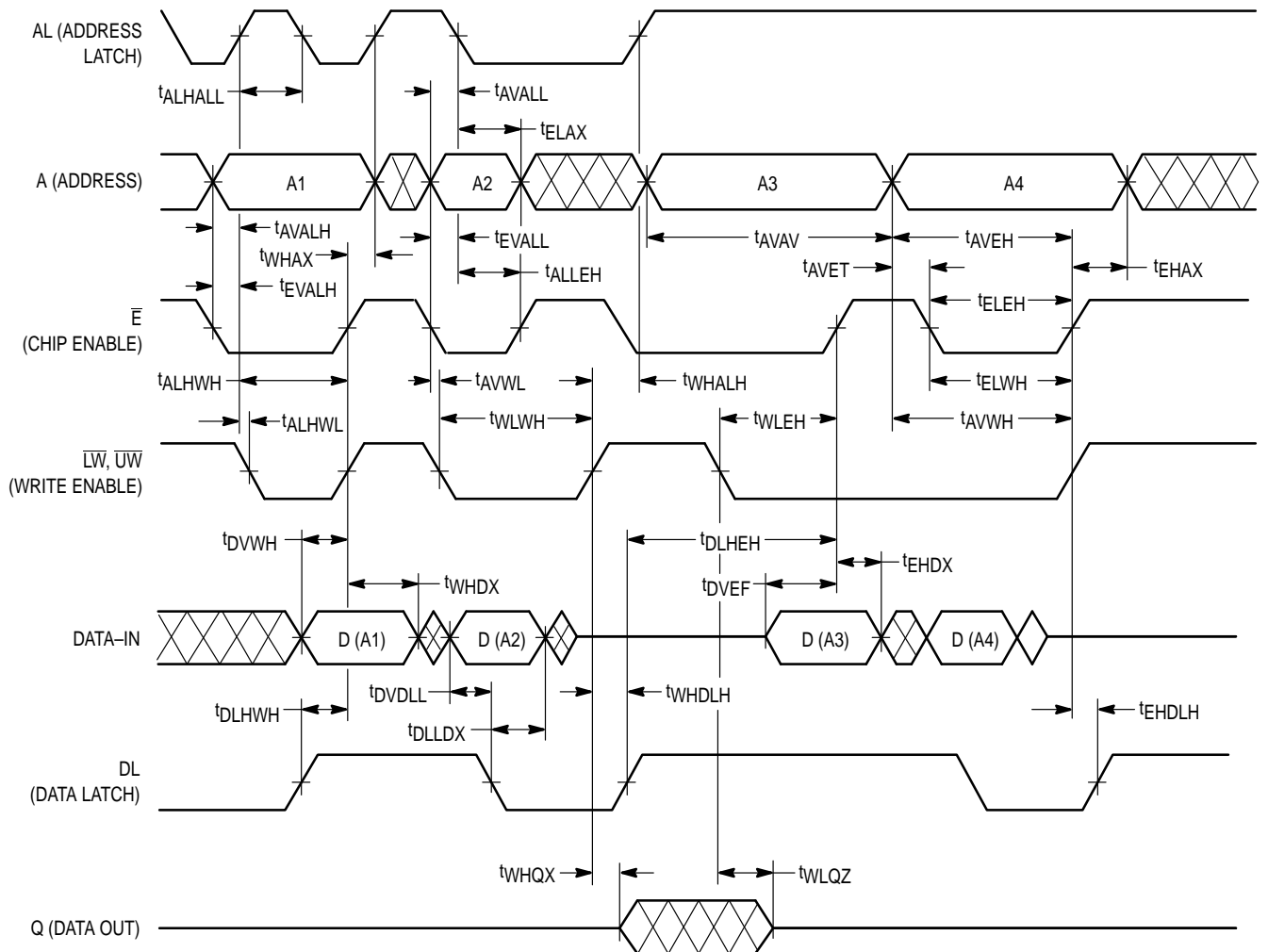
**LATCHED WRITE CYCLE TIMING** (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A518-10		MCM67A518-12		MCM67A518-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t <sub>AVAV</sub>	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t <sub>AVWH</sub>	9	—	10	—	13	—		
Address Valid to End of Write	t <sub>AVEH</sub>	9	—	10	—	13	—		
$\bar{E}$ Valid to AL Low	t <sub>EVALL</sub>	2	—	2	—	2	—		
Address Valid to AL Low	t <sub>AVALL</sub>	2	—	2	—	2	—		
$\bar{E}$ Valid to AL High	t <sub>EVALH</sub>	0	—	0	—	0	—		
Address Valid to AL High	t <sub>AVALH</sub>	0	—	0	—	0	—		
AL High to $\bar{W}$ Low	t <sub>ALHWL</sub>	0	—	0	—	0	—		
Address Valid to $\bar{W}$ Low	t <sub>AVWL</sub>	0	—	0	—	0	—		
Address Valid to $\bar{E}$ Low	t <sub>AVEL</sub>	0	—	0	—	0	—		
Data Valid to DL Low	t <sub>DVDLL</sub>	2	—	2	—	2	—		
Data Valid to $\bar{W}$ High	t <sub>DVWH</sub>	5	—	6	—	7	—		
Data Valid to $\bar{E}$ High	t <sub>DVEH</sub>	5	—	6	—	7	—		
DL High to $\bar{W}$ High	t <sub>DLHWH</sub>	5	—	6	—	7	—		
DL High to $\bar{E}$ High	t <sub>DLHEH</sub>	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\bar{E}$ High	t <sub>ALLEH</sub>	2	—	2	—	3	—		4
AL Low to Address Invalid	t <sub>ALLAX</sub>	2	—	2	—	3	—		4
DL Low to Data Invalid	t <sub>DLLDX</sub>	2	—	2	—	3	—		
$\bar{W}$ High to Address Invalid	t <sub>WHAX</sub>	0	—	0	—	0	—		
$\bar{E}$ High to Address Invalid	t <sub>EHAX</sub>	0	—	0	—	0	—		
$\bar{W}$ High to Data Invalid	t <sub>WHDX</sub>	0	—	0	—	0	—		
$\bar{E}$ High to Data Invalid	t <sub>EHDX</sub>	0	—	0	—	0	—		
$\bar{W}$ High to DL High	t <sub>WHDLH</sub>	0	—	0	—	0	—		
$\bar{E}$ High to DL High	t <sub>EFDLH</sub>	0	—	0	—	0	—		
$\bar{W}$ High to AL High	t <sub>WHALH</sub>	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\bar{W}$ High	t <sub>ALHWH</sub>	9	—	10	—	13	—		5
Write Pulse Width ( $\bar{G}$ Low)	t <sub>WLWH</sub>	9	—	10	—	13	—		
Write Pulse Width ( $\bar{G}$ High)	t <sub>WLWH</sub>	8	—	9	—	12	—		
Write Pulse Width	t <sub>WLEH</sub>	9	—	10	—	13	—		6
Enable to End of Write	t <sub>ELWH</sub>	9	—	10	—	13	—		7
Enable to End of Write	t <sub>ELEH</sub>	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t <sub>ALHALL</sub>	5	—	12	—	15	—	ns	4
Output Buffer Control:								ns	
$\bar{W}$ High to Output Valid	t <sub>WHQV</sub>	10	—	12	—	15	—		
$\bar{W}$ High to Output Active	t <sub>WHQX</sub>	3	—	3	—	5	—		8
$\bar{W}$ Low to Output High-Z	t <sub>WLQZ</sub>	0	5	0	6	0	9		8, 9

**NOTES:**

1. W (write) refers to either one or both byte write enables  $\bar{LW}$  and  $\bar{UW}$ .
2. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
3. Both Write Enables must be equal to  $V_{IH}$  for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high the output will remain in a high impedance state.
7. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low the output will remain in a high impedance state.
8. Transition is measured  $\pm 500$  mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t<sub>WLQZ</sub> is less than t<sub>WHQX</sub> for a given device.
9. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low the output will remain in a high impedance state.


## LATCHED WRITE CYCLES



## ORDERING INFORMATION (Order by Full Part Number)

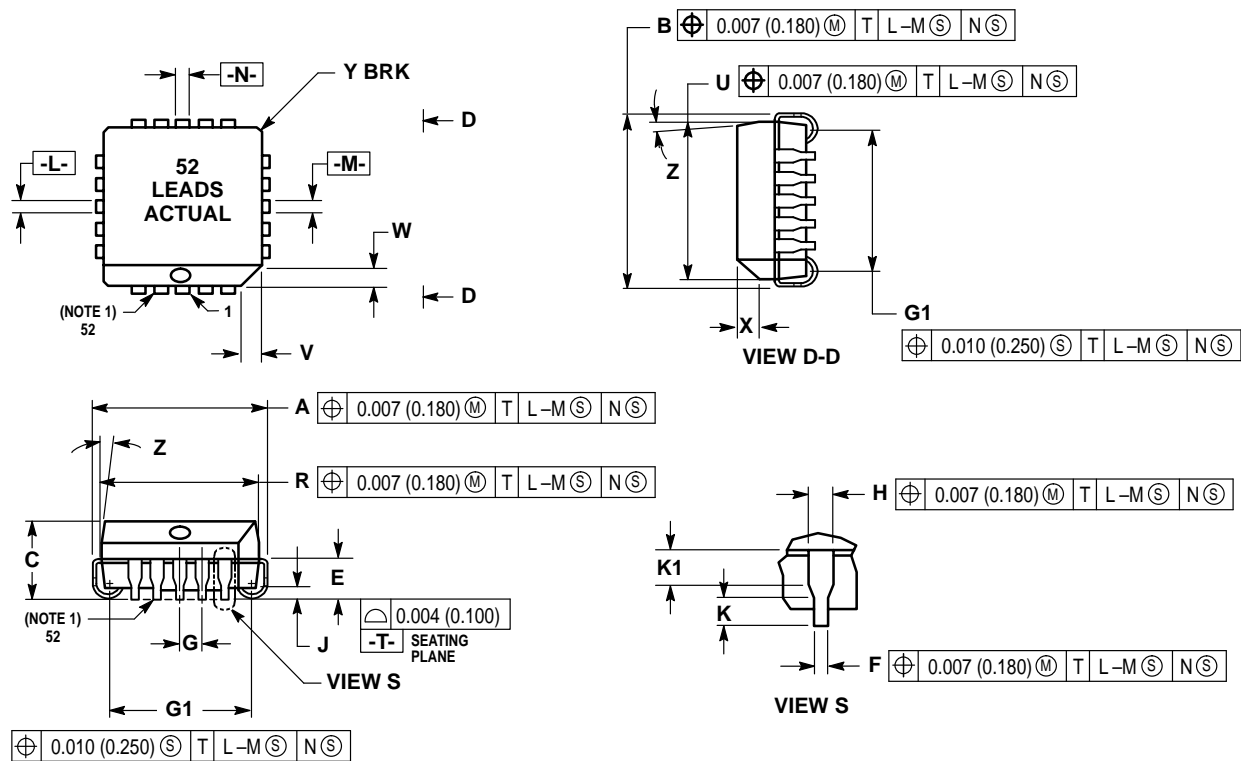
**MCM 67A518 X XX**  
 Motorola Memory Prefix \_\_\_\_\_ Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)  
 Part Number \_\_\_\_\_ Package (FN = PLCC)

Full Part Numbers — MCM67A518FN10 MCM67A518FN12 MCM67A518FN15

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# PACKAGE DIMENSIONS

## FN PACKAGE 52-LEAD PLCC CASE 778-02



**NOTES:**

1. DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

**Literature Distribution Centers:**

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