FUJITSU

8-CH 10-BIT A/D CONVERTER(ADC)

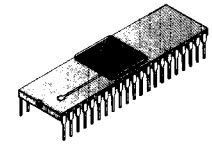
MB4051

July 1989
Edition 1.0

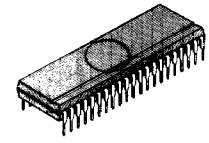
8-CHANNEL 10-BIT A/D CONVERTER

The Fujitsu MB4051 is a general purpose analog-to-digital converter (ADC) which features eight channels of analog inputs, 10-bit parallel data I/O port and programmable control register. Analog input signal on a selected input channel is converted to 10-bit digital data by the successive-approximation technique which provides high-speed conversion. The MB4051 is packaged in a standard 42-pin dual in-line packages.

- Multiplex 8-channel Analog Inputs
- Resolution: 10 bits
- Relative Accuracy: 8 bits Min.
- Linearity: ±1/2 LSB
- Successive-Approximation Technique: 50 μs/ch Max. at f_{CLK} = 250kHz
- Analog Input Voltage Range: 0V to 6.5V
- Analog Input Bias Current: 1μA Max.
- Input Impedance: over 500kΩ (for 6.5V Input)
- Built-in High Stabilized Reference Voltage Source
- Directly Connectable to DMA Controller as well as Microprocessor
- TTL Compatible Digital I/O Port
- Standard 42-pin DIP
- Power Supplies: +5V and ±8V
- Power Consumption: 400mW Typ.



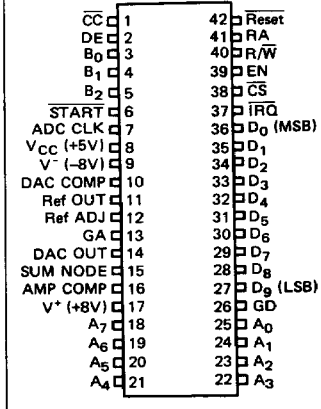
CERAMIC PACKAGE
DIP-42C-A01



PLASTIC PACKAGE
DIP-42P-M01

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (All Voltage referenced to A.G/D.G)

Parameter		Symbol	Value	Unit
Supply Voltage 1		V_{CC}	+7	V
Supply Voltage 2		V^+	+10	V
Supply Voltage 3		V^-	-10	V
Digital Input Voltage		V_{ID}	-0.5 to +5.5	V
Analog Input Voltage		V_{IA}	-3.0 to V^+	V
Operating Temperature		T_A	-35 to +90	°C
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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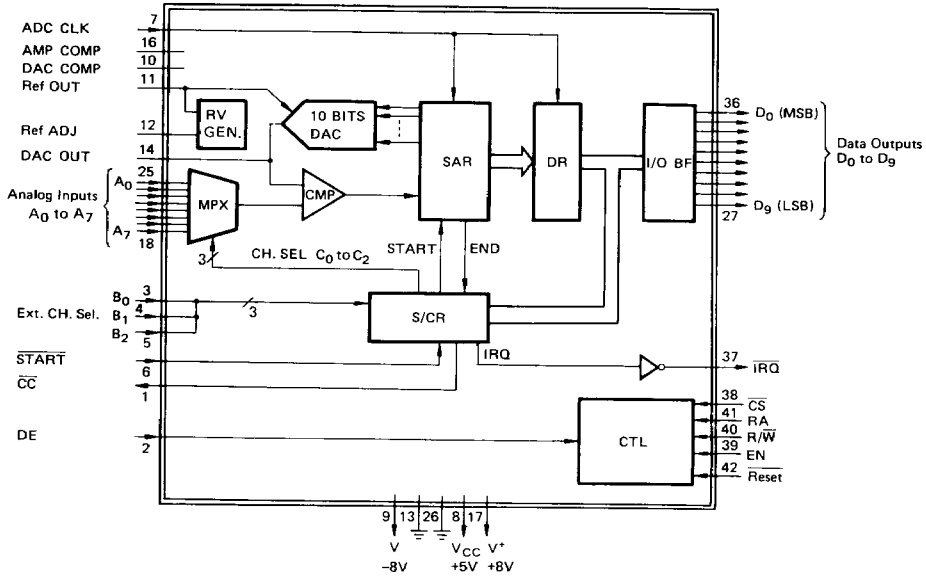
Fig. 1 – MB4051 BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage 1	V_{CC}	4.75	5.0	5.25	V
Supply Voltage 2	V^+	7.6	8.0	8.4	V
Supply Voltage 3	V^-	-8.4	-8.0	-7.6	V
Digital Output High Current	I_{OH}			-0.4	mA
Digital Output Low Current	I_{OL}			8	mA
Operating Temperature	T_{OP}	-30		+85	°C

NOTE: The negative value means "flow of current" from IC to out side of IC.

FUNCTIONAL BLOCK DESCRIPTIONS

Symbol	Name	Function
MPX	Multiplexer	Selects one channel from 8-channel analog input signals. Channel assignment is done by the 2nd thru 4th bits of control register which are programmed by the external channel select inputs B_0 thru B_2 or by a data from MPU.
CMP	Comparator	Compares an unknown analog input signal with an output signal of built-in DA converter. The result of comparison is transferred to the successive-approximation register (SAR).
DAC	DA Converter	10-bit digital-to-analog converter. Generates analog signal corresponding to digital signal specified by the SAR.
SAR	Successive-Approximation Register	According to the result from the comparator, generates the next step digital output to be transferred to the DAC and compared in the comparator. Composed of 10-bit register and control logic. After completion of data-conversion, acts as the data register (DR).
SR	Status Register	10-bit register which indicates the status of operations. Indicates the assigned channel by SR-2 to SR-4, status of the external control/MPU by SR-5, operation of AD conversion by SR-6 and completion of AD conversion by SR-7. (See Table 1, 2 of page 14)
CR	Control Register	10-bit register which controls the operation of ADC. Assigns a channel by CR-2 to CR-4, switches MPU/external control each other by CR-5, initiates AD conversion by CR-6. (See Table 1, 2 of page 14)
DR	Data Register	Stores a 10-bit data at the completion of AD conversion. Outputs the data at DE=1 during the external control mode (CR-5=5). If the DR is selected ($\overline{CS}$=0, RA=0, and R/$\overline{W}$=1) during the MPU control mode (CR-5=1), the contents can be read by MPU (EN=1).
I/O BF	Input/Output Buffer	Connected to the data-bus of MPU for sending or receiving the 10-bit data. The output is three-state TTL compatible.
CTL	Control Logic	Controls sending and receiving of data between blocks and used for initializing.
Ref	Reference Voltage Regulator	Specifies the maximum analog input signal level of ADC.

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PIN DESCRIPTIONS

Symbol	Name	Function
A_0 to A_7	Analog Input	Analog input terminals of 8 channels, one of which is assigned by CR-2 to CR-4.
D_0 to D_9 D_0 ..... MSB D_9 ..... LSB	Data I/O Port	Connected to 10-bit parallel data-bus for transferring 10-bit data between internal registers and MPU.
$\overline{CS}$	Chip Select	Chip-select terminal of ADC which is selected at $\overline{CS}$=0.
RA	Register Address	Address input for the internal registers. Selects the data register (DR) at RA=0 and the control register (CR)/status register (SR) at RA=1.
R/$\overline{W}$	Read-Write Control	Input for the read-write signal from MPU (MPU read mode at R/$\overline{W}$=1).
EN	Enable Signal	Input for the enable signal of MPU system. EN is used as timing for data transfer between MPU and ADC.
$\overline{Reset}$	Reset	Initializes the ADC at $\overline{Reset}$=0.
B_0 to B_2	External Channel Select Input	When ADC is controlled external (CR-5=0), the inputs from B_0 to B_2 are set in CR-2 to CR-4 at the falling edge of $\overline{START}$. (See Table 3 of page 14)
$\overline{START}$	Start	AD conversion starts at the rising edge of $\overline{START}$ when the external control mode (CR-5=0).
$\overline{CC}$/$\overline{IRQ}$ (Open Collector)	Conversion Complete/ Interrupt Request	Indicates the completion of data conversion. After completion of data conversion, $\overline{CC}$ goes low at the external control mode (CR-5=0) or $\overline{IRQ}$ goes low at the MPU control mode (CR-5=1). In both cases, they go high after the content of the data register is read.
DE	Data Enable	During DE=1 at the external control mode, the data in a register assigned by RA are output on D_0 to D_9.
ADC CLK	AD Conversion Clock	Clock for AD conversion which is input to the SAR and determines the conversion speed of ADC. A data conversion is completed by 12 cycles of clock. Not required to synchronize with the EN (Enable) signal from MPU system. Minimum cycle time of this clock is 2μs.
Ref OUT/ Ref ADJ	Reference Output/ Reference Adjustment	Terminals for output of reference voltage which specifies the full-scale value of analog input signal and for its adjustment.
AMP COMP/ DAC COMP/ DAC OUT/ SUM NODE	Amplifier Compensation/ DAC Compensation/ DAC Output/ Sum Node	Terminals for frequency adjustment of the internal operational amplifier with connected capacitors having specified capacitances. SUM NODE is also used for offset adjustment.
$V^+/V_{CC}/V^-$	Terminals for Power Supply	To be supplied +8V, +5V and −8V, respectively. (Note 1)
GA/GD	Analog Ground/ Digital Ground	Terminals for ground.

NOTE 1: MB3758 DC-DC Converter is available, which generates +8V and −8V from signal +5V power supply.

ELECTRICAL CHARACTERISTICS

1. ANALOG CIRCUIT CHARACTERISTICS

(V_{CC} = +5V, V^+ = +8V, V^- = -8V, T_A = -30°C to +85°C)

Parameter		Value			Unit	Note
		Min	Typ	Max		
Resolution				10	bit	
Accuracy	Relative Accuracy	8			bit	
	Gain Error		±1		% of FSR	Adjustable
	Offset Error		±0.03		% of FSR	Adjustable
	Differential Linearity Error		±0.5		LSB	
Drift	Full Scale Voltage		40		ppm/°C	
	Offset Voltage		±0.5		ppm of FSR/°C	
Full Scale Power Supply Fluctuation Suppressing Ratio	Positive Power Supply		1.0		mV/V	8V±5%
	Negative Power Supply		-0.5		mV/V	-8V±5%
Analog Input	Input Current			1	μA	V_{IA} = 0 to 6.5V
	Full Scale Voltage			6.5	V	
Reference Voltage	Reference Voltage		5.0		V	
	Drift		30		ppm/°C	
Supply Current	Positive Power Supply		7	12	mA	
	Negative Power Supply		-10	-17	mA	
Conversion Cycle Time				50	μs/ch	f_{CLK} = 250Hz

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2. DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC} = +5V ± 5%, V^+ = +8V, V^- = −8V, T_A = −30°C to +85°C)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input High Voltage	V_{IH}			2			V
Input Low Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IC}	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
Output High Voltage	V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −2.6mA		2.4			V
Output Low Voltage	V_{OL}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OL} = 4mA			0.4	V
			I_{OL} = 8mA			0.5	
Output Current (Off State)	I_{OZ}	V_{IH} = 2V, V_{CC} = 5.25V V_{IL} = 0.8V	V_O = 2.7V			20	μA
			V_O = 0.4V			−20	
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.25V				20	μA
		V_{IH} = 7V, V_{CC} = 5.25V				100	
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.25V				−400	μA
Output Short Current	I_{OS}	V_O = 0V, V_{CC} = 5.25V		−15		−95	mA
Supply Current	I_{CC}	A_0 to A_7, $\overline{Reset}$ = GND, V_{CC} = 5.25V		30	55	92	mA

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3. DIGITAL CIRCUIT AC CHARACTERISTICS
(V_{CC} = +5V±5%, V^+ = +8V, V^- = –8V, T_A = –30°C to +85°C)

ADC CLK

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Cycle time	t_{CY}		4			μs
H Level Pulse Width	t_{WAC^+}		1			μs
L Level Pulse Width	t_{WAC^-}		1			μs

Read Mode

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EN Pulse Width	P_{WEN}		270			ns
$\overline{CS}$, R/$\overline{W}$, RA Setup Time	t_{AS}		20			ns
$\overline{CS}$, R/$\overline{W}$, RA Hold Time	t_{AH}		10			ns
Enable Time from EN	t_{EEN}	Fig. 2*			160	ns
Access Time from RA	t_{ARA}	Fig. 2*			300	ns
Disable Time from EN	t_{DEN}	Fig. 2*	10		120	ns
$\overline{IRQ}$ Recovery Time from EN	t_{IR}	Fig. 3*			240	ns

* : See page 11

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Write Mode

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EN Pulse Width	P_{WEN}		270			ns
$\overline{CS}$, R/$\overline{W}$, RA Setup Time	t_{AS}		20			ns
$\overline{CS}$, R/$\overline{W}$, RA Hold Time	t_{AH}		10			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns

External Control AD Conversion

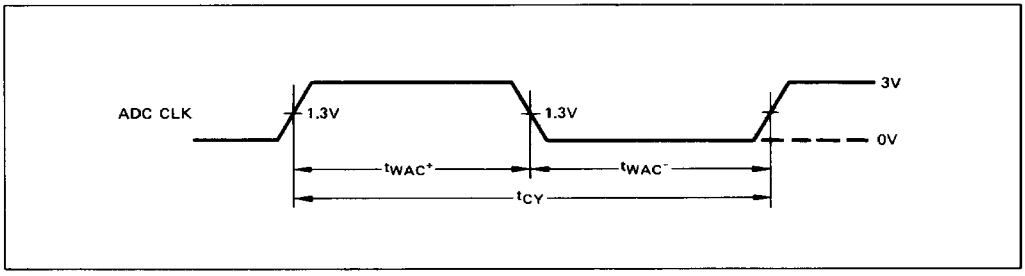
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
$\overline{START}$ Pulse Width	P_{WSL}		270			ns
Channel Setup Time	t_{BS}		20			ns
Channel Hold Time	t_{BH}		270			ns

External Control Read Mode

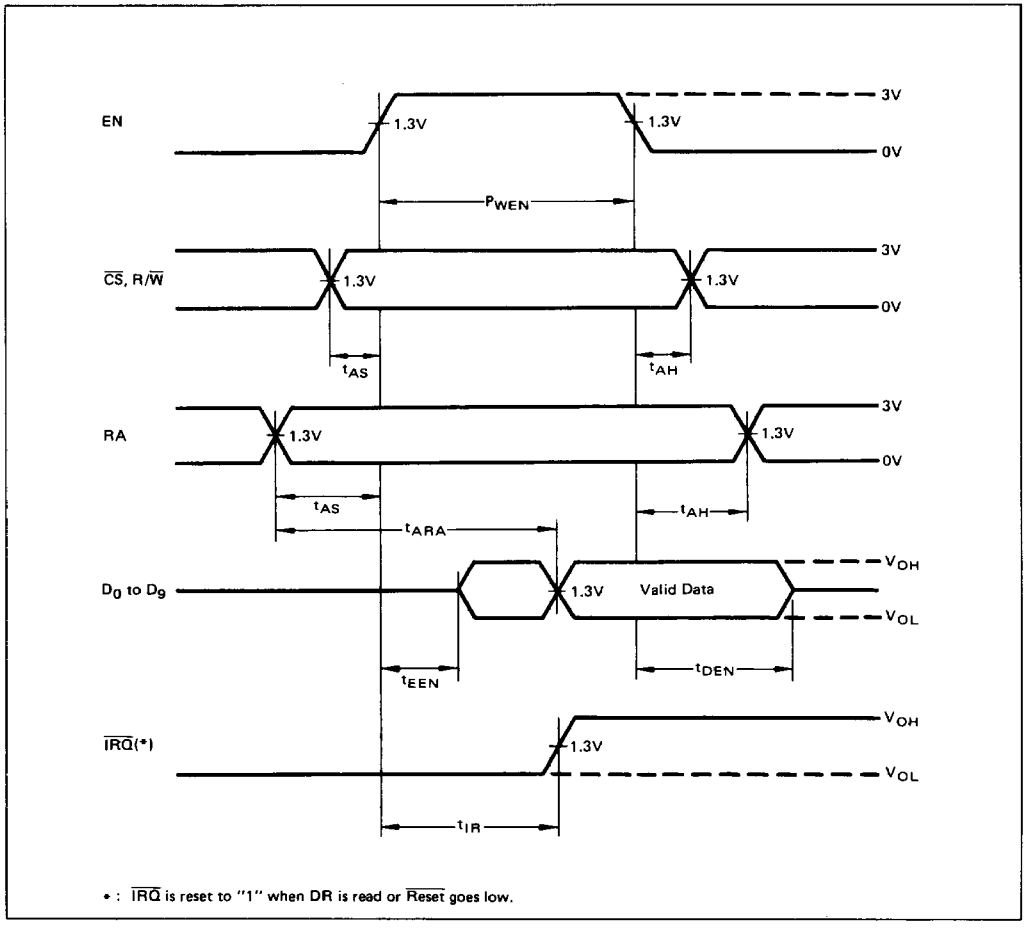
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
DE Pulse Width	P_{WDEH}		270			ns
Enable Time from DE	t_{EDE}	Fig. 2*			160	ns
Disable Time from DE	t_{DDE}	Fig. 2*	10		160	ns
$\overline{CC}$ Recovery Time from DE	t_{CCR}	Fig. 3*			280	ns

* : See page 11

ADC CLK



READ Timing Diagram



• : $\overline{IRQ}$ is reset to "1" when DR is read or $\overline{Reset}$ goes low.

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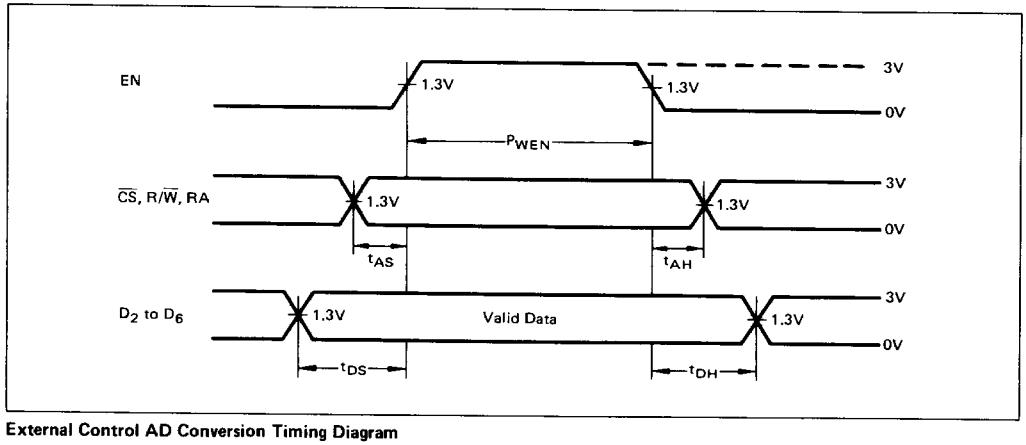
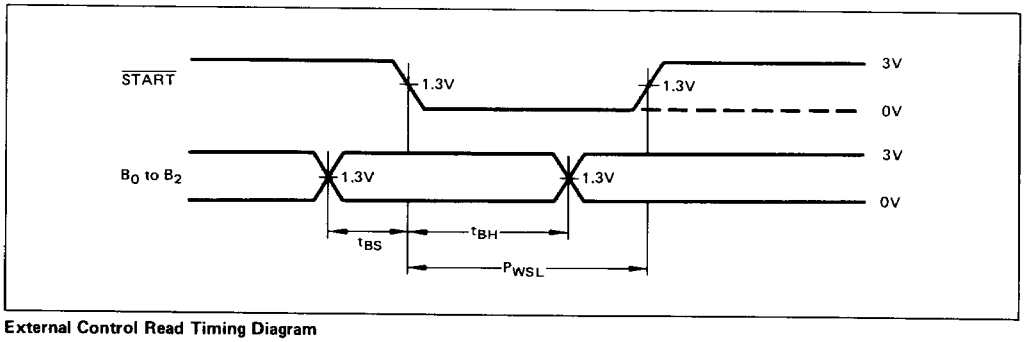
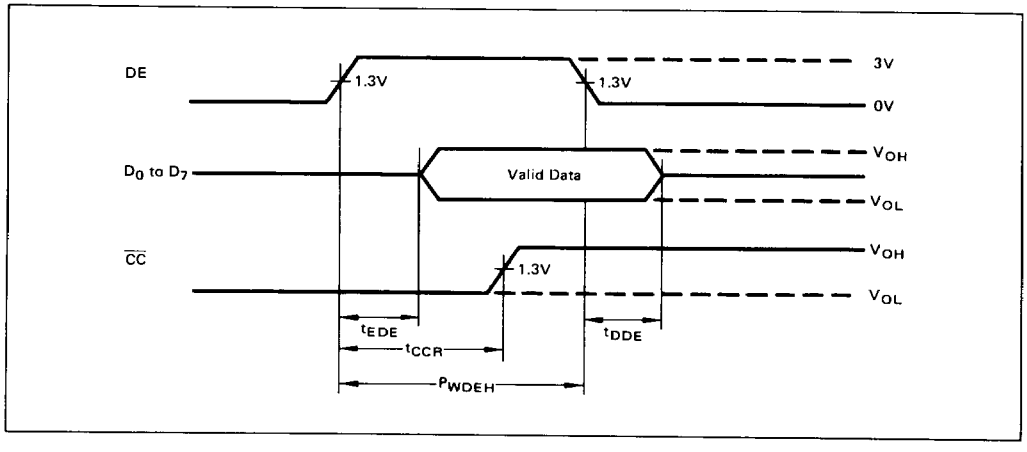
WRITE Timing Diagram



External Control AD Conversion Timing Diagram



External Control Read Timing Diagram



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4. SWITCHING CHARACTERISTICS TEST CONDITIONS

Fig. 2 – 3-STATE OUTPUT LOAD CONDITION

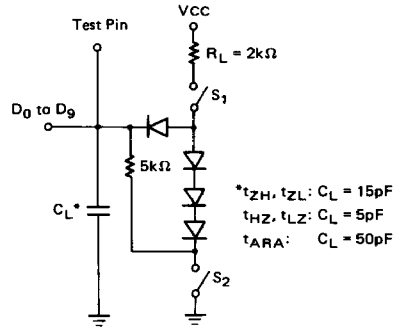
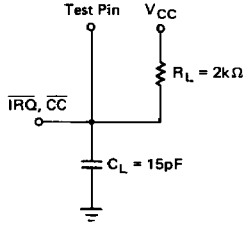
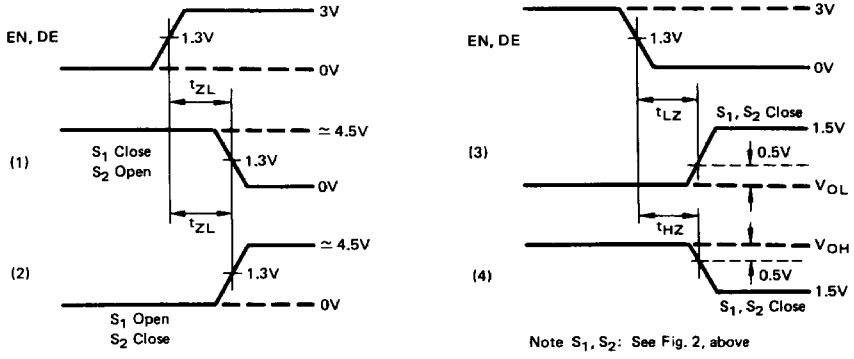


Fig. 3 – OPEN COLLECTOR OUTPUT LOAD CONDITION



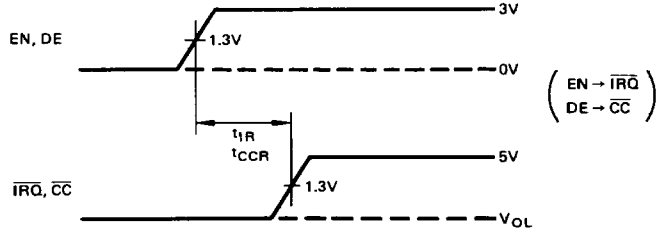
5. SWITCHING WAVEFORM

Enable, Disable Time (3-State Output)



Note S_1, S_2: See Fig. 2, above

$\overline{IRQ}$ or $\overline{CC}$ Recovery Time (Open Collector Output)



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TYPICAL CHARACTERISTICS CURVES

Fig. 4 – OUTPUT VOLTAGE vs. INPUT VOLTAGE

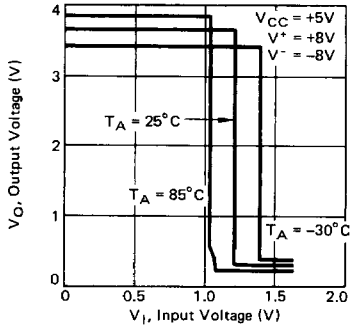


Fig. 5 – OUTPUT HIGH VOLTAGE vs. OUTPUT HIGH CURRENT

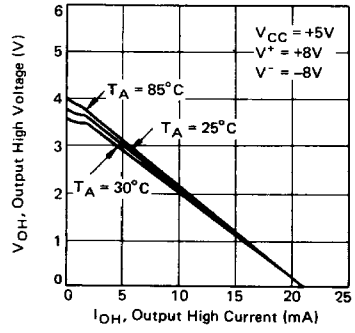


Fig. 6 – OUTPUT LOW VOLTAGE vs. OUTPUT LOW CURRENT

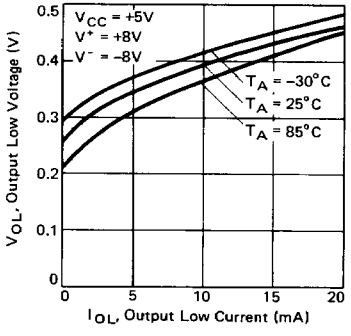


Fig. 7 – INPUT CURRENT vs. INPUT VOLTAGE (B_0 INPUT)

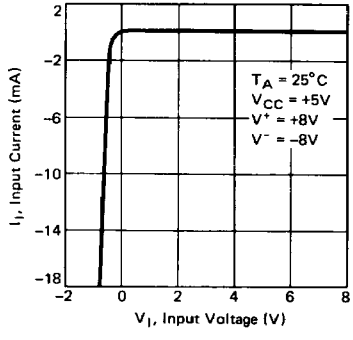
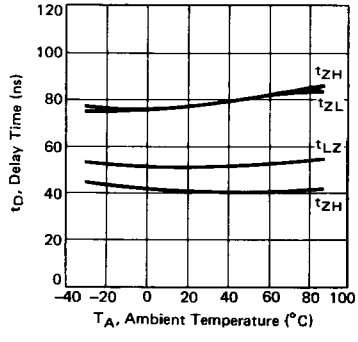


Fig. 8 – DELAY TIME vs. AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 9 – SUPPLY CURRENT vs. SUPPLY VOLTAGE

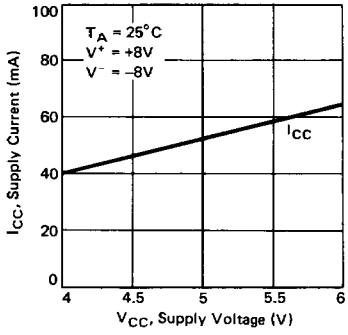


Fig. 10 – SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE

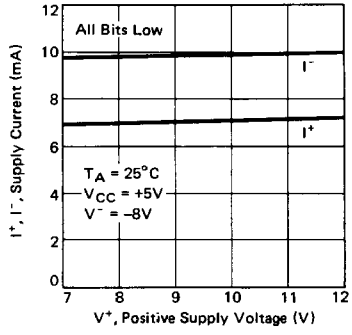


Fig. 11 – SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE

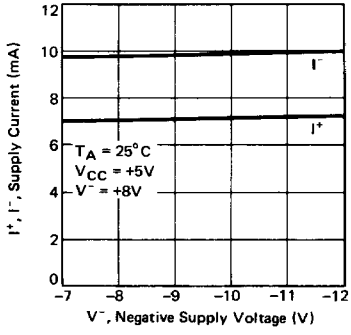


Fig. 12 – FULL SCALE VOLTAGE vs. REFERENCE VOLTAGE SUPPLY VOLTAGE (V^+, $|V^-|$)

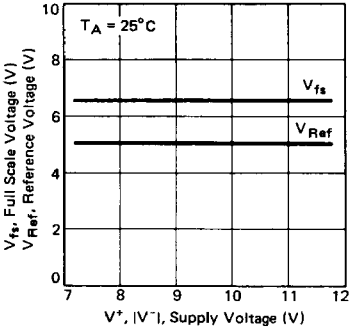


Fig. 13 – OPERATION WAVEFORM

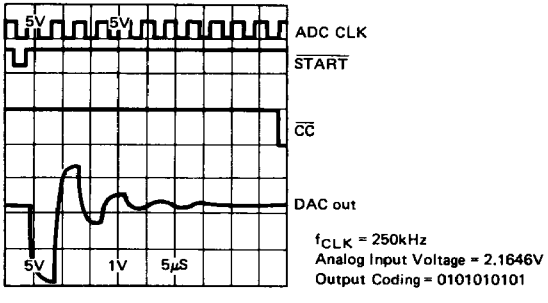


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Table 1. BIT CONSTRUCTION OF DR AND S/C R

	RA	R/$\overline{W}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9
DR	0	1 Read	Bit 0 (MSB)	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9 (LSB)
S/C R	1	1 Read	–	–	Input CH. Select			Mode Control	Busy	IRQ	–	–
		0 Write			C_0	C_1	C_2	INT/EXT	Start	–		

Table 2. CHANNEL SELECT FOR MPU CONTROL

C_2	C_1	C_0	Selected CH.
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

Table 3. CHANNEL SELECT FOR EXTERNAL CONTROL

B_2	B_1	B_0	Selected CH.
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

ADC OPERATION MODES

According to the status of 5th bit (CR-5) in the built-in control register, ADC has two operation modes: external control mode and MPU control mode.

Just after an initialization ($\overline{\text{Reset}}$ going from low to high), ADC is in the external control mode (designation of channel, start of data conversion and data output are controlled through the external control input terminals). This mode is useful for ADC applications only or for DMA operation independent of MPU.

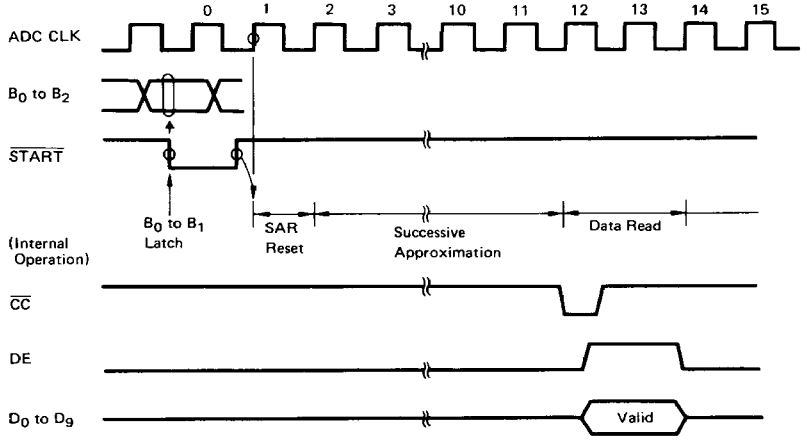
When the MPU control mode is required, set CR-5 of the control register high through MPU.

EXTERNAL CONTROL MODE (CR-5=0):

This mode is used when ADC is controlled by the external hardware. An analog input signal channel is designated by B_0 to B_2 and the AD conversion starts at the second rising edging of ADC clock after $\overline{\text{START}}$ goes low.

At the completion of 10-bit data conversion, $\overline{\text{CC}}$ (Convert Complete) goes low to notify it to external devices. The converted data is read after the low state of $\overline{\text{CC}}$ and DE goes high.

ADC TIMING FOR EXTERNAL CONTROL MODE



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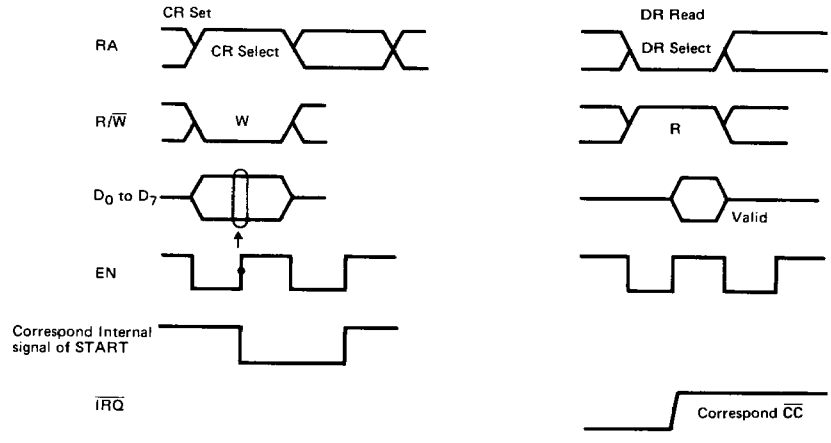
MPU CONTROL MODE (CR-5=1):

This mode is used when ADC is controlled by the MPU software. Because of CR-5=0 at initialization, CR-5 should be set high through MPU. After completion of the conversion, CR-7 (IRQ flag) is set high and $\overline{IRQ}$ output goes low to interrupt MPU operation.

After confirming $\overline{IRQ}$=0, MPU starts the interrupt routine to select the data register of ADC and reads it. After MPU reads the data register, $\overline{IRQ}$ is reset high. In this mode, all signals on $\overline{START}$ and B_0 to B_2 are ignored. When the ADC is required to return to the external control mode, CR-5 is set low through MPU or $\overline{RESET}$ is set low.

ADC TIMING FOR MPU CONTROL MODE



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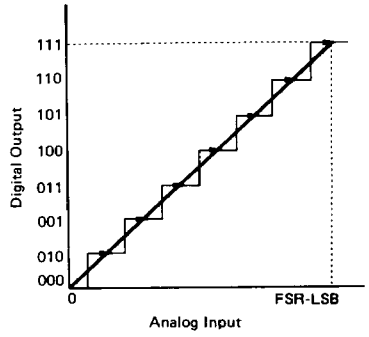
TECHNICAL INFORMATION

DEFINITION OF TERMS

Resolution:
The minimum distinguishable analog deviation in AD converter. Since MB4051 is 10-bit AD converter, it is possible to resolute an analog signal, from 0V to 6.5V (FSR), into 2^{10} = 1024 parts.

EXAMPLE OF RESOLUTION
(3-BIT RESOLUTION)

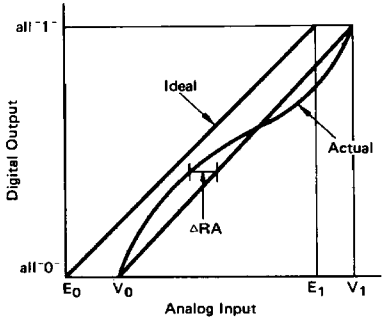


Relative Accuracy:
Deviation between a straight line from the zero point of the device (all "0") to the full-scale point (all 'L') and an actual conversion characteristic curve.

Gain Error:
Difference between an ideal input voltage span and an actual input voltage span. In the MB4051, according to the procedure described separately, it is possible to adjust the gain error to zero.

Offset Error:
Difference between an ideal cirtical input voltage which makes all output bits zero and an actual critical input voltage. In the MB4051, such offset error can be adjusted according to the procedure described separately.

RELATIVE ACCURACY/GAIN
ERROR/OFFSET ERROR



*: Relative Accuracy = ΔRA

$$\text{Gain Error} = \frac{(V_1 - V_0) - (E_1 - E_0)}{FSR} \times 100 \text{ (\% of FSR)}$$

$$\text{Offset Error} = \frac{V_0 - E_0}{FSR} \times 100 \text{ (\% of FSR)}$$

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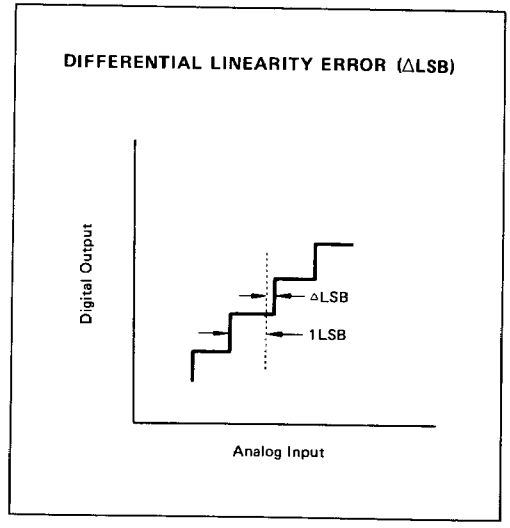
DEFINITION OF TERMS (Continued)

Differential Linearity Error:
Input voltage deviation from an ideal input voltage which is necessary to change the output code as large as 1LSB. The differential linearity error of ±1/2LSB means that, when the input signal changes 1/2LSB to 3/2LSB, digital code varies 1LSB.



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Example of Output Coding

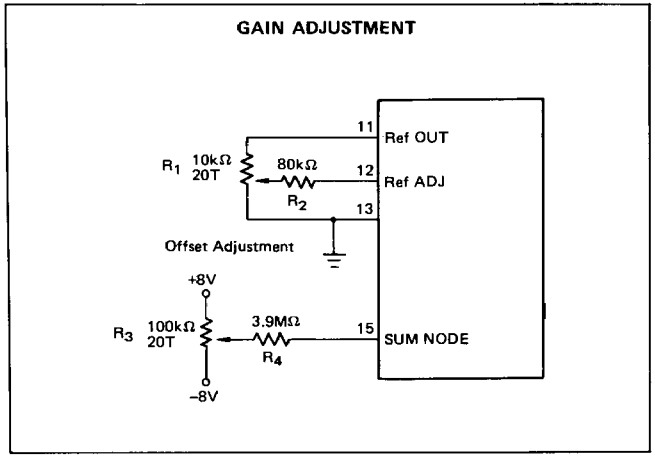
Scale	Input Voltage	MSB	D1	D2	D3	D4	D5	D6	D7	D8	LSB
FS-1LSB	6.4937	1	1	1	1	1	1	1	1	1	1
FS/2	3.2500	1	0	0	0	0	0	0	0	0	0
FS/4	1.6250	0	1	0	0	0	0	0	0	0	0
FS/8	0.8125	0	0	1	0	0	0	0	0	0	0
FS/16	0.4063	0	0	0	1	0	0	0	0	0	0
FS/32	0.2031	0	0	0	0	1	0	0	0	0	0
FS/64	0.1016	0	0	0	0	0	1	0	0	0	0
FS/128	0.0508	0	0	0	0	0	0	1	0	0	0
FS/256	0.0254	0	0	0	0	0	0	0	1	0	0
FS/512	0.0127	0	0	0	0	0	0	0	0	1	0
FS/1024 = 1LSB	0.0063	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	0	0	0	0	0	0	0	0	0

APPLICATIONS INFORMATION

ADJUSTMENT OF OFFSET AND GAIN

In the MB4051, Both gain-error and offset-error can be adjusted to zero by trimmers connected as shown below. In this case, potentiometers and resistors for trimmers should have temperature characteristics below 100 ppm/°C to ensure long-term stability and less temperature drift.

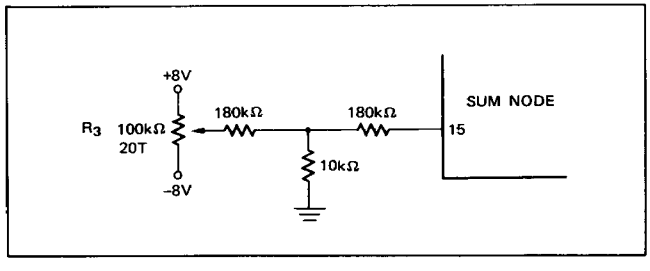
The following external adjustment circuits should be located as near as possible to the package.



Offset Adjustment

By applying the voltage of 1/2LSB, i.e., 3.2mV to an analog input channel, continuously execute AD conversion of the applied input voltage. Then, adjust potentiometer R_3 during the conversion so that the conversion results become "0000000000" and "0000000001", alternatively. The range of adjustment is about ±0.2% of FSR in the circuit shown below.

The R_4 resistor for offset adjustment can be replaced with smoller resistors as follows.



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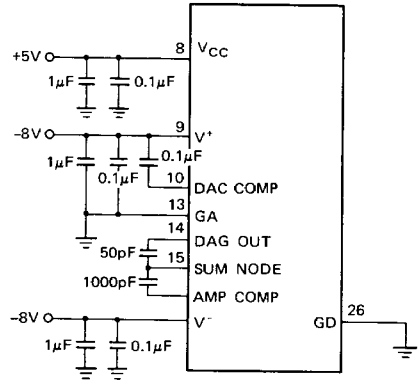
GAIN ADJUSTMENT

After offset adjustment, by applying FSR-3/2LSB (6.4905V) to an analog input, execute AD conversion of the applied input voltage. Then, adjust potentiometer R_1 during the conversion so that the conversion results become "1111111111" and "1111111110", alternatively. The range of adjustment is about −12% to +5% of FSR in the circuit shown.

PRECAUTIONS FOR CIRCUIT STABILIZATION

To stabilize the ADC operation and by-pass power supply line noise, connect the external capacitors as shown.

CAPACITORS FOR STABILIZATION AND POWER SUPPLY BYPASS

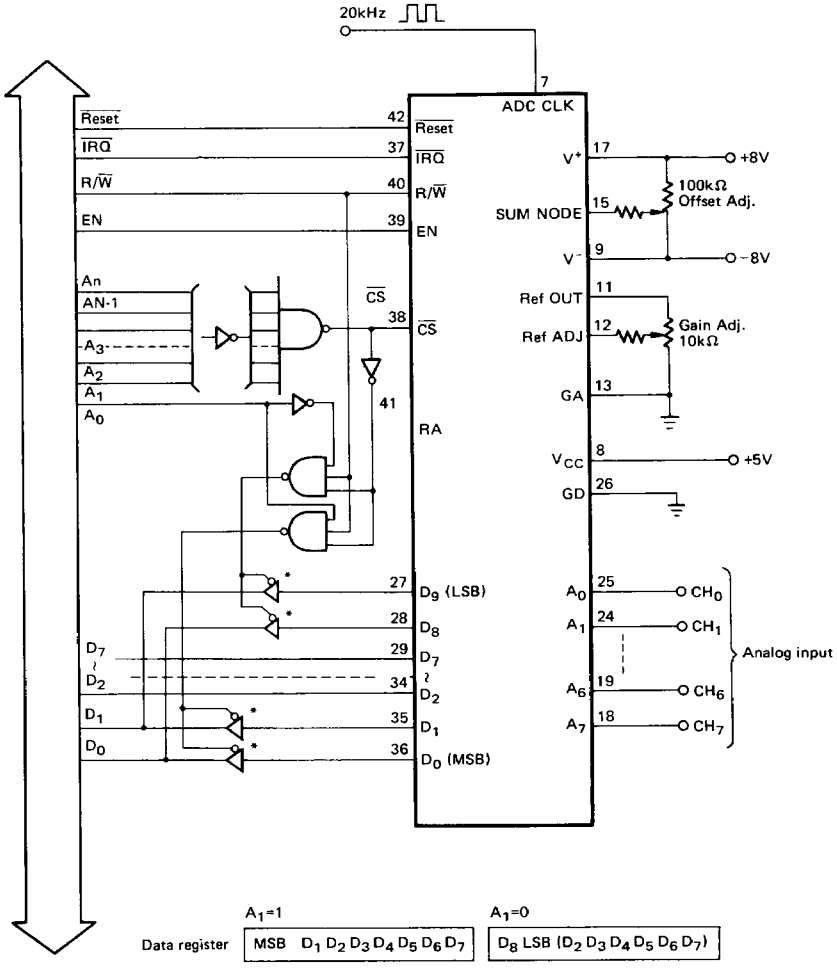


Bypass capacitor for filtering line-noise should have good high-frequency characteristics and should be connected as near as possible to the package.

If a printed circuit board is used, the ground-line should be made as wide as possible and the pattern should be made in such a manner that the analog input signal line does not pick up noise from the digital signal and so on. Unused digital input should be kept in an inactive state listed below and unused analog input should be connected to analog ground (GA).

Inactive State	Terminals
"L"	EN, RA, R/$\overline{W}$, DE, B_0 to B_2
"H"	$\overline{Reset}$, $\overline{CS}$, $\overline{START}$

EXAMPLE OF INTERFACE TO 8-BIT MPU
(PROVIDE A CHANGE CIRCUIT FOR UPPER 2-BITS)



NOTE: * MB74LS367 or MB487x1

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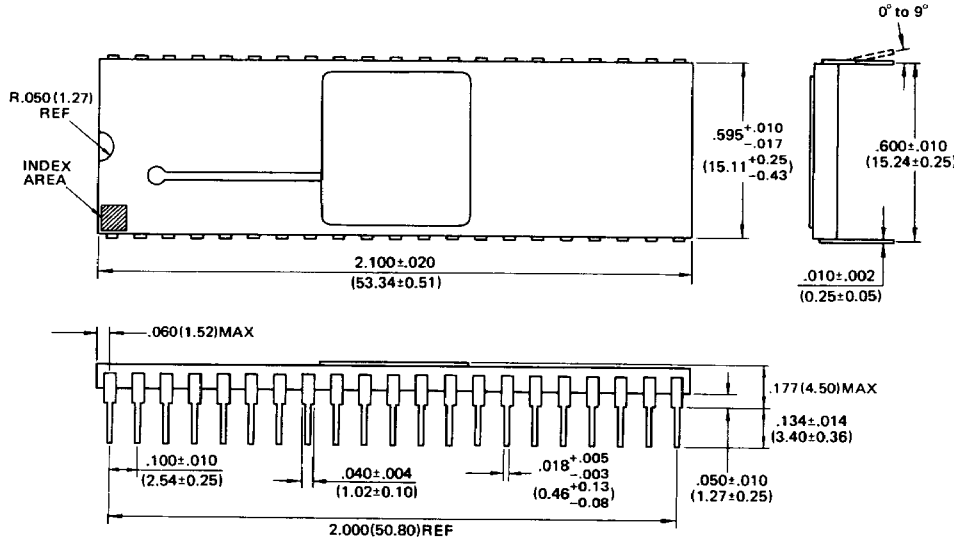
PACKAGE DIMENSIONS

42-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42C-A01)



Dimensions in
inches (millimeters)

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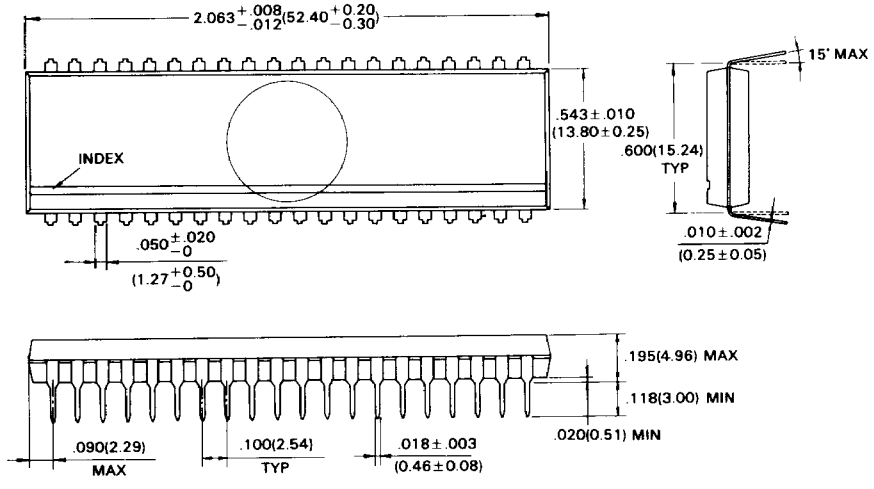
PACKAGE DIMENSIONS (continued)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-40P-M01)



Dimensions in
inches (millimeters)

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