

SHARP

LZ2547

Single-voltage (5 V) operation 1/5-type
Color CCD Area Sensor for PAL

Description

LZ2547 is a 1/5-type (3.6 mm) solid state imaging device driven by only 5 V single power supply.

Having about 220,000 pixels (horizontal 384 × vertical 582), it allows a stable color image.

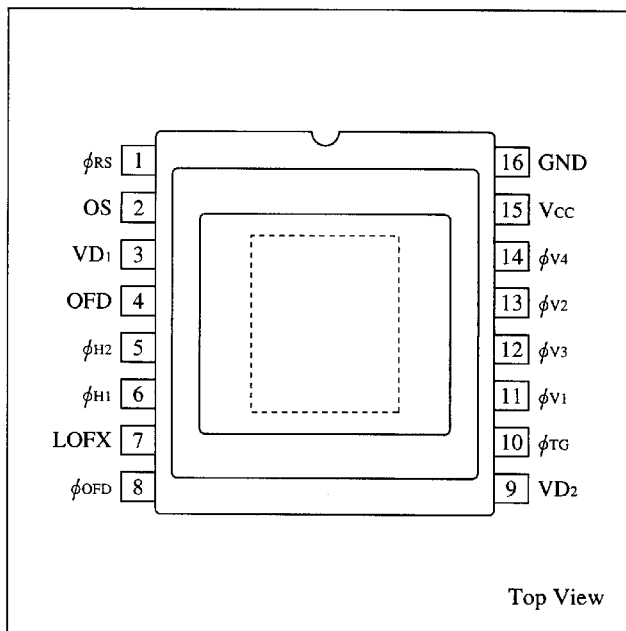
Features

1. Single-voltage (5 V) operation
2. Number of video picture elements : 362(H) × 582(V)
Pixel pitch : 8.2 μm(H) × 3.8 μm(V)
Number of optical back pixels : Horizontal; front 2 and rear 20
3. Compatible with PAL standard
4. Reduced fixed pattern noise and lag
5. No sticking and no image distortion
6. Blooming suppression structure
7. Built-in output amplifier, voltage generator, pulse mix circuit
8. Variable electronic shutter (1/50 to 1/10 000 s)
9. Package : 16-pin WDIP [Ceramic] Pin-pich 1.27 mm
(WDIP016-N-0450)

Pin Description

| No. | Symbol | Pin name | Note |
|-----|-----------------|--------------------------------------|------|
| 1 | ϕ_{RS} | Reset transistor gate clock | 1 |
| 2 | OS | Video output | |
| 3 | VD ₁ | Voltage-generator output | 2 |
| 4 | OFD | Overflow drain | 3 |
| 5 | ϕ_{H2} | Horizontal shift register gate clock | |
| 6 | ϕ_{H1} | Horizontal shift register gate clock | |
| 7 | LOFX | Electronic shutter clock | |
| 8 | ϕ_{OFD} | Electronic shutter clock | 4 |
| 9 | VD ₂ | Voltage-generator output | 2 |
| 10 | ϕ_{TG} | Transfer gate clock | |
| 11 | ϕ_{V1} | Vertical shift register gate clock | 5 |
| 12 | ϕ_{V3} | Vertical shift register gate clock | |
| 13 | ϕ_{V2} | Vertical shift register gate clock | |
| 14 | ϕ_{V4} | Vertical shift register gate clock | |
| 15 | V _{CC} | Power supply | |
| 16 | GND | Ground | |

Pin Connections



- Note 1. ϕ_{RS} : Input the clock through a 0.1 μF capacitor.
- Note 2. VD₁, VD₂ : Connect to GND through a 0.1 μF capacitor and a zener-diode (15.5 ± 0.5 V).
VD₁ : Connect to GND through a 1 MΩ variable resistor.
- Note 3. OFD : Supply DC voltage with a following emitter-follower circuit (with a 1 MΩ emitter resistance).
· Collector connects VD₁
· Emitter connects OFD through a diode
· Base connects a 1 MΩ variable resistor
- Note 4. ϕ_{OFD} : Connect to OFD through a diode and a 0.22 μF capacitor.
- Note 5. ϕ_{V1} - ϕ_{V4} : Input the clock through a 0.1 μF capacitor.

Absolute Maximum Ratings

(Ta=25 °C)

| Parameter | Symbol | Rating | Unit |
|-----------------------------------------|-------------------|-----------------------|------|
| Power supply | V _{CC} | 0 to +7.3 | V |
| Overflow drain voltage | V _{OFD} | 0 to +35 | V |
| Reset gate clock P-P level | V _{φ RS} | 0 to +V _{CC} | V |
| Vertical shift register clock P-P level | V _{φ v} | 0 to +V _{CC} | V |
| Horizontal shift register clock voltage | V _{φ H} | 0 to +V _{CC} | V |
| Transfer gate clock voltage | V _{φ TG} | 0 to +V _{CC} | V |
| Electronic shutter clock voltage | V _{LOFX} | 0 to +V _{CC} | V |
| Storage temperature | T _{stg} | -40 to +85 | °C |
| Operating ambient temperature | T _{opr} | 0 to +60 | °C |

Recommended Operating Conditions

| Parameter | | Symbol | MIN. | TYP. | MAX. | Unit |
|-------------------------------------------|---------------------------------|-------------------------------------------------------------------------------|------|-----------------|------|------|
| Operating ambient temperature | | T _{opr} | | 25 | | °C |
| Power supply voltage | | V _{CC} | 4.75 | 5.0 | 5.25 | V |
| Overflow drain voltage | When DC is applied | V _{OFD} | 3.0 | (adjust) | 16 | V |
| | When pulse is applied P-P level | V _{φ OFD} | | | 16 | V |
| Ground voltage | | GND | | 0 | | V |
| Reset gate clock | P-P level | V _{φ RS} | | V _{CC} | | V |
| Vertical shift register clock | P-P level | V _{φ v1} , V _{φ v2} , V _{φ v3} , V _{φ v4} | | V _{CC} | | V |
| Horizontal shift register clock | LOW level | V _{φ H1L} , V _{φ H2L} | | 0 | | V |
| | HIGH level | V _{φ H1H} , V _{φ H2H} | | V _{CC} | | V |
| Transfer gate clock | LOW level | V _{φ TGL} | | 0 | | V |
| | HIGH level | V _{φ TGH} | | V _{CC} | | V |
| Electronic shutter clock | LOW level | V _{LOFXL} | | 0 | | V |
| | HIGH level | V _{LOFXH} | | V _{CC} | | V |
| Vertical shift register clock frequency | | f _{φ v1} , f _{φ v2} , f _{φ v3} , f _{φ v4} | | 15.63 | | kHz |
| Horizontal shift register clock frequency | | f _{φ H1} , f _{φ H2} | | 6.75 | | MHz |
| Reset gate clock frequency | | f _{φ RS} | | 6.75 | | MHz |

■ Electrical Characteristics

- Drive method : Field accumulation
- DC and AC conditions : The typical values under the recommended operating conditions.
- Ta=25 °C
- Temperature of light source : 3 200 K
- Infrared absorbing filter (CM-500, 1 mm) is used.

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit | Note |
|-------------------------------|-------------------|------|------|------|------|------|
| Standard output voltage | V _o | | 150 | | mV | 5 |
| Photo response non-uniformity | PRNU | | | 15 | % | 6 |
| Saturation signal | V _{sat} | 450 | | | mV | 7 |
| Dark output voltage | V _{dark} | | 0.5 | | mV | 4, 8 |
| Dark signal non-uniformity | DSNU | | 0.5 | | mV | 4, 9 |
| Sensitivity | R | | 170 | | mV | 10 |
| Smear ratio | SMR | | -85 | | dB | 11 |
| Image lag | AI | | | 1.0 | % | 12 |
| Blooming suppression ratio | ABL | 1000 | | | | 13 |
| Current dissipation | I _{oD} | | 4.0 | 8.0 | mA | |
| Output impedance | R _o | | 400 | | Ω | |
| Vector breakup | | | | 10 | °, % | 14 |
| Line crawling | | | | 3.0 | % | 15 |
| Luminance flicker | | | | 2.0 | % | 16 |

Note 4. Ta=60 °C

Note 5. The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

Note 6. The image area is divided into 10×10 segments. The voltage of a segment is the average of output voltage from all the pixels within the segment.

PRNU is defined by $(V_{max} - V_{min})/V_o$, where V_{max} and V_{min} are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage V_o is 150 mV.

Note 7. The image area is divided into 10×10 segments. The saturation signal is defined as the minimum of each segment's voltage which is the average of output voltage from all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.

Note 8. The average output voltage under a non-exposure condition.

Note 9. The image area is divided into 10×10 segments.

DSNU is defined by $(V_{dmax} - V_{dmin})$ under the non-exposure condition where V_{dmax} and V_{dmin} are the maximum and the minimum values of each segment's voltage, respectively that is the average output voltage over all pixels in the segment.

Note 10. The average output voltage when a 1 000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.

Note 11. The sensor is adjusted to position a V/10 square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/10 square.

Note 12. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.

Note 13. The sensor is adjusted to position a V/10 square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.

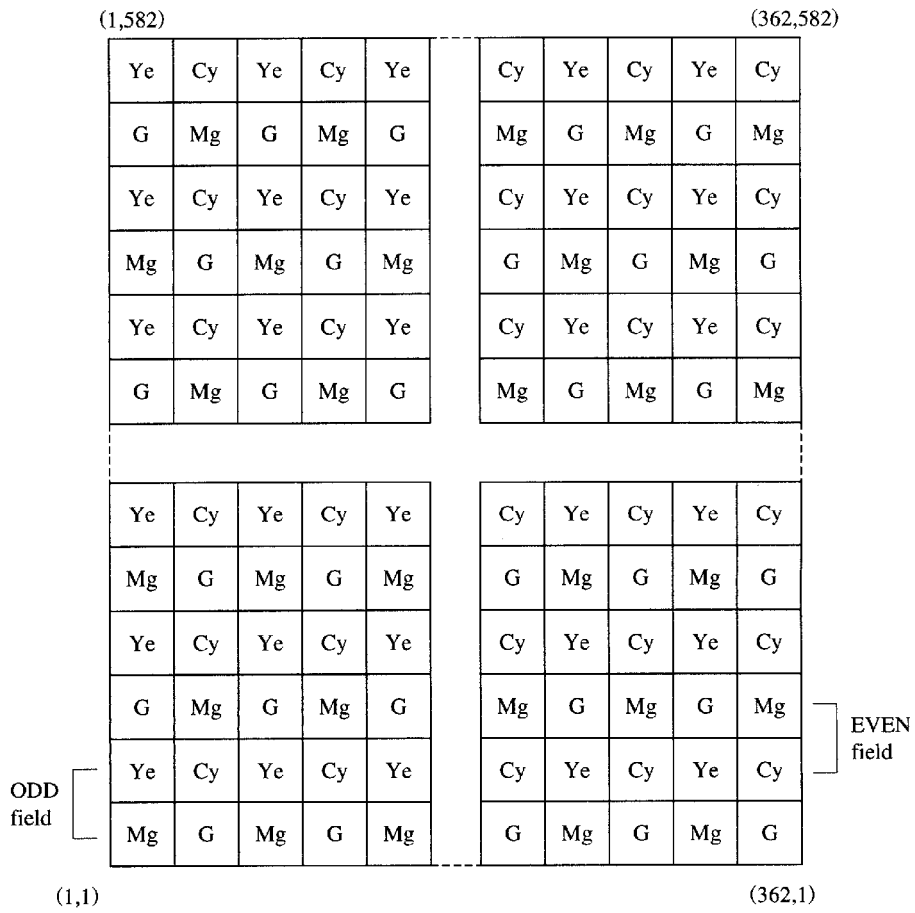
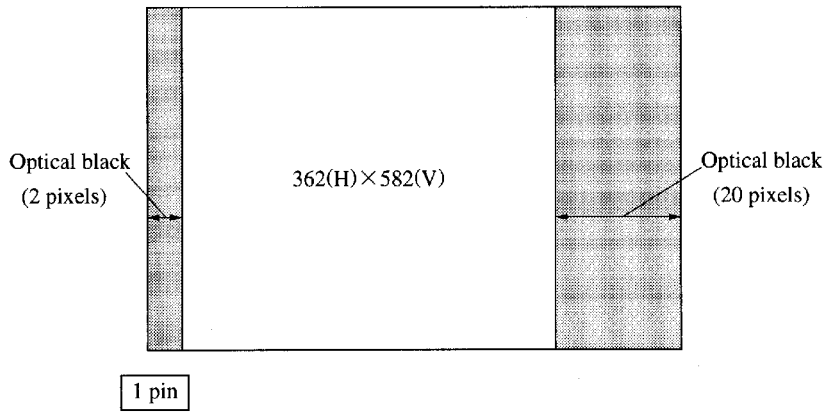
Note 14. Observed with a vector scope when the color bar chart is imaged under the standard exposure condition.

Note 15. The difference between the average output voltage of the (Mg + Ye), (G + Cy) line and the (Mg + Cy), (G + Ye) line under the standard exposure condition.

Note 16. The difference between the average output voltage of the odd field and the even field.

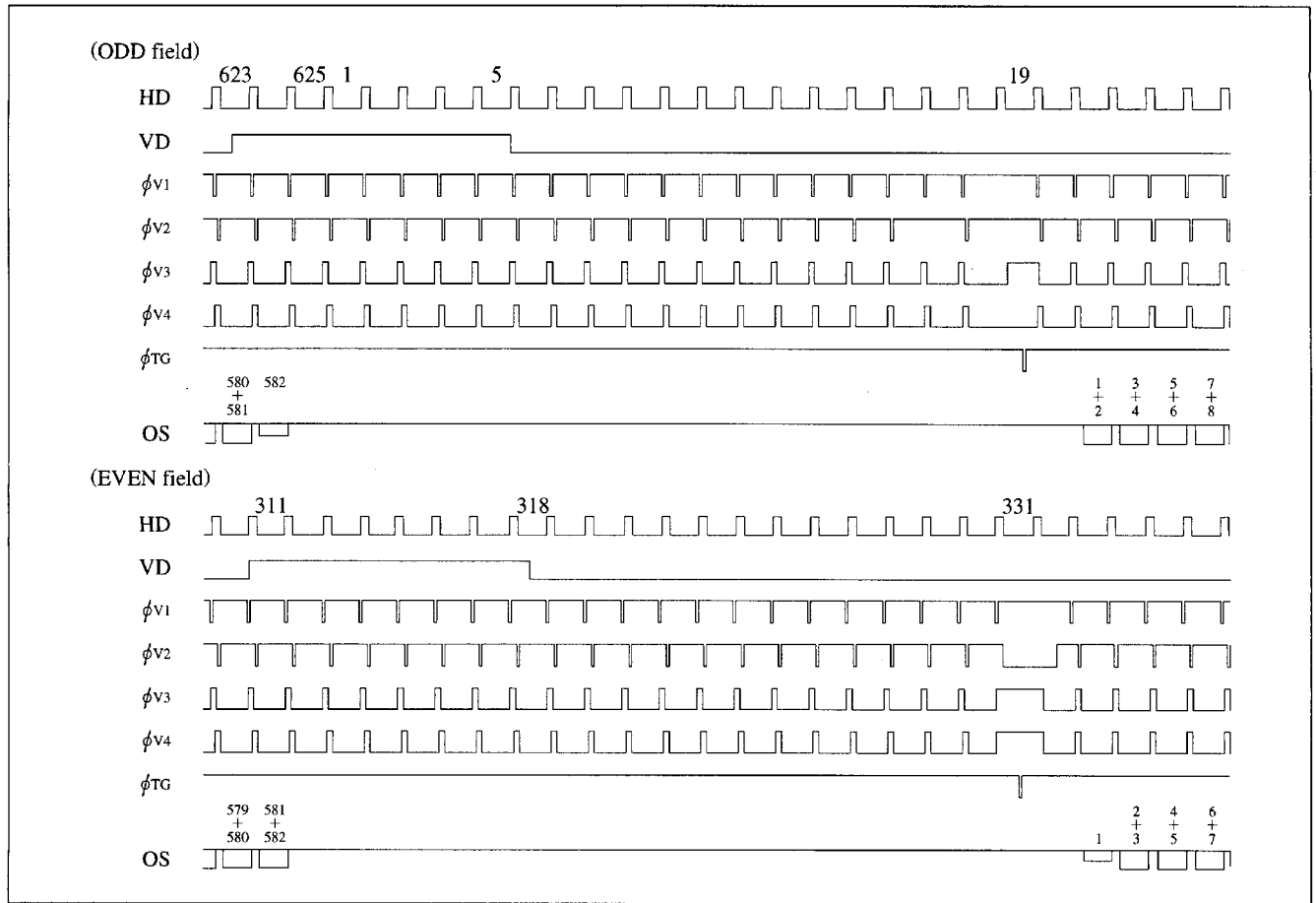
※ The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.

■ Composition of Pixels and Arrangement of Color Filters

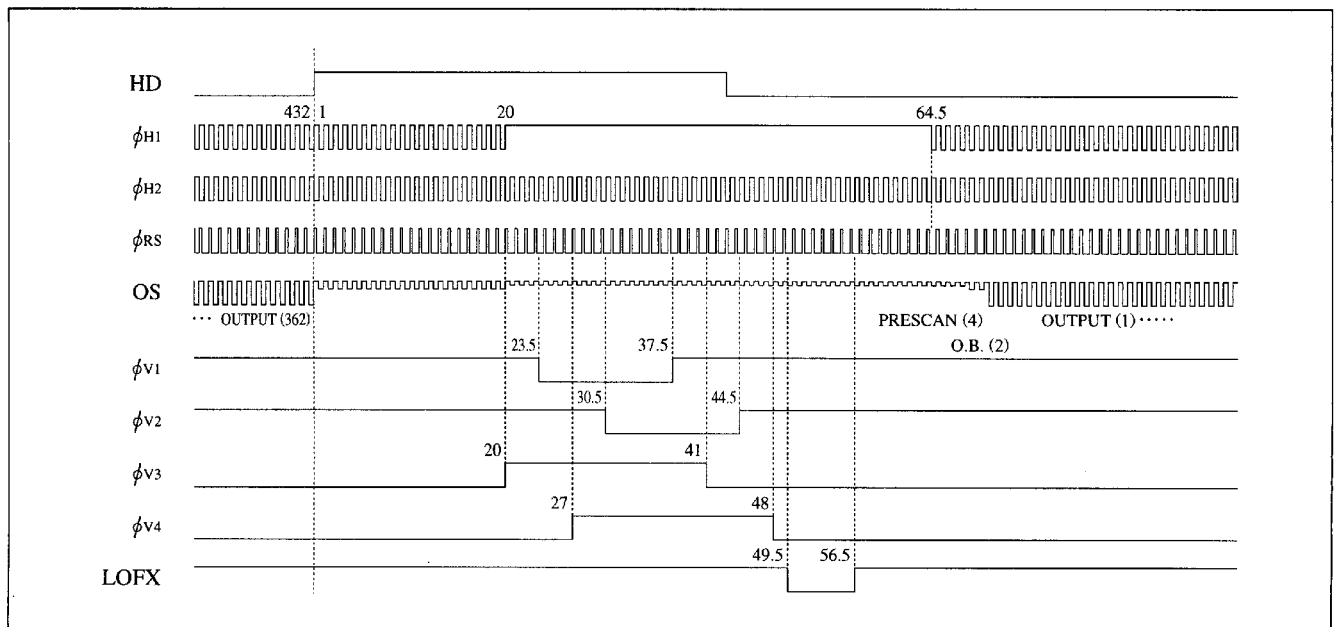


■ Timing Diagram

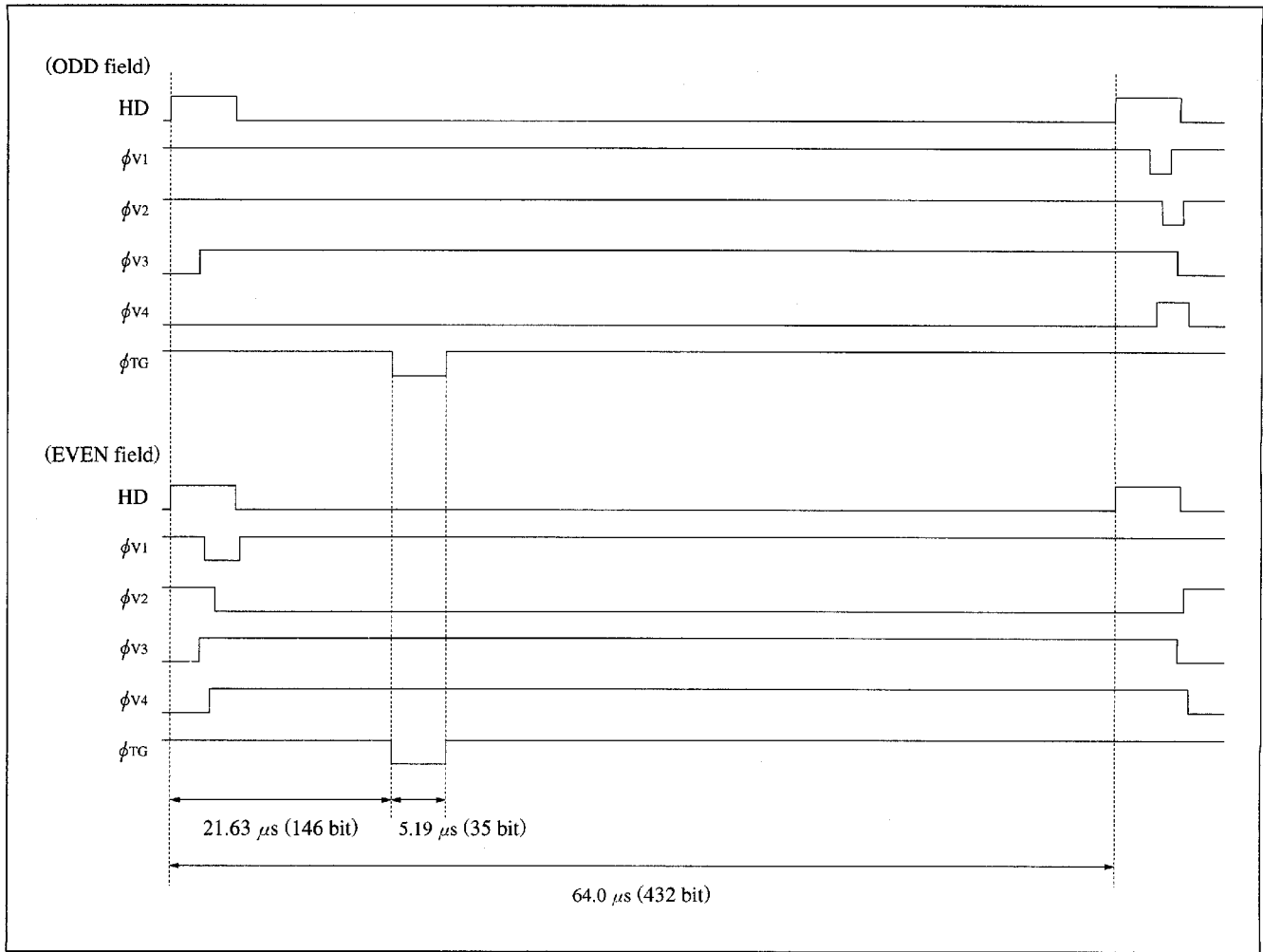
(1) Vertical Transfer Timing



(2) Horizontal Transfer Timing



(3) Read Out Timing



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