GOULD

AMI • Semiconductors

Asynchronous Communication Interface Adapter

S6551/S6551A

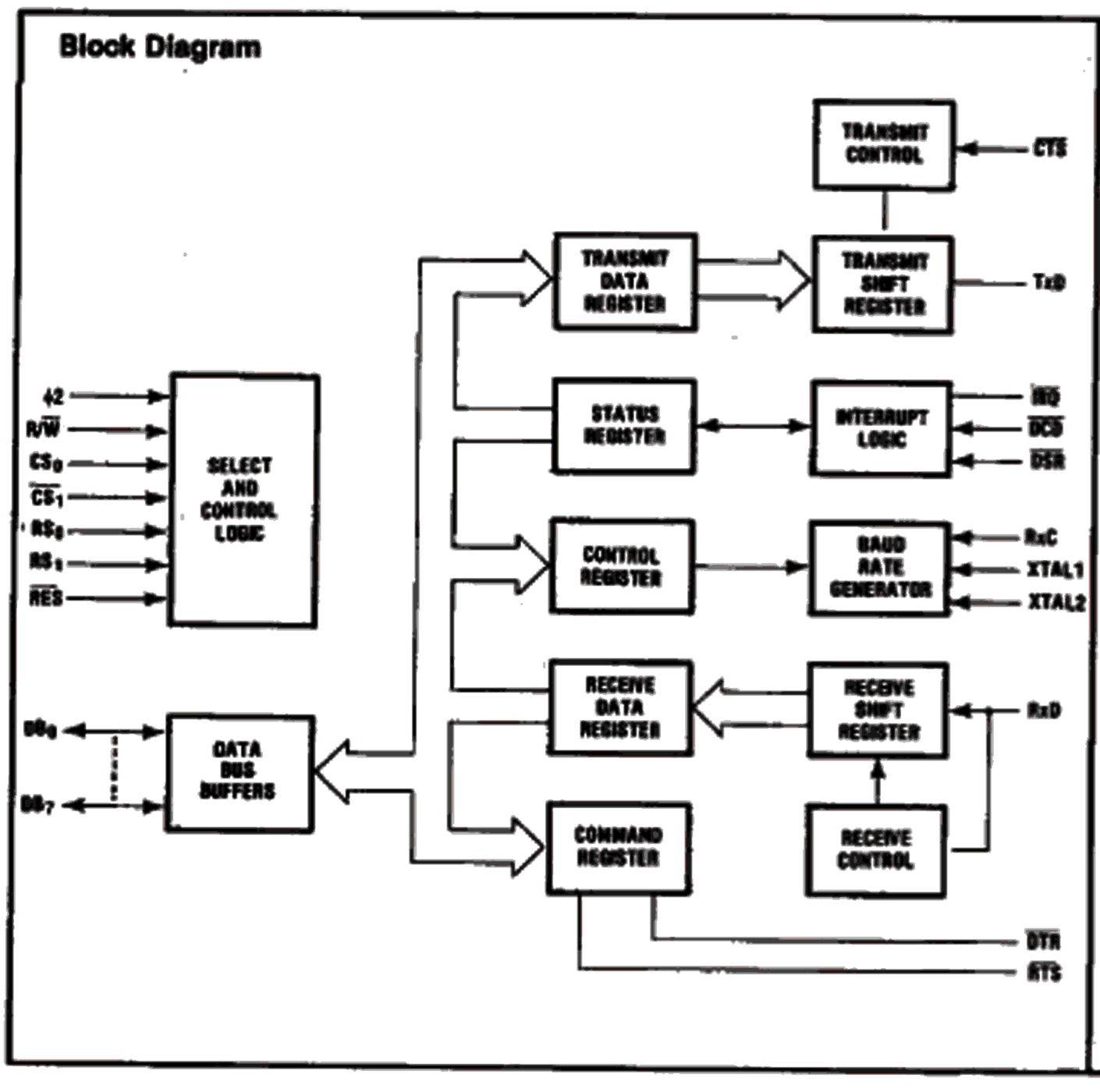
Features

- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single +5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16X Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

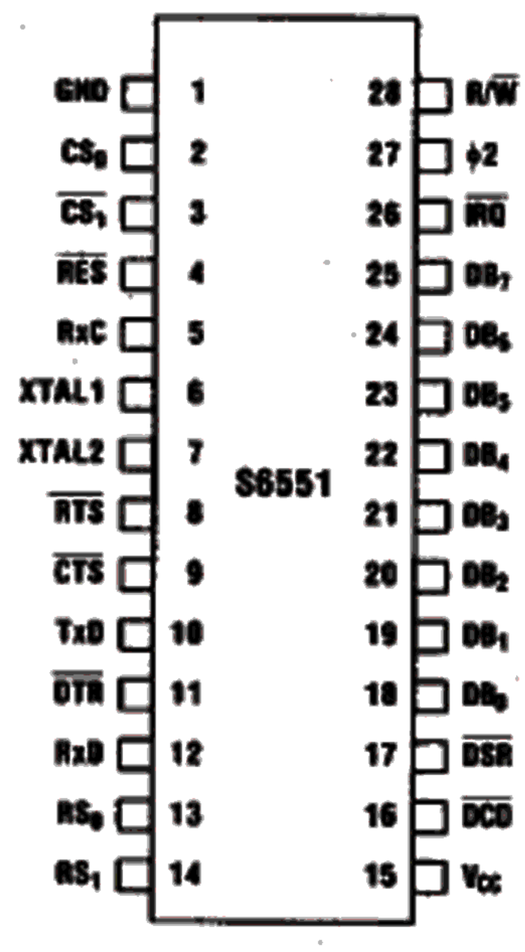
General Description

The S6551/S6551A is an Asynchronous Communication Adapter (ACIA) intended to provide interfacing for the microprocessors to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3V to +7.0V
Input/Output Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{IN}	Input Leakage Current: V_{IN} = 0 to 5V (ϕ2, R/W, RES, CS_0, CS_1, RS_0, RS_1, CTS, RxD, DCD, DSR)	—	±1.0	±2.5	μA
I_{TSI}	Input Leakage Current for High Impedance State (Three State)	—	±2.0	±10.0	μA
V_{OH}	Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, TxD, RxC, RTS, DTR)	2.4	—	—	V
V_{OL}	Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, RTS, DTR, IRQ)	—	—	0.4	V
I_{OH}	Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, TxD, RxC, RTS, DTR)	—	—	−100	μA
I_{OL}	Output Low Current (Sinking): V_{OL} = 0.4V (DB_0-DB_7, TxD, RxC, RTS, DTR, IRQ)	—	—	1.6	mA
I_{OFF}	Output Leakage Current (Off State): V_{OUT} = 5V (IRQ)	—	1.0	10.0	μA
C_{CLK}	Clock Capacitance (ϕ2)	—	—	20	pF
C_{IN}	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF
C_{OUT}	Output Capacitance	—	—	10	pF
P_D	Power Dissipation (See Graph) (T_A = 0°C)	—	170	300	mW

Write Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, unless otherwise noted)

		S6551		S6551A		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	ϕ2 Pulse Width	400	—	200	—	ns
t_{ACW}	Address Set-Up Time	120	—	70	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	150	—	60	—	ns
t_{HW}	Data Bus Hold Time	20	—	20	—	ns

(t_r and t_f = 10 to 30ns)

Figure 1. Power Dissipation vs. Temperature

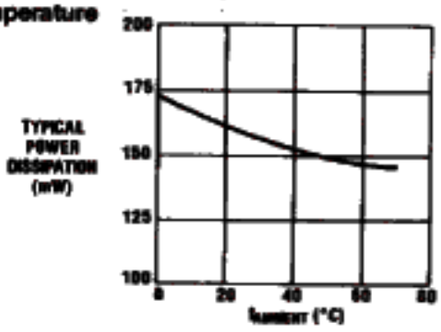
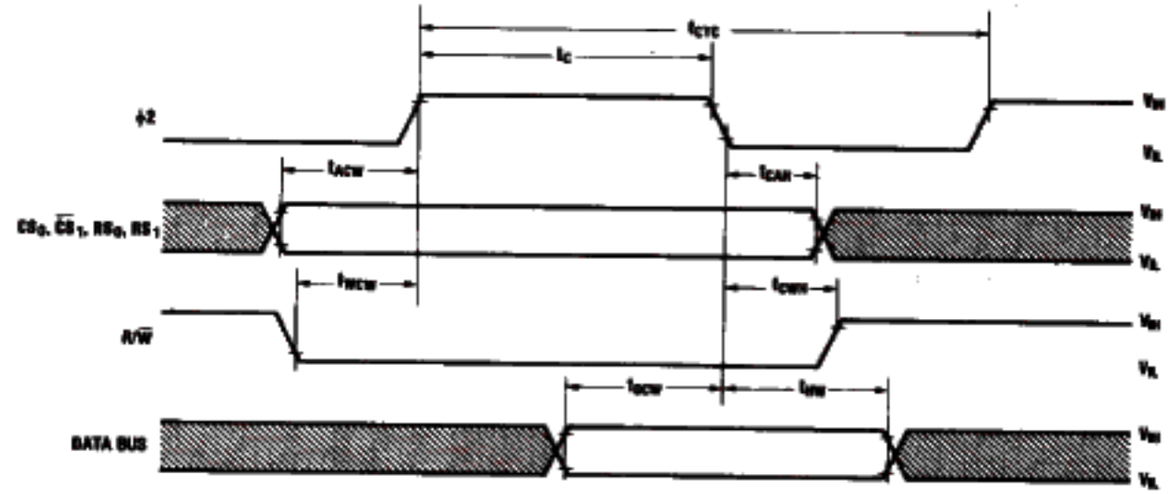


Figure 2. Write Timing Characteristics



Read Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, unless otherwise noted)

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	ϕ2 Pulse Width	400	—	200	—	ns
t_{ACR}	Address Set-Up Time	120	—	70	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	200	—	150	ns
t_{HR}	Read Hold Time	20	—	20	—	ns
t_{CDA}	Bus Active Time (Invalid Data)	40	—	40	—	ns

Figure 5. Test Load for Data Bus (DB_0–DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS Outputs

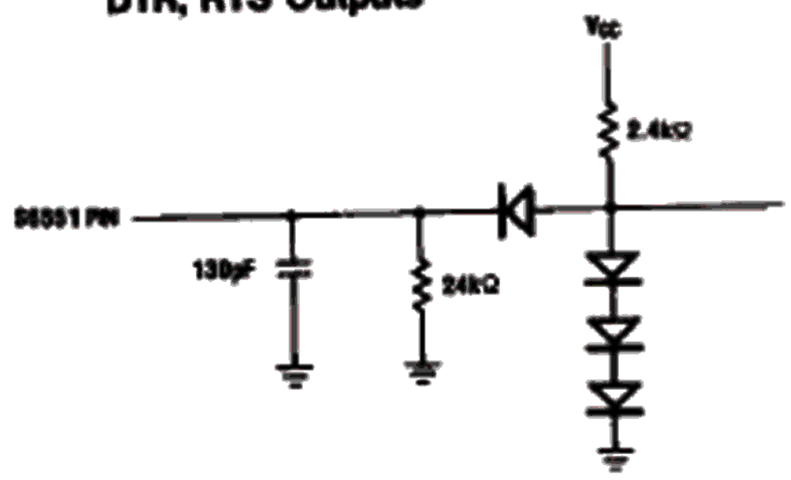


Figure 6a. Interrupt and Output Timing

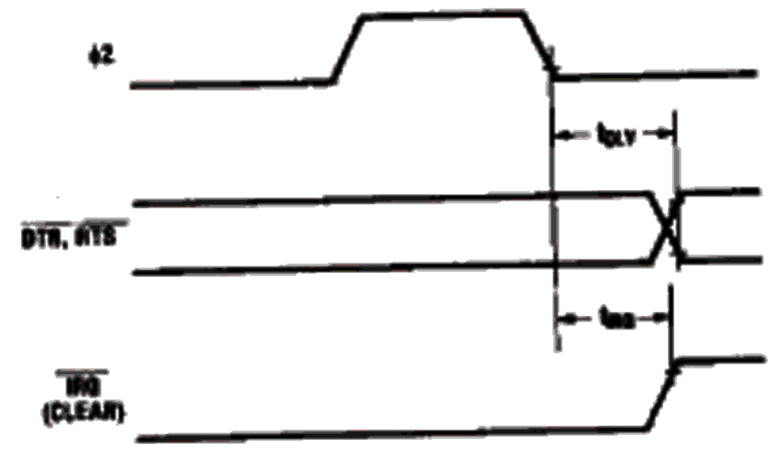


Figure 6b. Transmit Timing with External Clock

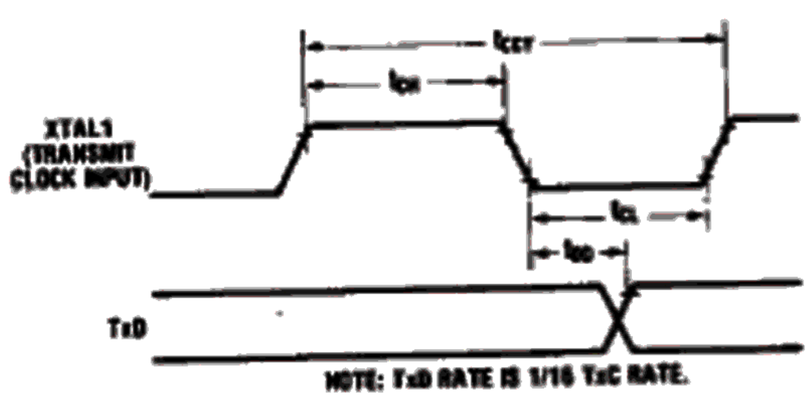


Figure 6c. Receive External Clock Timing

Pin Description

$\overline{RES}$ (Reset). During system initialization a low on the RES input will cause internal registers to be cleared.

ϕ2 Input Clock. The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the S6551.

R/$\overline{W}$ (Read/Write). The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6551. A low on the R/$\overline{W}$ pin allows a write to the S6551.

$\overline{IRQ}$ (Interrupt Request). The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0–DB_7 (Data Bus). The DB_0–DB_7 pins are the eight data lines used for transfer of data between the processor and the S6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0–$\overline{CS_1}$ (Chip Selects). The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The S6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects). The two register select lines are normally connected to the processor address lines to allow the processor to select the various S6551 internal registers. The following table indicates the internal register select coding:

Table 1

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the S6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these diferences are described in the individual register definitions.

Figure 3. Clock Generation

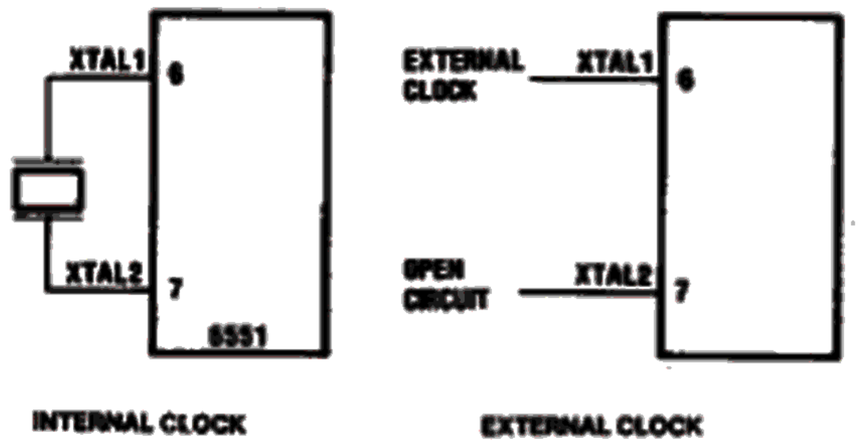
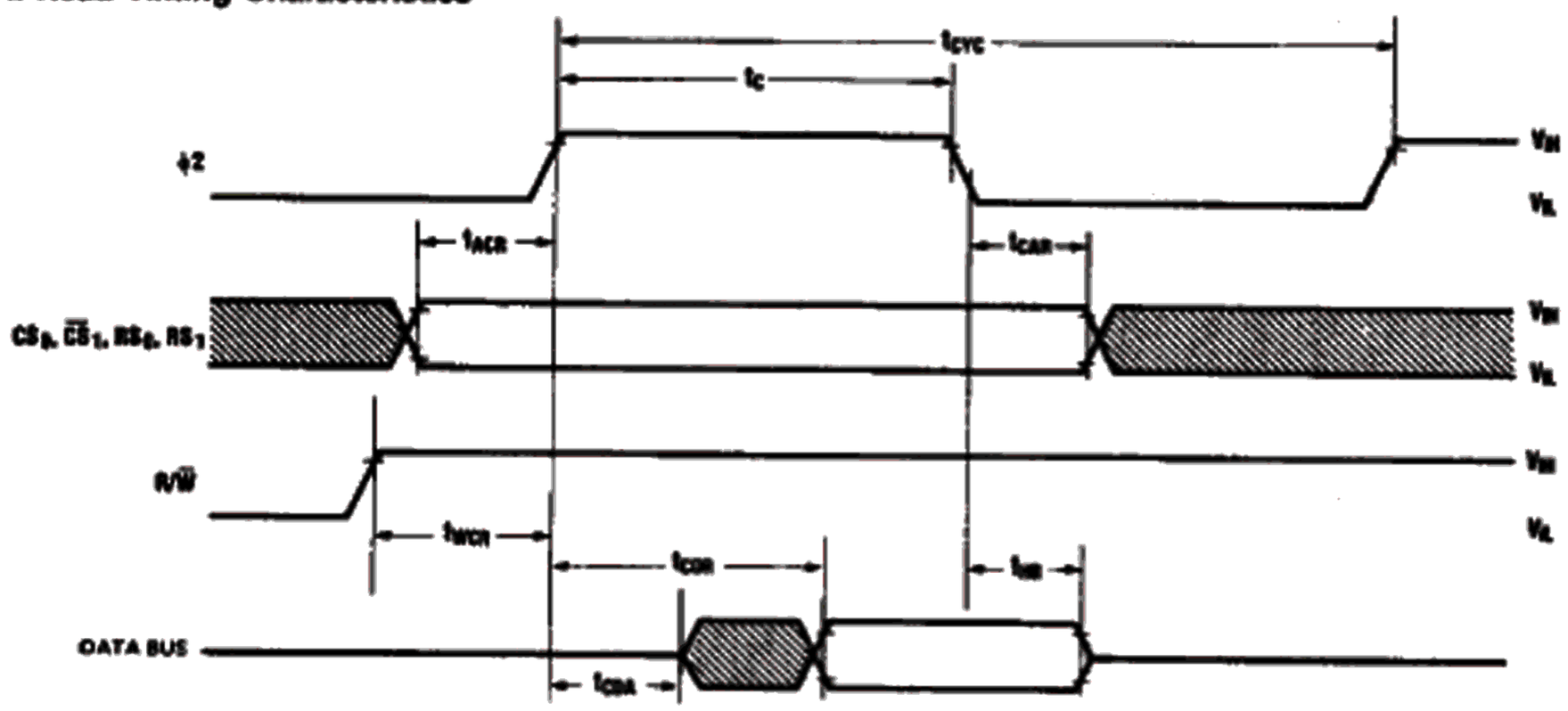


Figure 4. Read Timing Characteristics



Transmit/Receive Characteristics

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Transmit/Receive Clock Rate	400*	—	400*	—	ns
t_{CH}	Transmit/Receive Clock High Time	175	—	175	—	ns
t_{CL}	Transmit/Receive Low Time	175	—	175	—	ns
t_{DD}	EXTAL1 to TxD Propagation Delay	—	500	—	500	ns
t_{DLY}	Propagation Delay ($\overline{RTS}$, DTR)	—	500	—	500	ns
t_{IRQ}	$\overline{IRQ}$ Propagation Delay (Clear)	—	500	—	550	ns

(t_r and t_f = 10 to 30ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

XTAL1, XTAL2 (Crystal Pins). These pins are normally directly connected to the external crystal (1.8432MHz M-Tron MP-2 recommended) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data). The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data). The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock). The RxC is a bi-directional pin which serves as either the receiver 16xclock input or the receiver 16xclock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send). The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

CTS (Clear to Send). The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready). This output pin is used to indicate the status of the S6551 to the modem. A low on $\overline{\text{DTR}}$ indicates the S6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready). The $\overline{\text{DSR}}$ input pin is used to indicate to the S6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{\text{DSR}}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{\text{DSR}}$ occurs, $\overline{\text{IRQ}}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{\text{DSR}}$ does not affect either Transmitter or Receiver operation.

$\overline{\text{DCD}}$ (Data Carrier Detect). The $\overline{\text{DCD}}$ input pin is used to indicate to the S8551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{\text{DCD}}$, like $\overline{\text{DSR}}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{\text{DCD}}$ occurs, $\overline{\text{IRQ}}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{\text{DCD}}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Figure 7. Transmitter/Receiver Clock Circuits

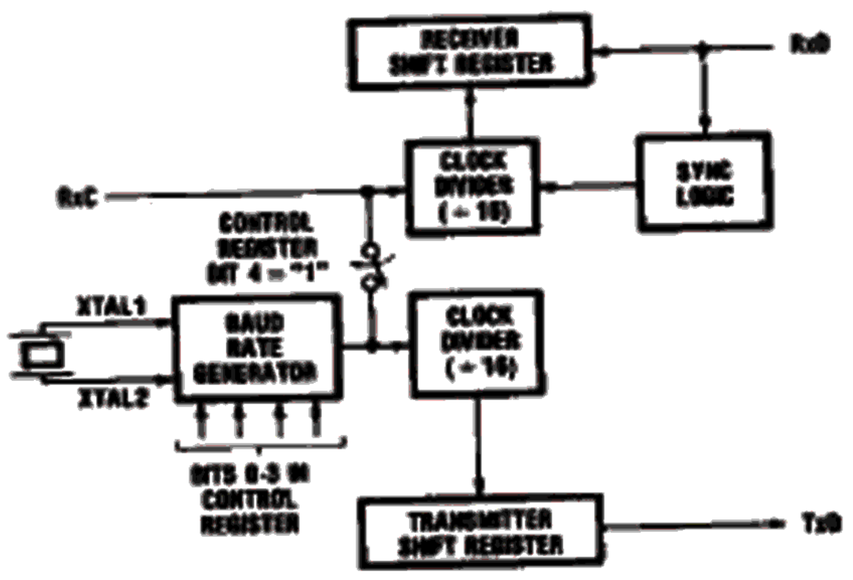
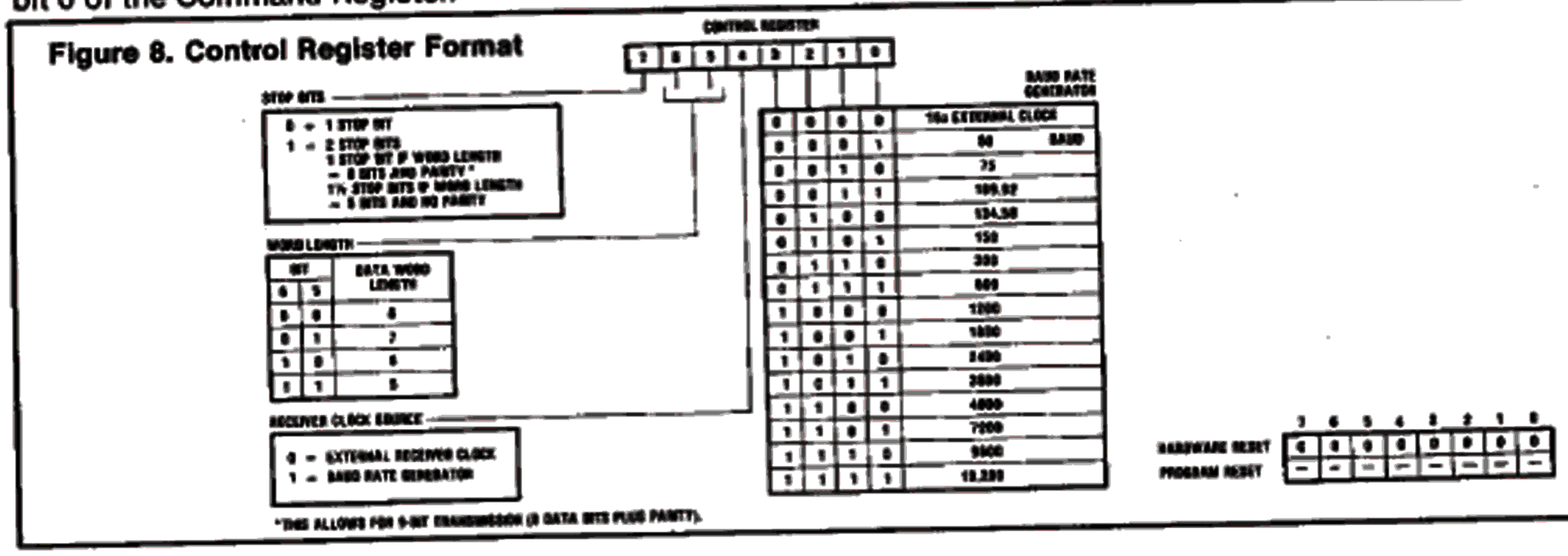


Figure 8. Control Register Format



Internal Organization

The Transmitter/Receiver sections of the S6551 are depicted by the block diagram in Figure 7.

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the S6551.

Control Register

The Control Register is used to select the desired mode for the S6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 8.

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 9.

Figure 9. Command Register Format

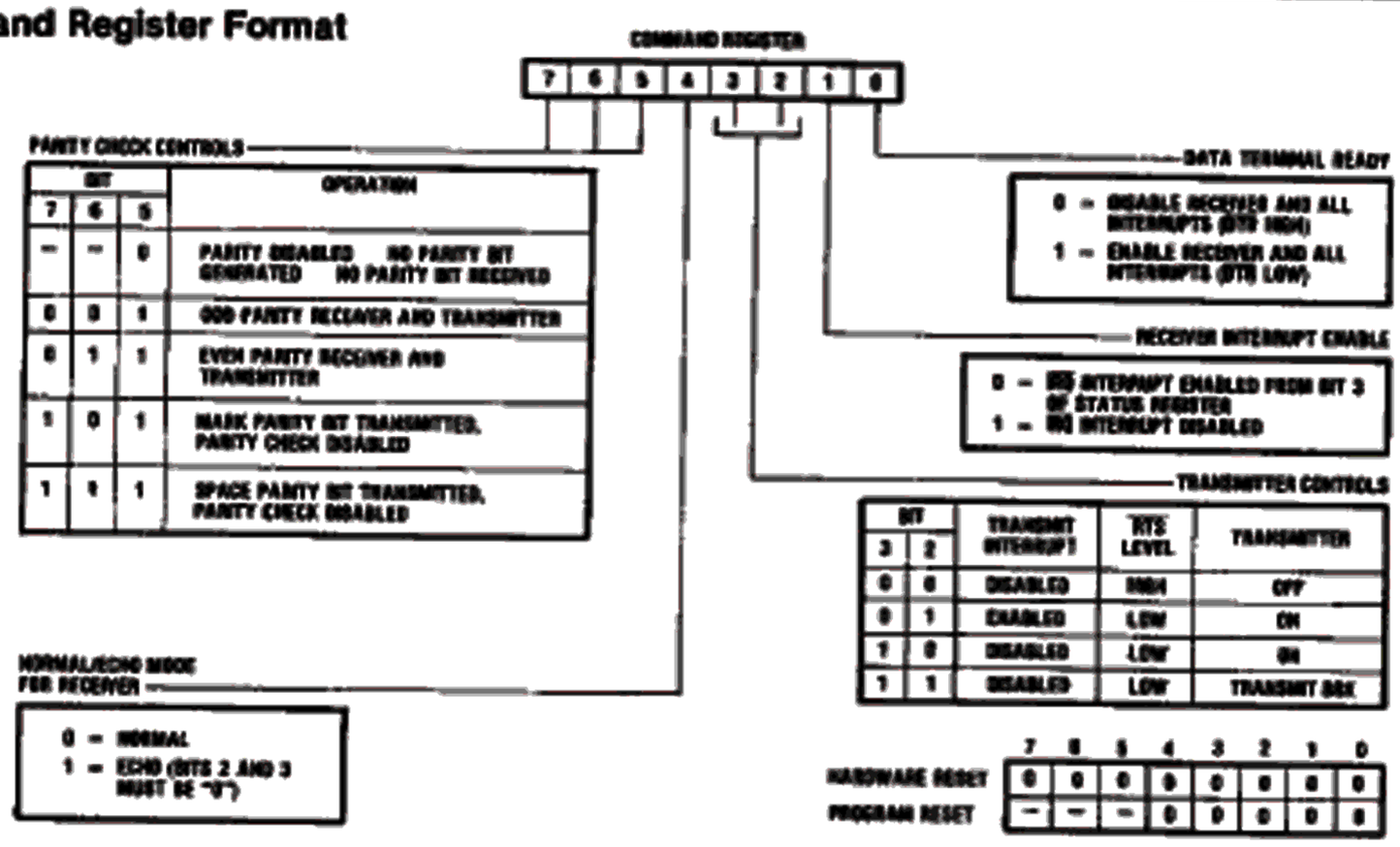
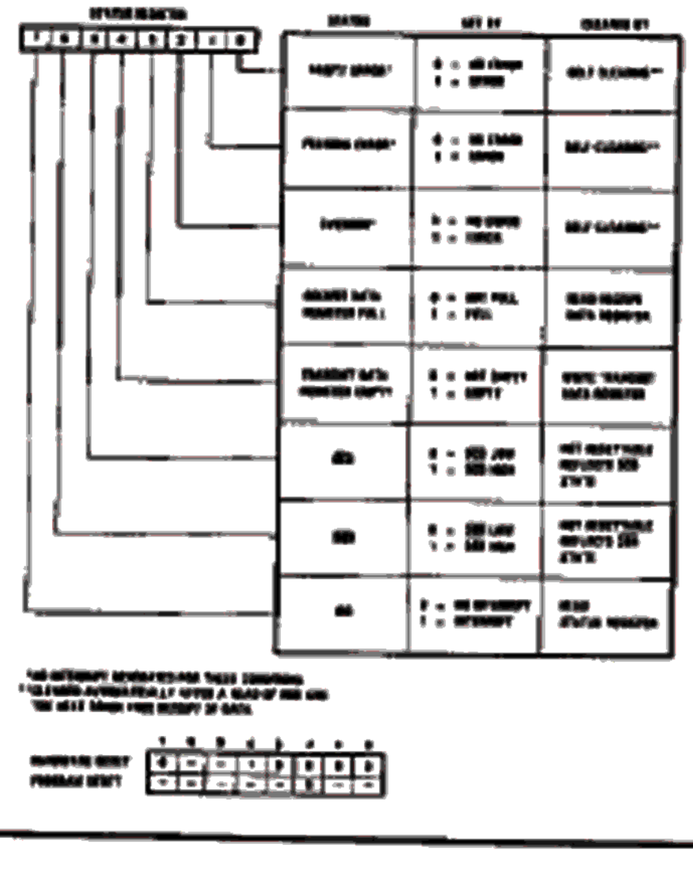


Figure 10. Status Register Format



Status Register

The Status Register is used to indicate to the processor the status of various S6551 functions and is outlined in Figure 10.

Transmit and Receive Data Registers

These registers are used as temporary data storage for the S6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 11 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

Figure 11. Serial Data Stream Example