64M-Bit (4Mx16 /2Mx32) Synchronous MASKROM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Address: Row address: RA_0 ~ RA_{12}
  Column address: CA_0 ~ CA_7 (x32): CA_0 ~ CA_8 (x16)
- Switchable organization
  4,194,304 x 16(word mode) /
  2,097,152 x 32(double word mode)
- All inputs are sampled at the rising edge of the system clock
- Read Performance at memory point of view
  @33MHz 4-1-1-1 (RAS Latency=1, CAS Latency=3)
  @50MHz 5-1-1-1 (RAS Latency=1, CAS Latency=4)
  @66MHz 5-1-1-1 (RAS Latency=1, CAS Latency=4)
  @83MHz 7-1-1-1 (RAS Latency=2, CAS Latency=5)
  @100MHz 7-1-1-1 (RAS Latency=2, CAS Latency=5)
- t_{SAC} : 6ns
- Default mode by user requirement
- MRS cycle with address key programs
  -. RAS Latency(1 & 2)
  -. CAS Latency(3 ~ 6)
  -. Burst Length : 4, 8
  -. Burst Type : Sequential & Interleaved
- DQM for data-out masking
- Package :86TSOP2 - 400

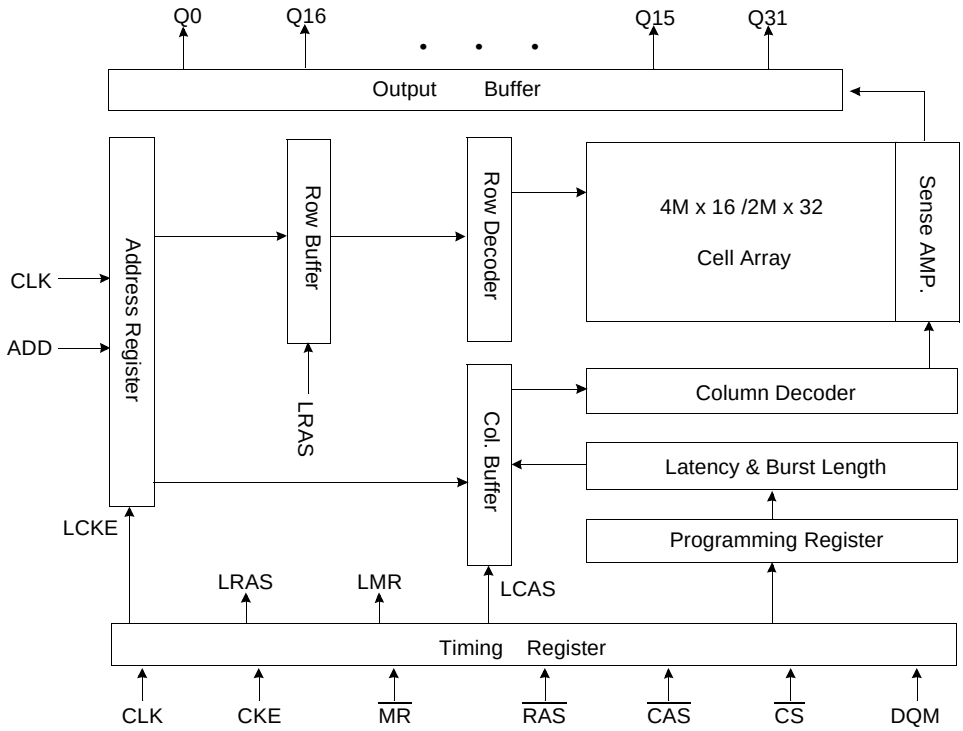
GENERAL DESCRIPTION

The K3S7V2000M-TC is a synchronous high bandwidth mask programmable ROM fabricated with SAMSUNG′s high performance CMOS process technology and is organized either as 4,194,304 x16bit(word mode) or as 2,097,152 x32bit(double word mode) depending on polarity of $\overline{WORD}$ pin.(see pin function description). Synchronous design allows precise cycle control, with the use of system clock, I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	MAX Freq.	Interface	Package
K3S7V2000M-TC10	100MHz	LVTTL	86TSOP2
K3S7V2000M-TC12	83MHz		
K3S7V2000M-TC15	66MHz		
K3S7V2000M-TC20	50MHz		
K3S7V2000M-TC30	33MHz		

FUNCTIONAL BLOCK DIAGRAM



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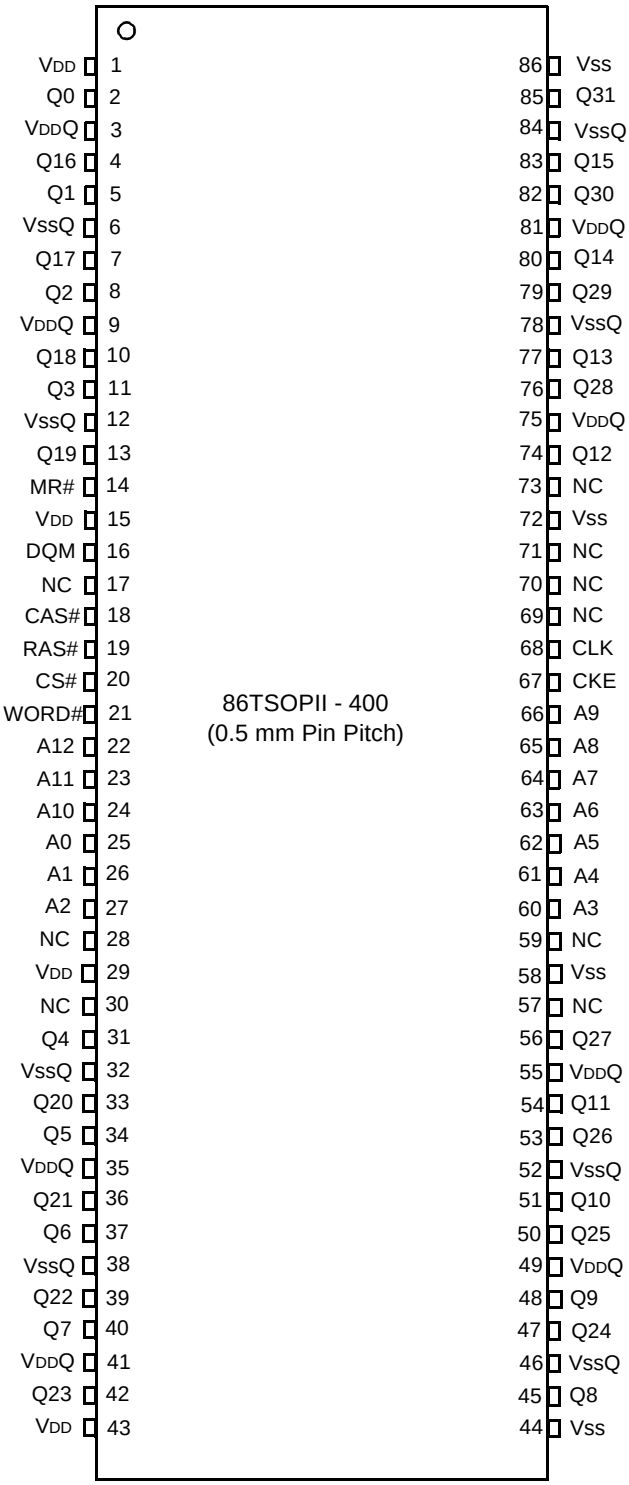
PIN CONFIGURATION (TOP VIEW)



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the rising edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK and CKE.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby mode.
A_0 ~ A_{12}	Address	Row / Column addresses are multiplexed on the same pins. Row address: RA_0 ~ RA_{12}, Column address: CA_0 ~ CA_7 (x32): CA_0 ~ CA_8 (x16)
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the rising edge of the CLK with $\overline{RAS}$ low. Enables row access
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the rising edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{MR}$	Mode Register Set	Enables mode register set with $\overline{MR}$ low. (Simultaneously $\overline{CS}$,$\overline{RAS}$ and $\overline{CAS}$ are low)
Q_0 ~ Q_{31}	Data Output	
V_{DD}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
$V_{DD}Q/V_{SS}Q$	Data Output Power/ Ground	Power and ground for the output buffers.
$\overline{WORD}$	x32/x16 Mode Selection	Double word mode/word mode, depending on polarity of $\overline{WORD}$ pin. Should be set before $\overline{CAS}$ enabling.
DQM	Data-out Masking	It works similar to $\overline{OE}$ during read operation.
N.C	No Connection	This pin is recommended to be left No Connection on the device.

Note1. V_{DD} and $V_{DD}Q$ is same voltage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on V_{DD} Relative to Vss	V_{DD}, $V_{DD}Q$	-0.5	4.6	V
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5	V_{DD} + 0.5≤4.6	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{STG}	-55	125	°C
Short circuit current	I_{OS}	-	50	mA
Power Dissipation	P_D	-	1	W

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.

DC OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, $V_{DD}Q$	3.0	3.3	3.6	V
Supply Voltage(Ground)	V_{SS},$V_{SS}Q$	0	0	0	V

DC CHARACTERISTICS

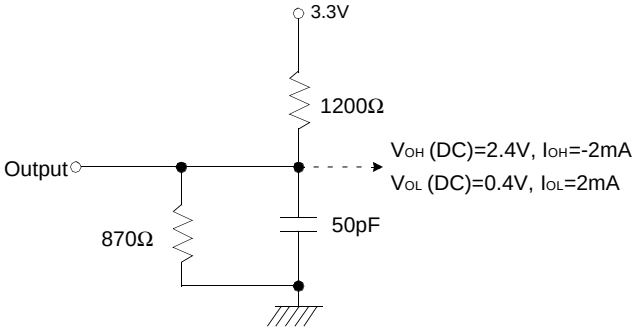
Parameter	Symbol	Min	Max	Unit	Test Condition
Standby Current (Note3)	I_{CC3P}	-	150	uA	CKE≤V_{IL}(Max), t_{CC}=Min
	I_{CC3PS}	-	150	uA	CKE=0, t_{CC}=Min
Active Standby Current	I_{CC3N}	-	50	mA	$\overline{CS}$≥V_{IH}(Min), t_{CC}=Min, All Outputs Open
Burst Mode Operating Current	I_{CC4}	-	100	mA	t_{CC}=Min, All Outputs Open
Input Leakage Current	I_{IL}	-10	10	uA	0V≤V_{IN}≤V_{DD} + 0.3V Pins not under test=0V
Output Leakage Current (Dout Disabled)	I_{OL}	-10	10	uA	(0V≤V_{OUT}≤V_{DD} Max) Q# in High-Z
Input High Voltage, All Inputs	V_{IH}	2.0	V_{DD} + 0.3	V	(Note1)
Input Low Voltage, All Inputs	V_{IL}	-0.3	0.8	V	(Note2)
Output High Voltage Level (Logic 1)	V_{OH}	2.4	-	V	I_{OH}=-2mA
Output Low Voltage Level (Logic 0)	V_{OL}	-	0.4	V	I_{OL}=2mA

Note : 1. V_{IH}(Max)=4.6V for pulse width≤10ns acceptable, pulse width measured at 50% of pulse amplitude.
2. V_{IL}(Min)=-1.5V for pulse width≤10ns acceptable, pulse width measured at 50% of pulse amplitude.
3. The condition is the same as Self Refresh Mode of SDRAM, that is, in this case $\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$ have to be set to Low, $\overline{MR}$ has to be set to High.

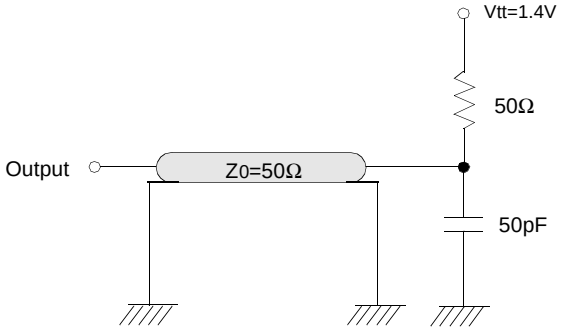
AC OPERATING TEST CONDITIONS (T_A = 0 to 70°C, V_{DD} = 3.3V±0.3V, unless otherwise noted.)

Parameter	Value
Timing Reference Levels of Input/Output Signals	1.4V
Input Signal Levels	V_{IH}/V_{IL}=2.4V/0.4V
Transition Time (Rise & Fall) of Input Signals	tr/tf=1ns/1ns
Output Load	LVTTL

Note : If CLK transition time is longer than 1ns, timing parameters should be compensated. Add [(tr+tf)/2-1]ns for transition time longer than 1ns. Transition time is measured between V_{IL}(Max) and V_{IH}(Min).



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETERS

(AC operating conditions unless otherwise noted)

Parameter	Symbol	up to 100MHz		up to 83MHz		up to 66MHz		up to 50 Mhz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CLK Cycle Time	t_{CC}	10		12		15	-	20	-	ns	
CLK to Valid Output Delay	t_{SAC}	-	6	-	6	-	6	-	6	ns	
Data Output Hold Time	t_{OH}	2	-	2	-	2	-	2	-	ns	
CLK High Pulse Width	t_{CH}	3	-	3.5	-	4	-	6.5	-	ns	
CLK Low Pulse Width	t_{CL}	3	-	3.5	-	4	-	6.5	-	ns	
Row-active to Row-active	t_{RC}	10	-	10	-	8	-	8	-	clks	1
Input Setup Time	t_{SS}	2	-	3	-	4	-	4	-	ns	
Input Hold Time	t_{SH}	1	-	1	-	2	-	2	-	ns	
CLK to Output in Low-Z	t_{SLZ}	0	-	0	-	0	-	0	-	ns	
CLK to Output in High-Z	t_{SHZ}	-	7	-	8	-	10	-	15	ns	
Transition Time	t_T	0.1	10	0.1	10	0.1	10	0.1	10	ns	
Valid CAS Enable to Valid CAS Enable	t_{VCVC}	8	-	8	-	7	-	7	-	clks	2

Note :

1. These t_{RC} values are for BL=8. For BL=4, t_{RC}=6 clks for up to 100MHz, t_{RC}=6 clks for up to 83MHz, t_{RC}=4 clks for up to 66MHz, t_{RC}=4 clks for up to 50MHz, and t_{RC}=3 clks for up to 33MHz.
   RAS latency increase means, a simultaneous t_{RC} increase in the same number of cycles.
   (If RAS latency is 3 clks, t_{RC} is 12 clks for BL=8.) Refer to attached technical note for gapless operation.
2. These t_{VCVC} values are for BL=8. For BL=4, t_{VCVC}=4clks for up to 100MHz, t_{VCVC}=4clks for up to 83MHz, t_{VCVC}=3clks for up to 66MHz, t_{VCVC}=3clks for up to 50MHz, and t_{VCVC}=2clks for up to 33MHz.
   Refer to attached technical note for gapless operation.

CAPACITANCE(T_A=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance	C_{IN}	-	5	pF
Output Capacitance	C_{OUT}	-	7	pF

FUNCTION TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$	DQM	Add.	$\overline{WORD}$	Notes
Register	Mode Register Set		H	X	L	L	L	L	X	Code	X	1
Row Active Row Access& Latch	Row Access & Latch		H	X	L	L	H	H	X	RA	X	
Read	Column Access & Latch		H	X	L	H	L	H	X	CA	X	
Burst Stop	(Burst Stop on Synch.DRAM)		H	X	L	H	H	L	X	X	X	
	(Precharge on Synch.DRAM)		H	X	L	L	H	L	X	X	X	
Power Down & Clock Suspend	Two Standby Mode	Entry	H	L	X	X	X	X	X	X	X	2
		Exit	L	H	X	X	X	X	X	X	X	
DQM			H	X					V	X		3
Illegal	(Write on Synch.DRAM)		H	X	L	H	L	L	X	CA	X	
	(Refresh on Synch.DRAM)		H	X	L	L	L	H	X	X	X	
No Operation Command			H	X	H	X	X	X	X	X	X	4
			H	X	L	H	H	H	X	X	X	
Organization Control			H	X	L	H	L	H	X	CA	H	5
											L	

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)
Abbreviations (RA: Row Address, CA: Column Address, NOP: No Operation Command, DWM: Double Word Mode, WM: Word Mode)

Notes :

1. A_0 ~ A_6: Program keys (@MRS). After power up, mode register set, can be set before issuing other input command. After the mode register set command is completed, no new commands can be issued for 3 CLK Cycles, and $\overline{CS}$ or $\overline{MR}$ state must be defined "H" within 3 CLK cycles. Refer to the Mode Register Field Table
2. In the case CKE is low, two standby modes are possible. Those are stand-by mode in power-down.
   Power Down: CKE="L" (at all the parts except the range of Row Active, Read & Data out)
   Clock Suspend: CKE="L" (at the range of Row Active, Read & Data Out)
3. DQM sampled at rising edge of a CLK makes a Hi-Z state the data-out state, delayed by 2CLK cycles.
4. Precharge command on Synch.DRAM can be used for Burst Stop operation during burst read operation only.
5. Mode selection control is decided simultaneously with column access start, and according to the polarity of $\overline{WORD}$ pin, "H" state is DWM, "L" state is WM.

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A6	A5	A4	A3	A2	A1	A0
Function	RAS Latency	CAS Latency			Burst Type	Burst Length	

RAS Latency		CAS Latency				Burst Type		Burst Length		
A6	Length	A5	A4	A3	Length	A2	Type	A1	A0	Length
0	1	0	0	0	Reserved	0	Sequential	0	0	Reserved
1	2	0	0	1	Reserved	1	Interleave	0	1	4
		0	1	0	3			1	0	8
		0	1	1	4			1	1	Reserved
		1	0	0	5					
		1	0	1	6					
		1	1	0	Reserved					
		1	1	1	Reserved					

Notes :
-. After power up, when user wants to change mode register set, user must exit from power down mode and start mode register set before entering normal operation mode.

ADDRESSING MAP

(1) $\overline{\text{WORD}}$ = "H" : x32 Organization

Function	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
Row Address	RA_0	RA_1	RA_2	RA_3	RA_4	RA_5	RA_6	RA_7	RA_8	RA_9	RA_{10}	RA_{11}	RA_{12}
Column Address	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6	CA_7[Note]	X	X	X	X	X

Note : Column Address MSB (at x32 organization) (X=Don't Care)

(2) $\overline{\text{WORD}}$="L" : x16 Organization

Function	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
Row Address	RA_0	RA_1	RA_2	RA_3	RA_4	RA_5	RA_6	RA_7	RA_8	RA_9	RA_{10}	RA_{11}	RA_{12}
Column Address	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6	CA_7	CA_8[Note]	X	X	X	X

Note : Column Address MSB (at x16 organization) (X=Don't Care)

(3) Each address is arranged as follows

for X32 operation,

	MSB												LSB
Address Register	AR20	AR19	AR18	...	AR9	AR8	AR7	AR6	...	AR3	AR2	AR1	AR0
Address	RA12	RA11	RA10	...	RA1	RA0	CA7	CA6	...	CA3	CA2	CA1	CA0

* Initial Address
- BL=4(CA0,CA1)
- BL=8(CA0,CA1,CA2)

BL=4

BL=8

for X16 operation,
when CA8 is set to Low, data belonging to 0~15th registers are output to Q0~Q15 pins, and when CA8 is set to High, data belonging to16~31th registers are output to Q0~Q15 pins.

x32 operation (double word mode)

Column Address								D15 ~ D0 (Hexadecimal)				D31 ~ D16 (Hexadecimal)			
CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0								
0	0	0	0	0	0	0	0	A	A	A	A	0	0	0	0
0	0	0	0	0	0	0	1	B	B	B	B	1	1	1	1
0	0	0	0	0	0	1	0	C	C	C	C	2	2	2	2
0	0	0	0	0	0	1	1	D	D	D	D	3	3	3	3
0	0	0	0	0	1	0	0	E	E	E	E	4	4	4	4
0	0	0	0	0	1	0	1	F	F	F	F	5	5	5	5

x16 operation (word mode)

Column Address									Data Out (Hexadecimal)				Comment
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0					
0	0	0	0	0	0	0	0	0	A	A	A	A	D15 ~ D0
0	0	0	0	0	0	0	0	1	B	B	B	B	D15 ~ D0
0	0	0	0	0	0	0	1	0	C	C	C	C	D15 ~ D0
0	0	0	0	0	0	0	1	1	D	D	D	D	D15 ~ D0
0	0	0	0	0	0	1	0	0	E	E	E	E	D15 ~ D0
0	0	0	0	0	0	1	0	1	F	F	F	F	D15 ~ D0
:													
1	0	0	0	0	0	0	0	0	0	0	0	0	D31 ~ D16
1	0	0	0	0	0	0	0	1	1	1	1	1	D31 ~ D16
1	0	0	0	0	0	0	1	0	2	2	2	2	D31 ~ D16

BURST SEQUENCE(BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE(BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as a reference for SMROM operation. A square wave signal(CLK) must be applied externally at cycle time t_{CC}. All operations are synchronized to the rising edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high, all inputs are assumed to be in valid state (low or high) for the duration of set-up and hold time around the positive edge of the clock for proper functionality and I_{CC} specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock into the SMROM and is asserted high during all cycles, except for power down, stand-by and clock suspend mode. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen for as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. The SMROM remains in the power down mode ignoring other inputs for as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1 CLK + t_{SS}" before the rising edge of the clock, then the SMROM becomes active from the same clock edge accepting all the input commands.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{MR}$ are high, the SMROM performs no operation (NOP). NOP does not initiate any new operation. Device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{MR}$ and all the address inputs are ignored. In addition, entering a mode register set command in the middle of a normal operation, results in an illegal state in SMROM.

POWER-UP

The following power-up sequence is recommended.

1. Apply power and start clock, Attempt to maintain $\overline{MR}$, CKE and DQM inputs to pull them high and the other pins are NOP condition at the inputs before or along with V_{DD}(and $V_{DD}Q$) supply.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 20us.
3. When user wants to change the default mode register set values, perform a MODE REGISTER SET cycle to program the RAS latency, CAS latency, burst length and burst type.
4. At the end of three clock cycles after the mode register set cycle, the device is ready for operation. When the above sequence is used for power-up, all outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.

MODE SELECTION CONTROL

Mode selection control is decided simultaneously with column access, and according to $\overline{WORD}$ pin voltage level. High level signifies double word mode(x32) and low level signifies word mode(x16).

ADDRESS DECODING

The address bits required to decode one of the available cell locations out of the total depth are multiplexed onto the address select pins and latched by externally applying two commands. The first command, $\overline{RAS}$ asserted low, latches the row address into the device. A second command, $\overline{CAS}$ asserted low, subsequently latches the column address.

DEVICE OPERATIONS

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SMROM. It programs the RAS latency, CAS latency, burst length, burst type. On power-up, the mode register is set to the default value defined by the user requirement. When and if the user wants to change its values, the user must exit from power down mode and start mode register set before entering normal operation mode. The mode register is reprogrammed by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{MR}$ (The SMROM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_7 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{MR}$ going low is the data written in the mode register. Three clock cycles are required to complete the program in the mode register, therefore after mode register set command is completed, no new commands can be issued for 3 clock cycles and $\overline{CS}$ or $\overline{MR}$ must be fixed to high within 3 clock cycles. The mode register is divided into various fields depending on functionality. The burst length field uses A_0 ~ A_1, burst type uses A_2, CAS latency (read latency from column address) uses A_3 ~ A_5, RAS latency uses A_6 ($\overline{RAS}$ to $\overline{CAS}$ delay). Refer to the table for specific codes for various burst length, burst type, CAS latencies and RAS latencies.

LATENCY

There are latencies between the issuance of a Row active command and when data is available on the I/O buffers. The $\overline{RAS}$ to $\overline{CAS}$ delay is defined as the RAS latency. The $\overline{CAS}$ to data out delay is the CAS latency. The CAS and RAS latencies are programmable through the mode register. RAS latencies of 1 and 2, and CAS latencies of 3 through 6 are supported. It is understood that some RAS and CAS latency values are reserved for future use, and may not be available in the first generation for SMROM. The followings are the supported minimum values in the first generation. RAS latency=2, and CAS latency=5 for 100MHz operation, and RAS latency=2, and CAS latency=5 for 83MHz operation, and RAS latency=1, and CAS latency=4 for 66MHz operation, and RAS latency=1, and CAS latenecy=4 for 50MHz operation, and RAS latency=1, and CAS latenecy=3 for 33MHz operation.

DQM OPERATION

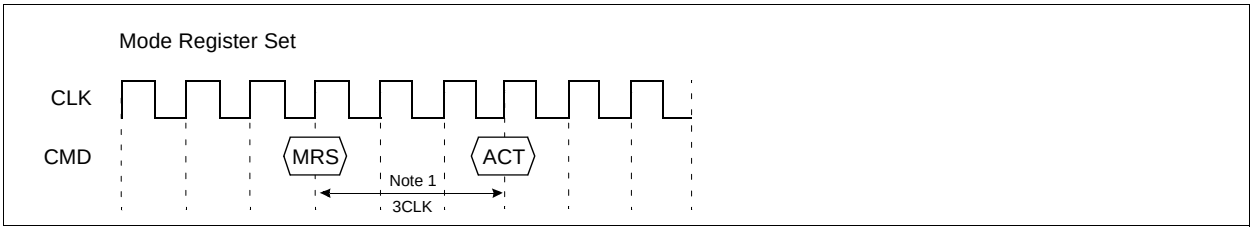
The DQM is used to mask output operations when a complete burst read is not required. It works similar to $\overline{OE}$ during a read operation. The read latency is two cycles from DQM, which means DQM masking occurs two cycles later in the read cycle. DQM operation is synchronous with the clock. The masking occurs for a complete cycle. (Also refer to the DQM timing diagram)

BURST READ

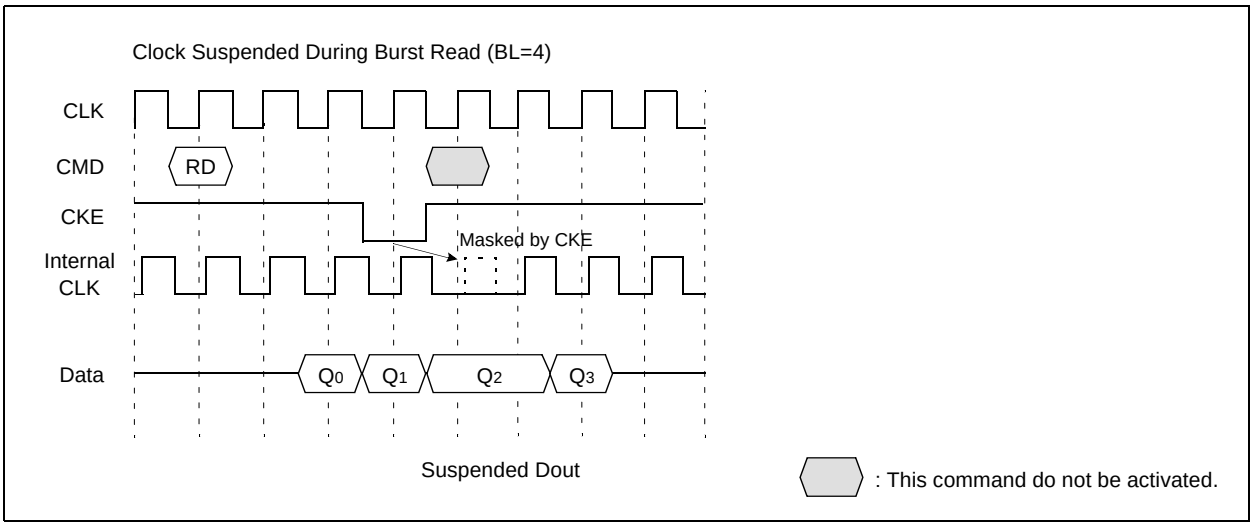
The burst read command is used to access a burst of data on consecutive clock cycles from an active row state. The burst read command is issued by asserting low $\overline{CS}$ and $\overline{CAS}$ with $\overline{MR}$ being high on the rising edge of the clock. The first output appears in CAS latency number of clock cycles after the issuance of the burst read command. The burst length, burst sequence and latency from the burst read command are determined by the mode register which is already programmed. Burst read can be initiated on any column address of the active row. The output goes into high-impedance at the end of the burst, unless a new burst read is initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

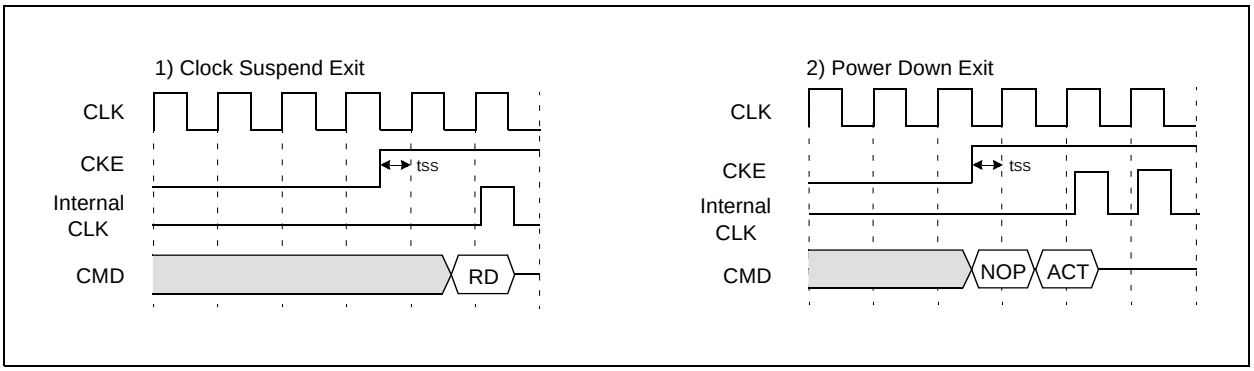
1. MRS



2. CLOCK Suspend



3. Clock Suspend Exit & power Down Exit

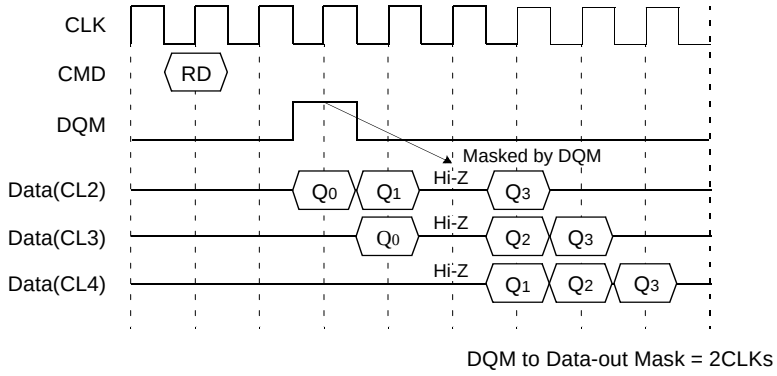


Note :

1. After mode register set command is completed, no new commands can be issued for 3 clock cycles, and MR or CS should be fixed "H" within a minimum of 3 clock cycles.

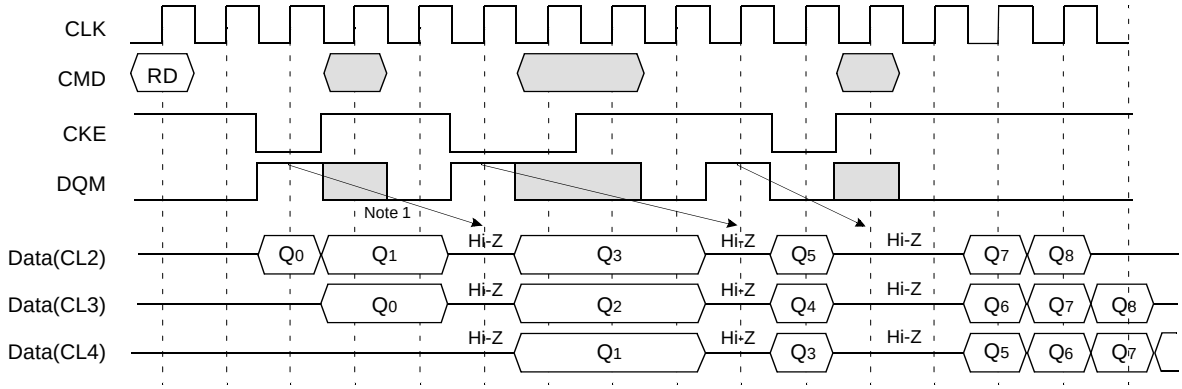
4. DQM Operation

1) Read Mask (BL=4)



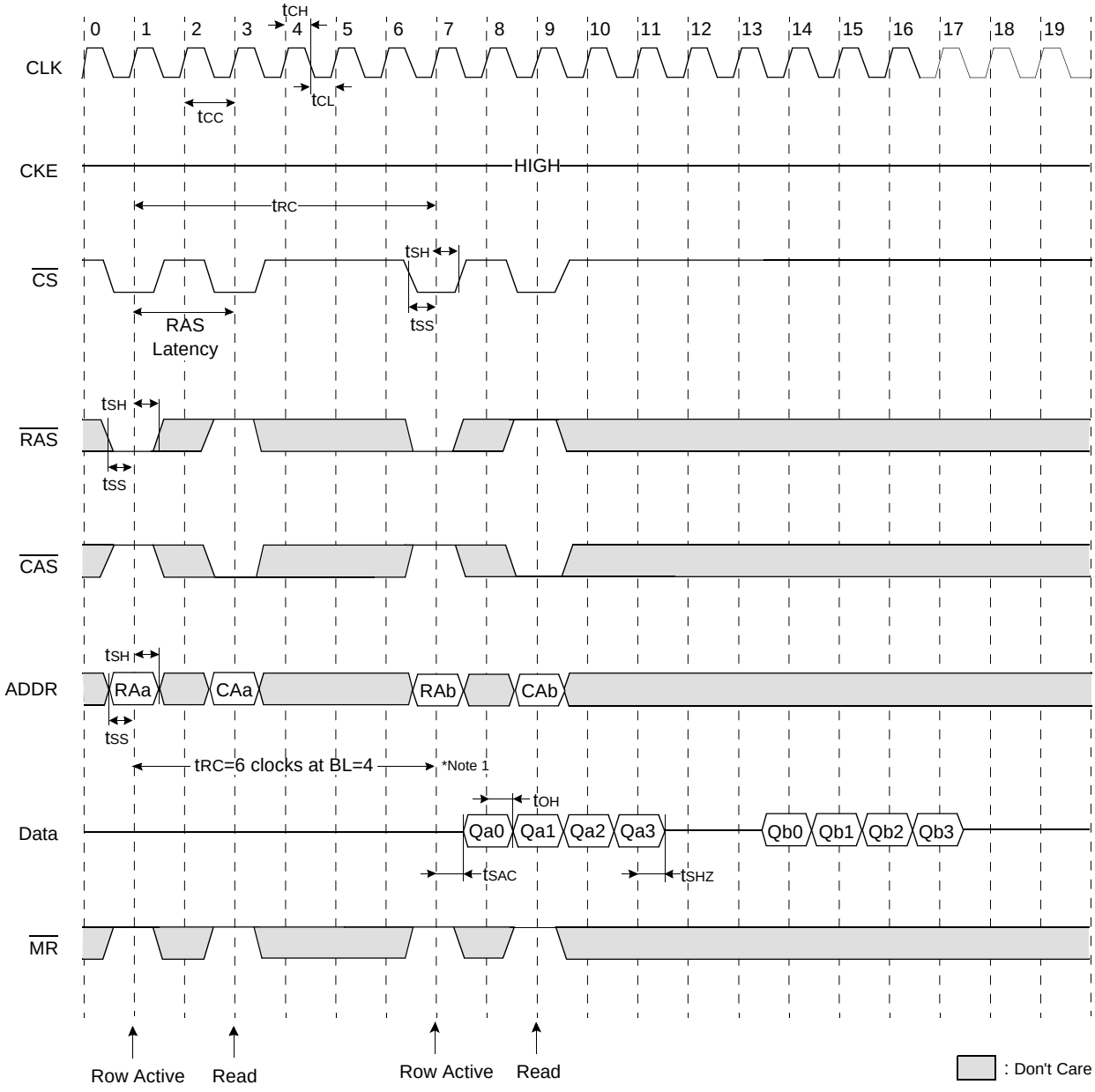
DQM to Data-out Mask = 2CLKs

2) DQM with Clock Suspended (BL=8)



*Note :
1. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"

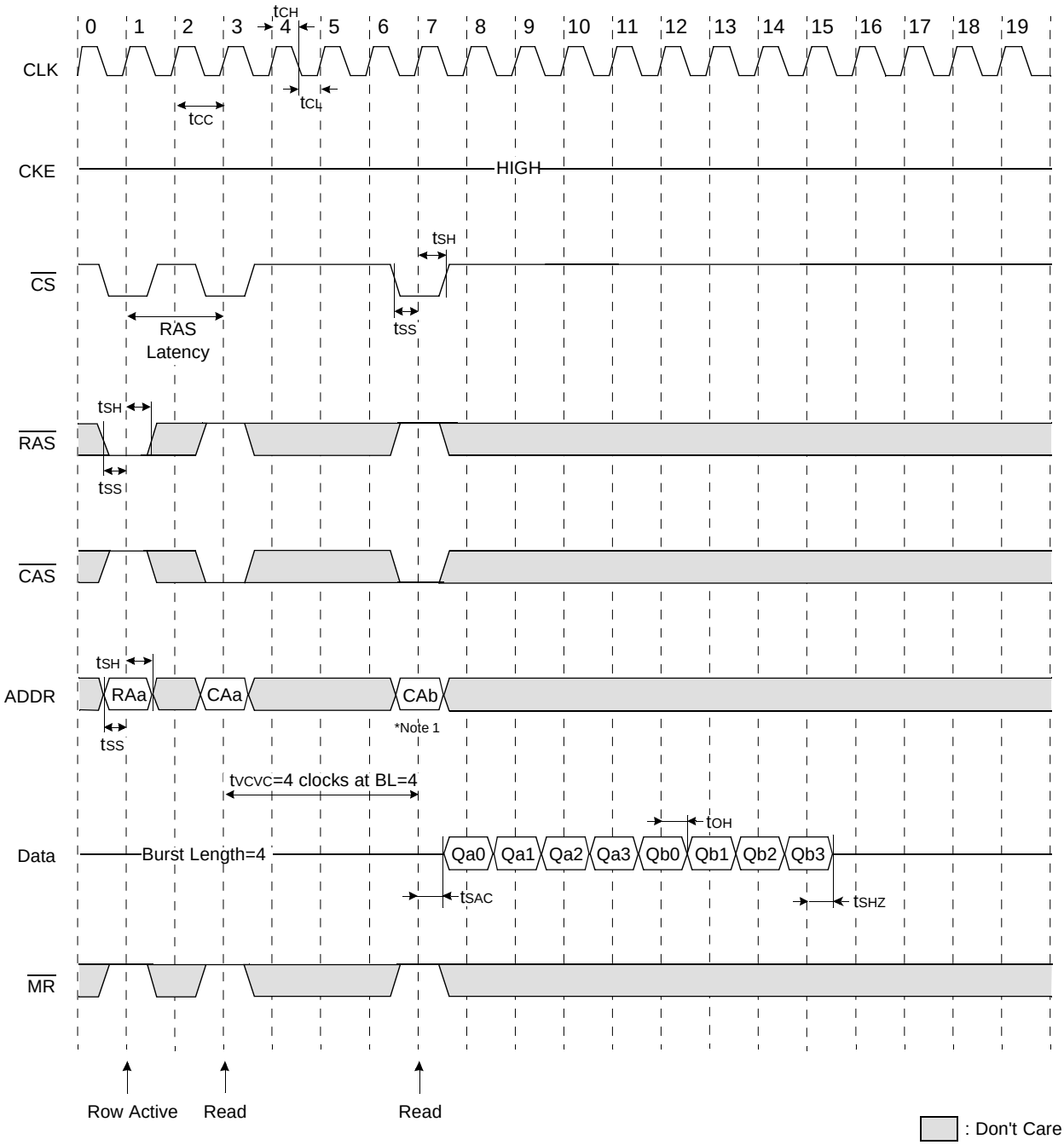
Read Cycle I : Normal @RAS Latency=2, CAS Latency=5, Burst Length=4



*Note:

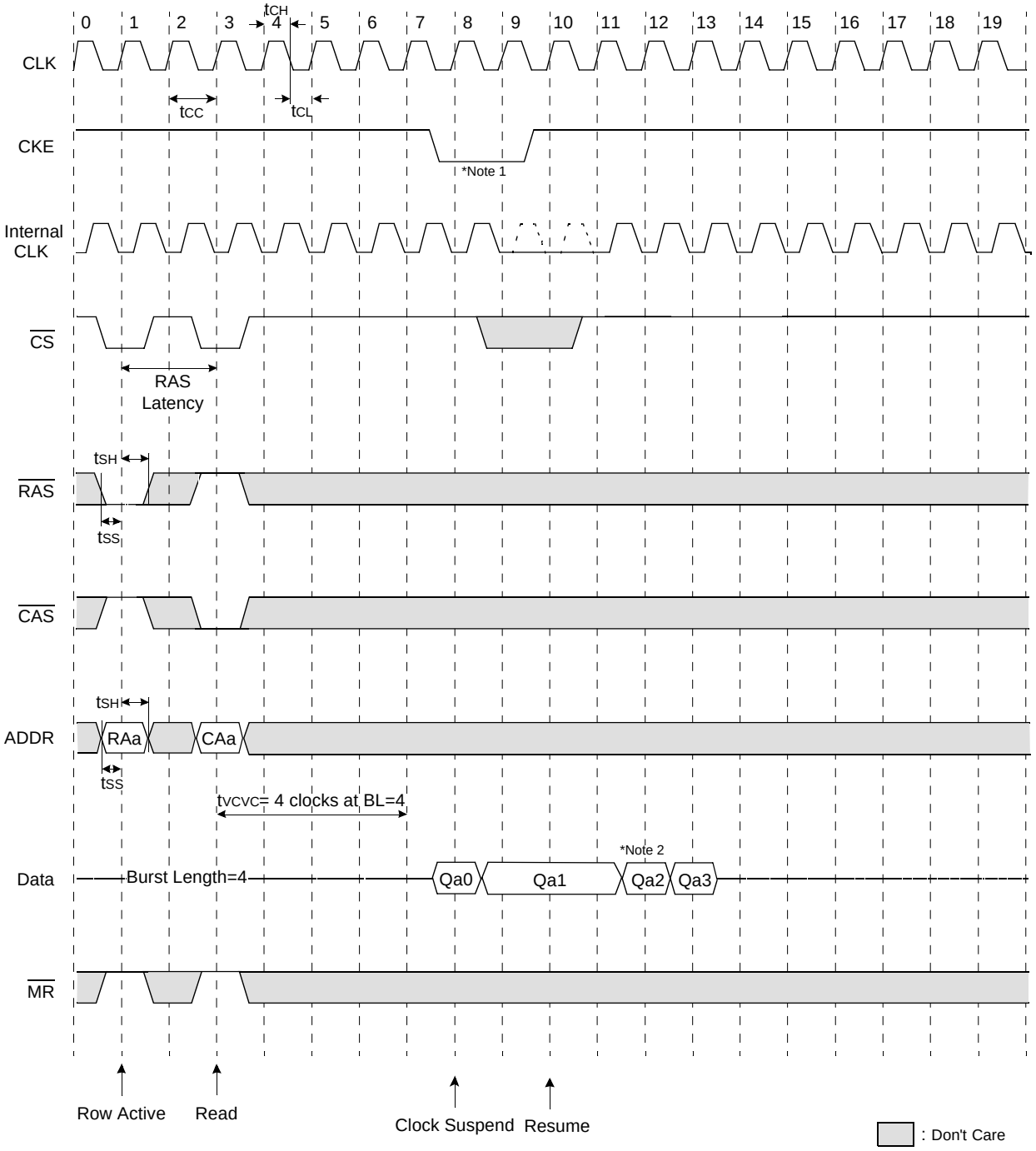
1. When the burst length is 4 at 100MHz, t_{RC} is equal to 6 clock cycles.

Read Cycle II : Consecutive Column Access @RAS Latency = 2, CAS Latency=5, BL = 4



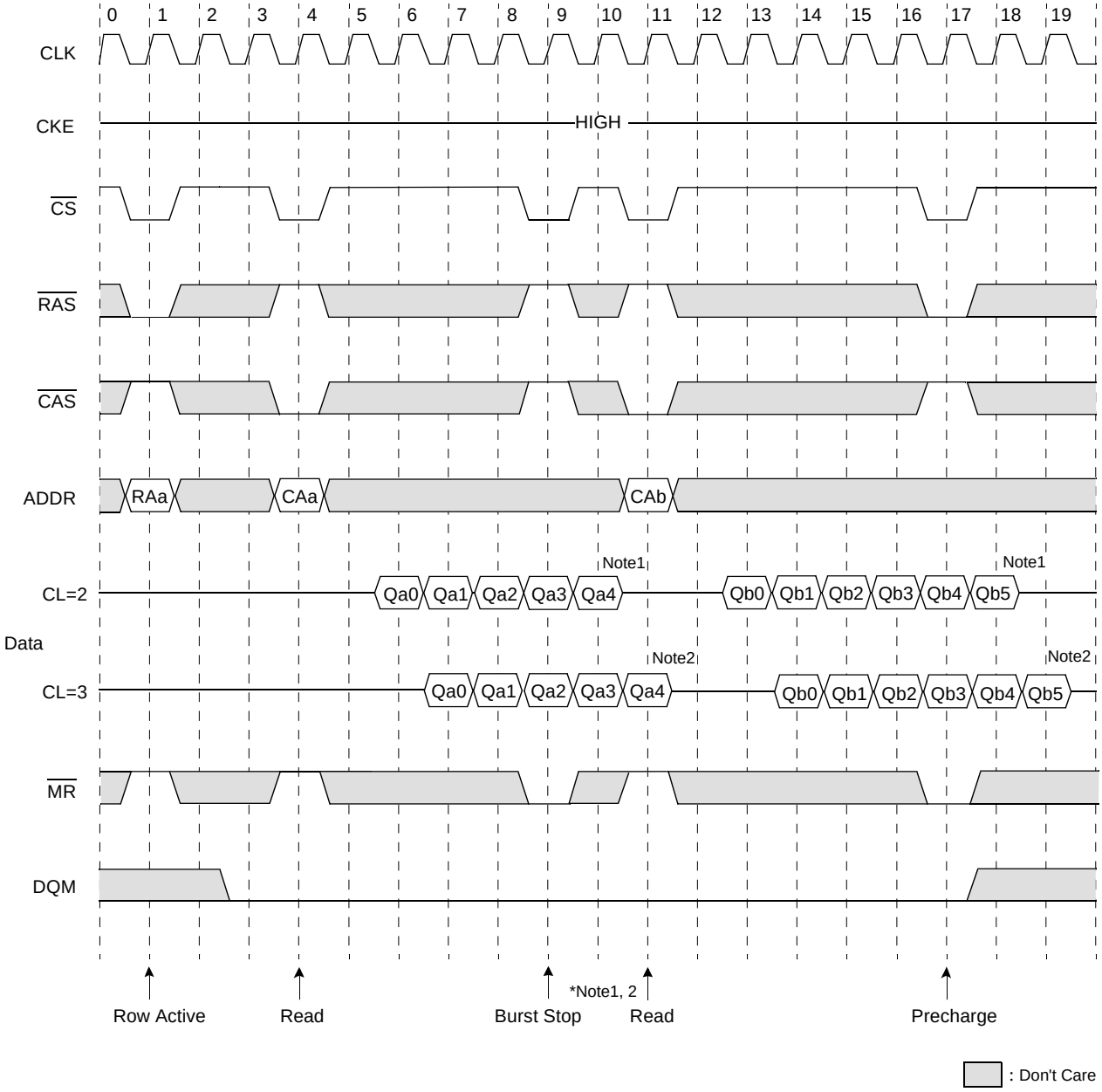
Note:
When column access is initiated beyond tVCVC,
1. at BL=4, CAa access read is completed, CAb access read begins.

Read Cycle III : Clock Suspend @RAS Latency = 2, CAS Latency=5, Burst Length=4



Note :
1. From next clock after CKE goes low, clock suspension begins.
2. For clock suspension, data output state is held & maintained.

Read Interrupted by Precharge Command & Burst Read Stop Cycle @Burst Length=8

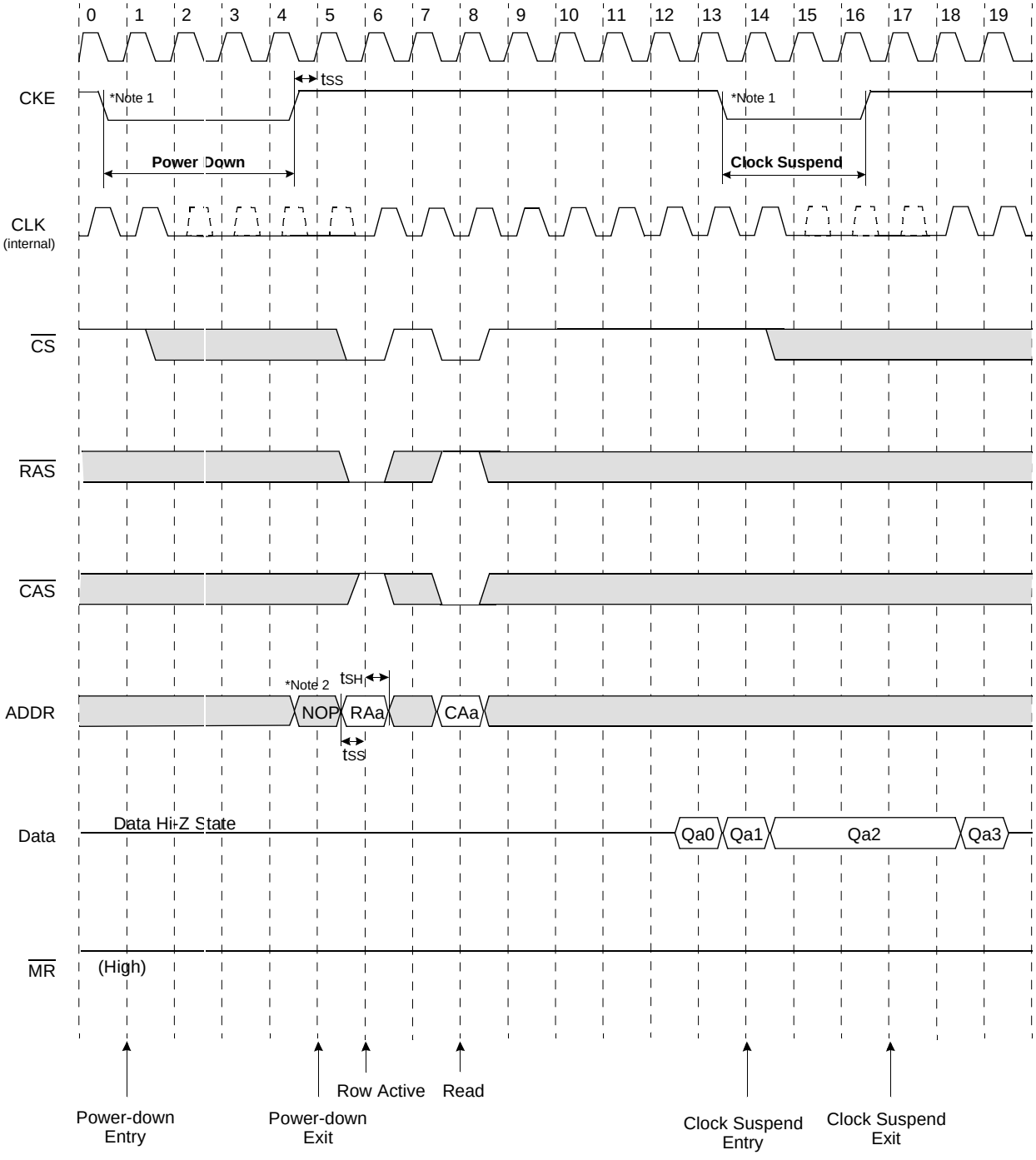


*Note :

1. The burst stop command is valid at every page burst length.
   The data bus goes to High-Z after the CAS latency from the burst stop command is issued.
2. The interval between read command (column address presented) and burst stop command is 1 cycle(min).

Power Down & Clock Suspend Cycle :

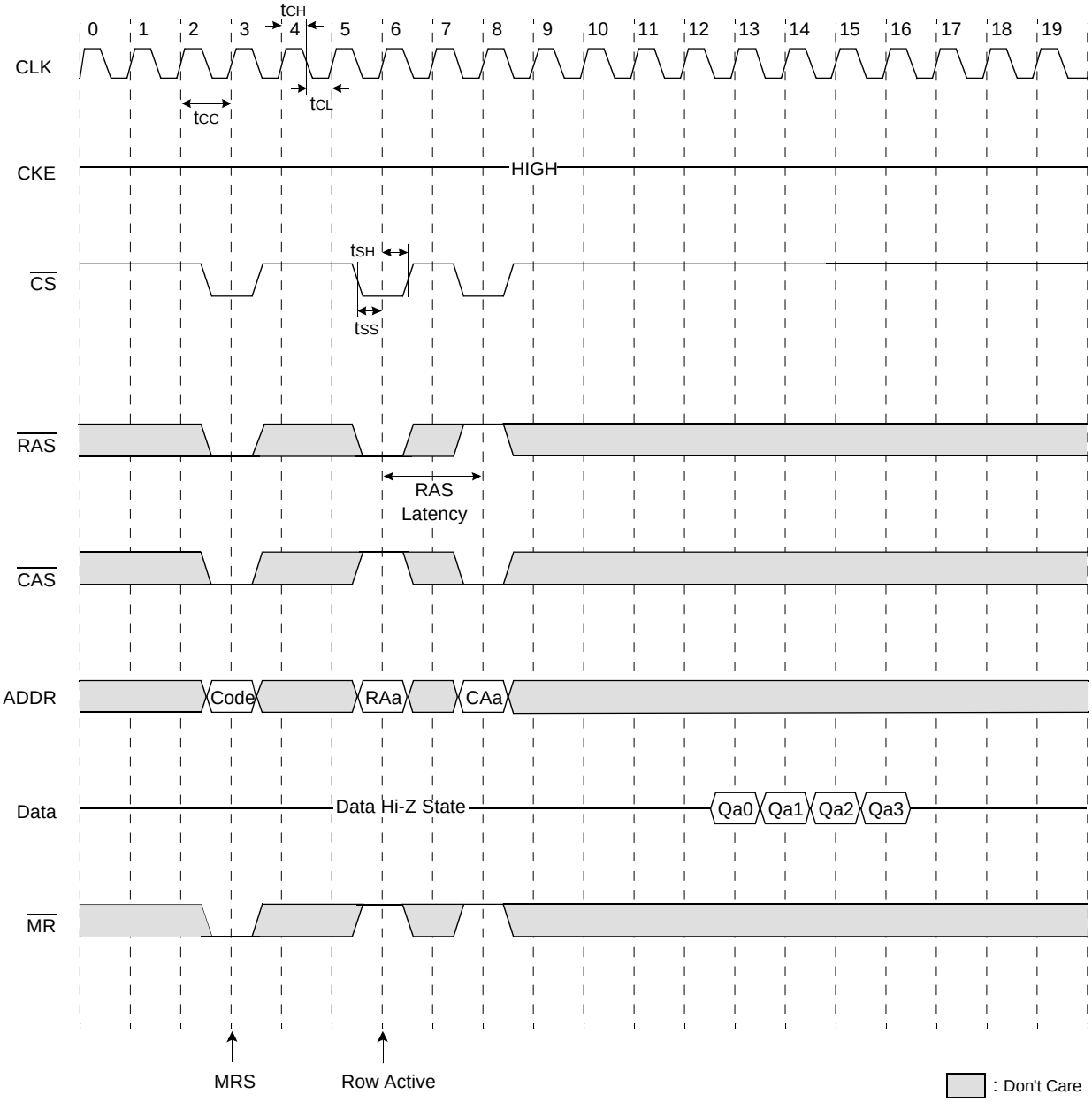
@RAS Latency = 2, CAS Latency=5, Burst Length=4



Note :
1. From next clock after CKE goes low, clock suspend and power down begins.
2. After power down exit, NOP should be issued and new command can be issued after 1clock.

Mode Register Set:

@RAS Latency = 2, CAS Latency=5, Burst Length=4



Note :

1. After the mode register set is completed, no new commands can be issued for 3CLK cycles.
2. After power up, necessarily mode register set should be completed at least one time and CS or MR must be fixed "H" within 3clock cycles, and when user wants to change mode register set, user must exit from power down mode and start mode register set before chip enters normal operation mode.

FUNCTION TRUTH TABLE

Current State	Input Signal						Next State Operation
	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$	Add.	
After Power Up*	L	X	X	X	X	X	-. Power Down
	H	L	L	H	H	RA	-. Row Active ; latch RA
	H	L	L	L	L	Code	-. Mode Register Set
Row Active	H	L	L	H	H	RA	-. If consecutive row access is issued within $t_{RCmin.}$ without $\overline{CAS}$ enabling, only the final RA is valid.
	H	L	H	L	H	CA	-. Begin READ ; latch CA
	H	L	L	L	L	Code	Illegal *
	L	X	X	X	X	X	-. Clock Suspend
READ	H	L	L	H	H	RA	-. Row Access in Read State, within the tRC, previous read is ignored and new row is activated. beyond the tRC, previous read is completed and new read begins.
	H	L	H	L	H	CA	-. Consecutive Column Access, within the t_{VCVC}, only the final CA is valid and the previous burst read is ignored. Beyond the t_{VCVC}, the previous read is completed and new read begins.
	H	L	L	H	L	X	-. NOP (After Burst Read) / Read Interrupt
	H	L	H	H	L	X	-. NOP (After Burst Read) / Read Interrupt
	H	L	L	L	L	Code	Illegal *
	L	X	X	X	X	X	-. Clock Suspend / Power Down
Any State	L	L	L	L	H	X	-. Low Power Consumption Mode
Any State	H	L	H	H	H	X	NOP
Any State	H	L	L	L	H	X	Illegal
	H	L	H	L	L	CA	Illegal

* : After the power up, when user wants to change MR set, user must exit from power down mode and start MR set before chip enters normal operation mode.

Technical Notes

1. Frequency vs. AC Parameter Relationship Table

K3S7V2000M-TC10

(unit : number of clock)

Burst Length	RAS Latency	CAS Latency	tRCmin.	tVCVCmin.
4	2	5	6	**4***
		6	7	5
8	2	5	10	**8***
		6	11	9

K3S7V2000M-TC12

(unit : number of clock)

Burst Length	RAS Latency	CAS Latency	tRCmin.	tVCVCmin.
4	2	5	6	**4***
		6	7	5
8	2	5	10	**8***
		6	11	9

K3S7V2000M-TC15

(unit : number of clock)

Burst Length	RAS Latency	CAS Latency	tRCmin.	tVCVCmin.
4	1	4	**4***	3/ **4***
		5	5	**4***
		6	6	5
	2	4	5	3/ **4***
		5	6	**4***
		6	7	5
8	1	4	**8***	7/ **8***
		5	9	**8***
		6	10	9
	2	4	9	7/**8***
		5	10	**8***
		6	11	9

K3S7V2000M-TC20

(unit : number of clock)

Burst Length	RAS Latency	CAS Latency	tRCmin.	tVCVCmin.
4	1	4	**4***	3/ **4***
		5	5	**4***
		6	6	5
	2	4	5	3/**4***
		5	6	**4***
		6	7	5
8	1	4	**8***	7/**8***
		5	9	**8***
		6	10	9
	2	4	9	7/ **8***
		5	10	**8***
		6	11	9

K3S7V2000M-TC30

(unit : number of clock)

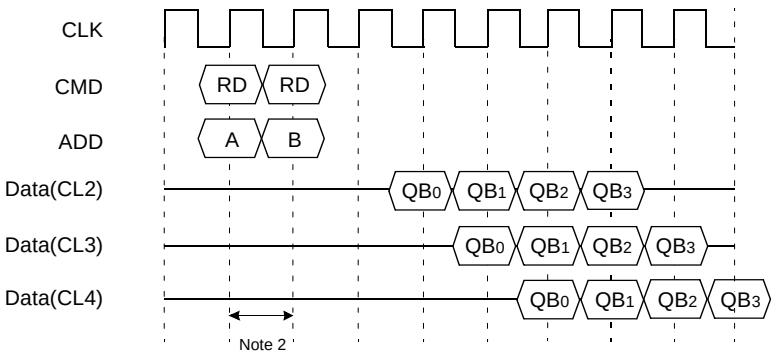
Burst Length	RAS Latency	CAS Latency	tRCmin.	tVCVCmin.
4	1	3	3/ **4***	2/ **4***
		4	**4***	3/ **4***
		5	5	**4***
		6	6	5
	2	3	**4***	2/**4***
		4	5	3/**4***
		5	6	**4***
		6	7	5
8	1	3	7/ **8***	6/ **8***
		4	**8***	7/ **8***
		5	9	**8***
		6	10	9
	2	3	**8***	6/**8***
		4	9	7/**8***
		5	10	**8***
		6	11	9

Note :
Above tables are not specification values, rather actual values.
There are no gapless operations for CAS latency 6.
* : Minimum clocks for Gapless Operation.

Technical Notes (Continuous)

2. *CAS Interrupt*

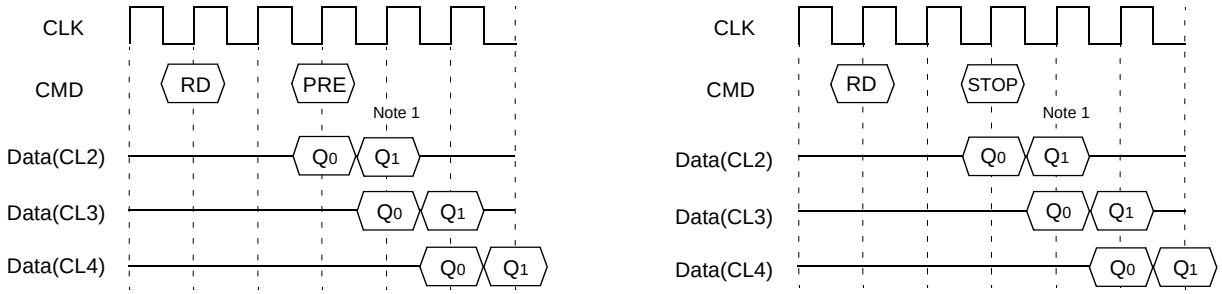
Read interrupted by Read (BL=4)Note 1



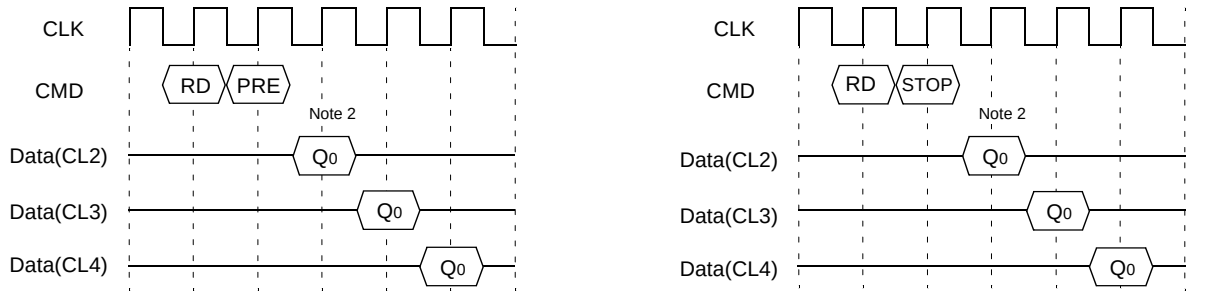
*Note :
1. By " Interrupt", It is meant to stop burst read by external command before the end of burst.
By "CAS Interrupt", to stop burst read by CAS access.
2. CAS to CAS delay. (=1CLK)

3. *Read interrupt operation by issuing the precharge or Burst Stop Command*

CASE I) Issued read Interrupt command during burst read operation period.



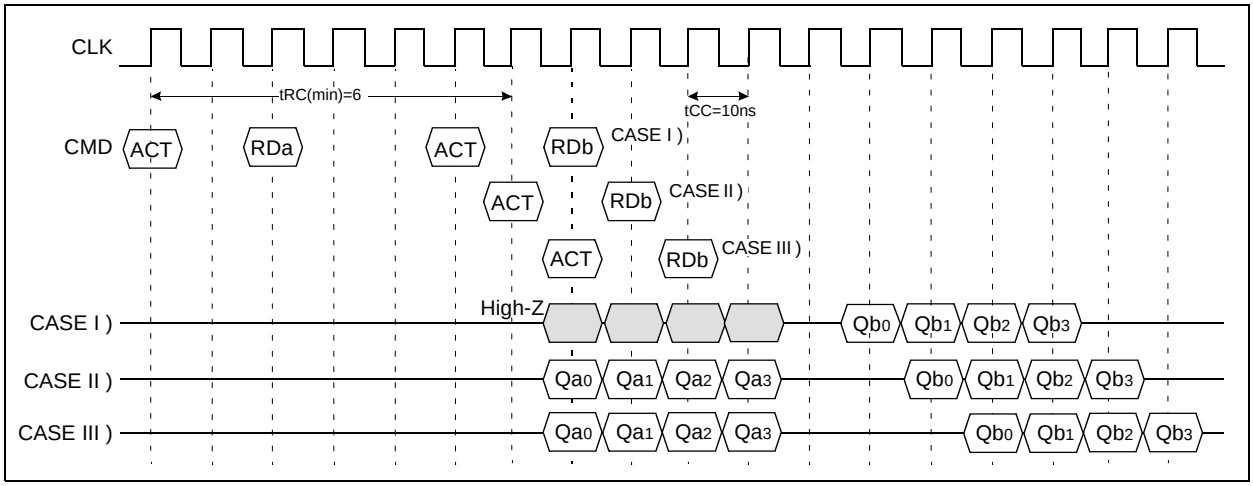
CASE II) Issued read Interrupt command between read command and data out.



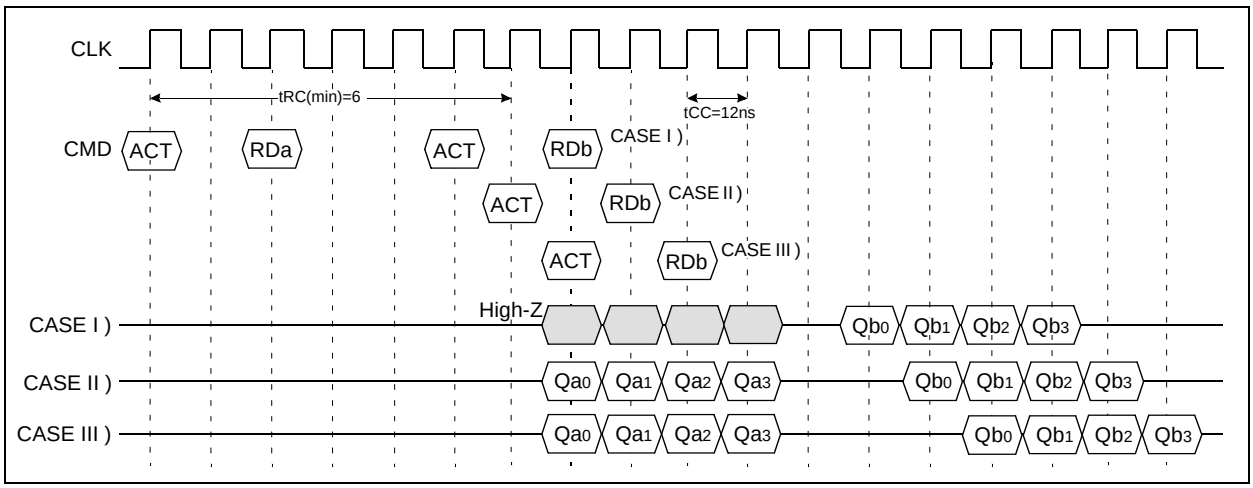
*Note :
1. The data bus goes to High-Z after CAS Latency from the burst stop (or precharge) command.
2. Valid output data will last up to CL-1 clock cycle from PRE command.

4. Read cycle depending on tRC

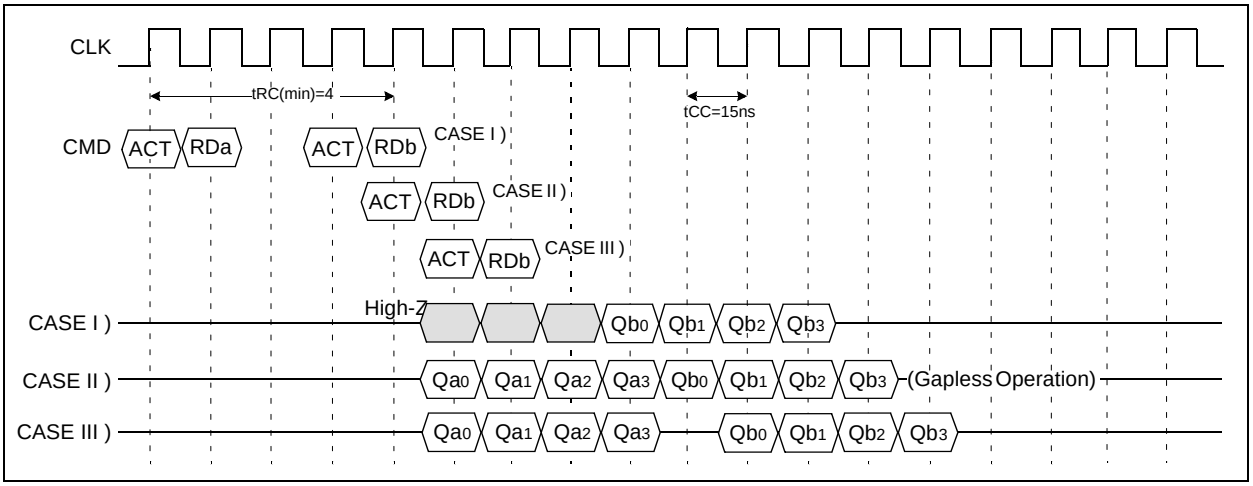
@ RL = 2, CL = 5, BL = 4 ; 100MHz



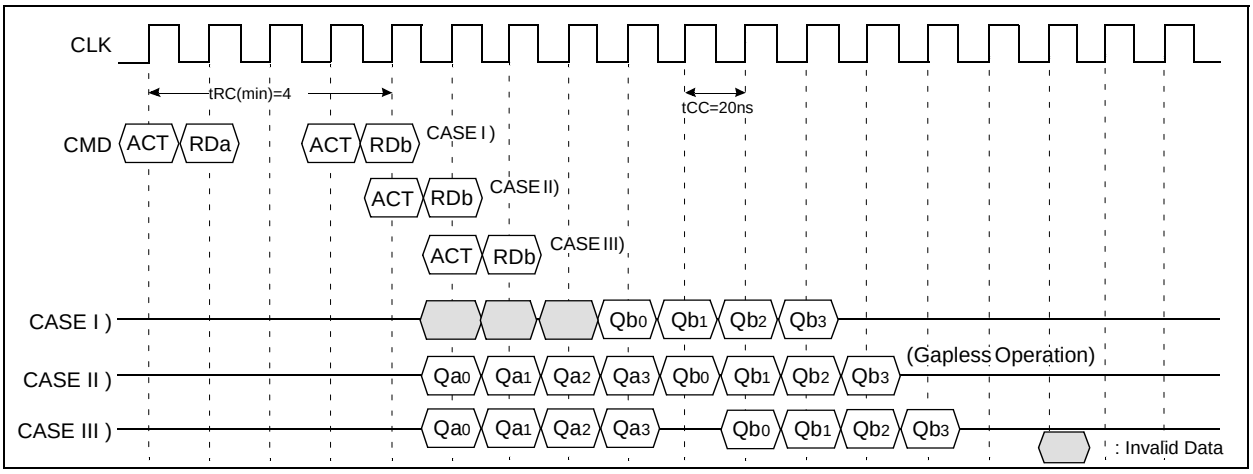
@ RL = 2, CL = 5, BL = 4 ; 83MHz



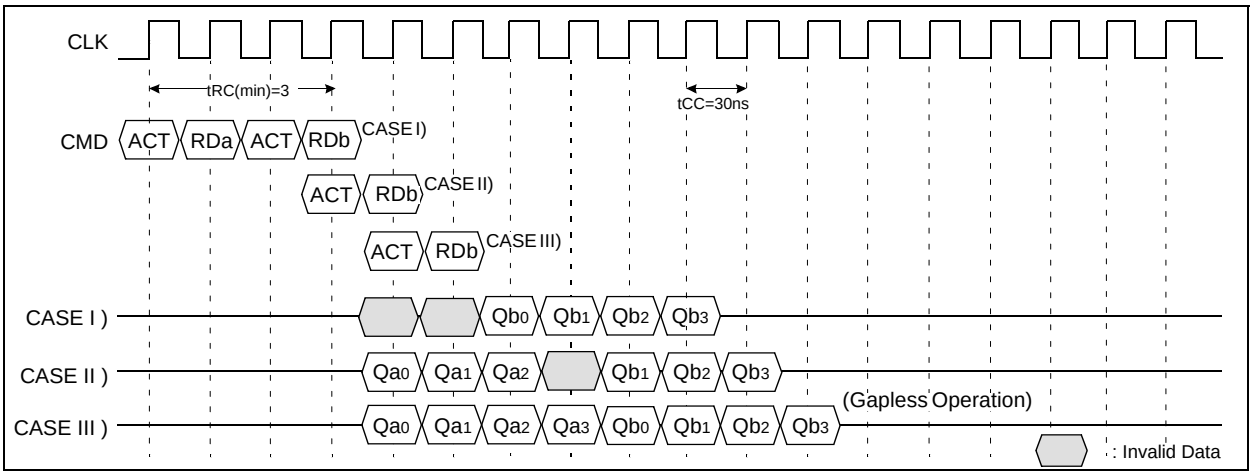
@ RL = 1, CL = 4, BL = 4 ; 66MHz



@ RL = 1, CL = 4, BL = 4 ; 50MHz

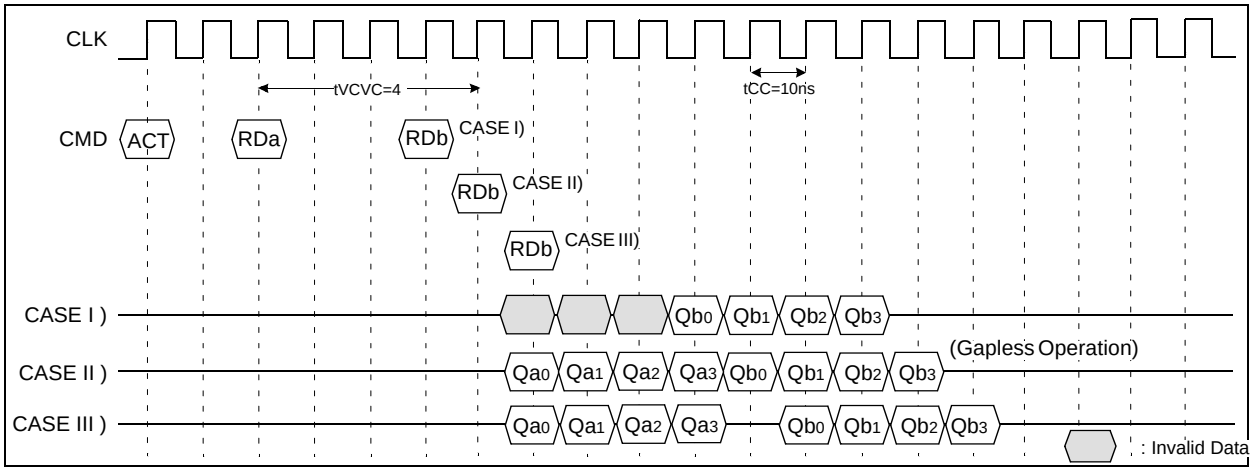


@ RL = 1, CL = 3, BL = 4 ; 33MHz

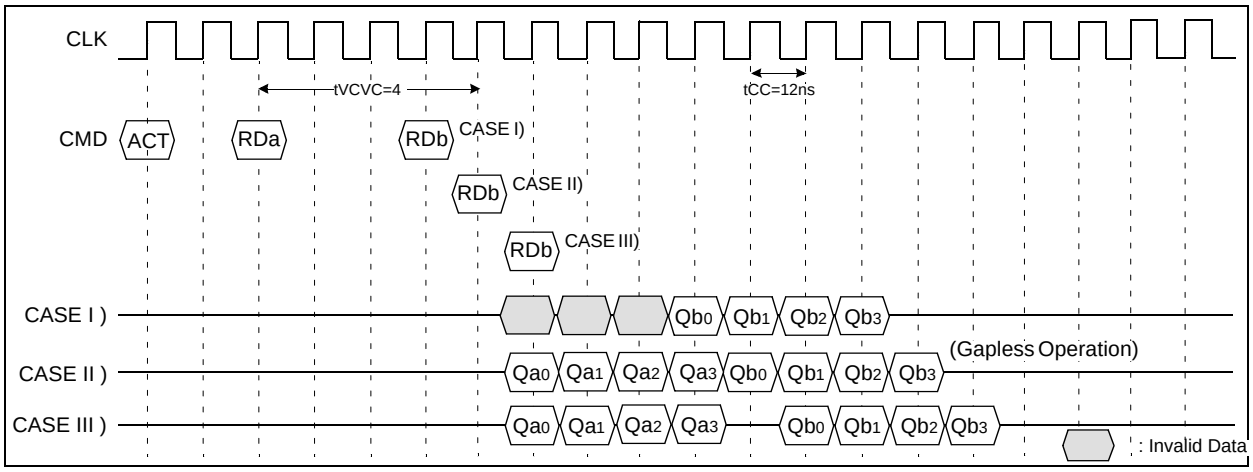


5. Read cycle depending on tVCVC

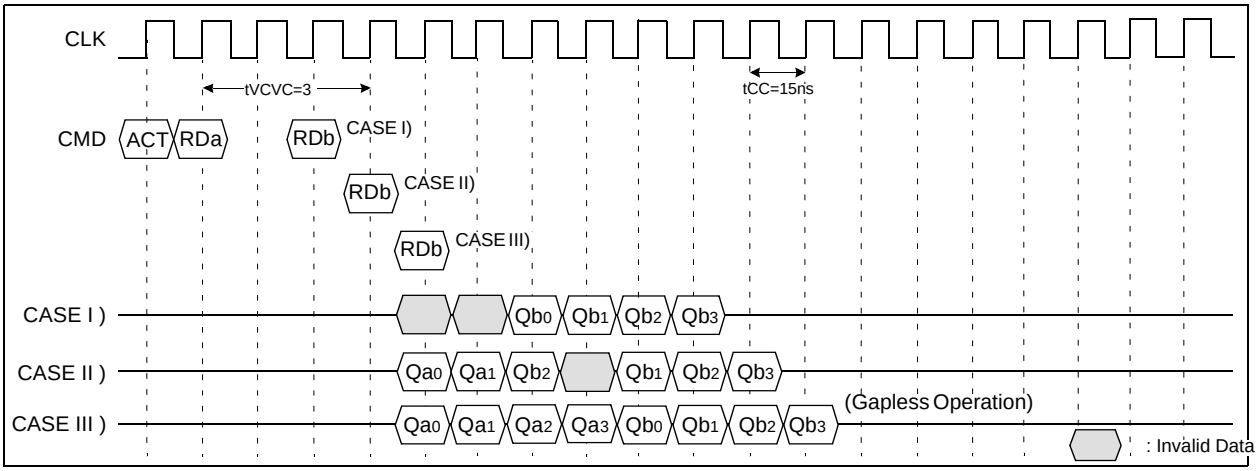
@ RL = 2, CL = 5, BL = 4 ; 100MHz



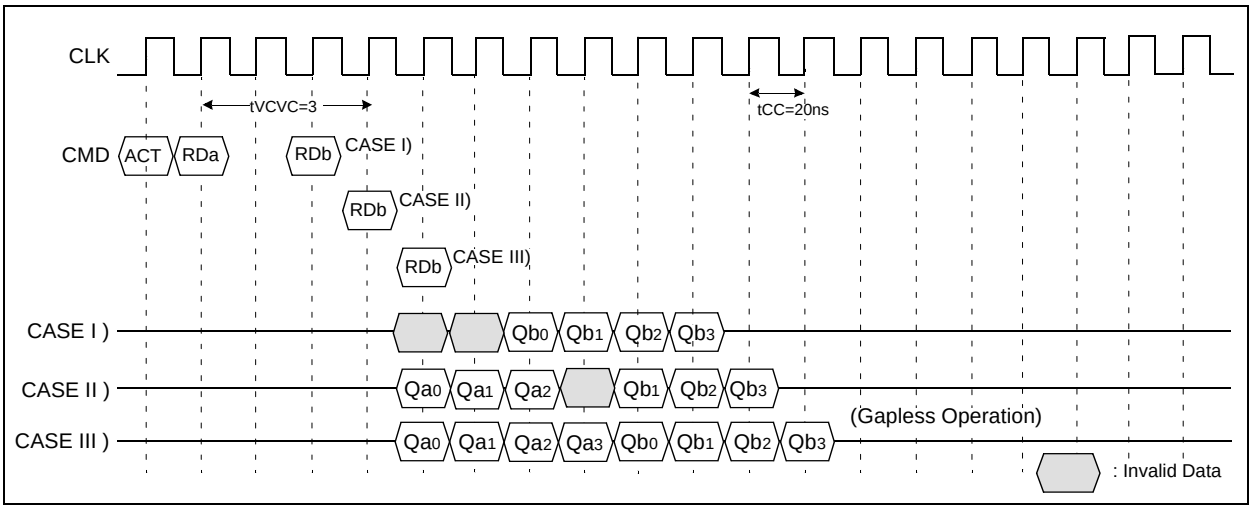
@ RL = 2, CL = 5, BL = 4 ; 83MHz



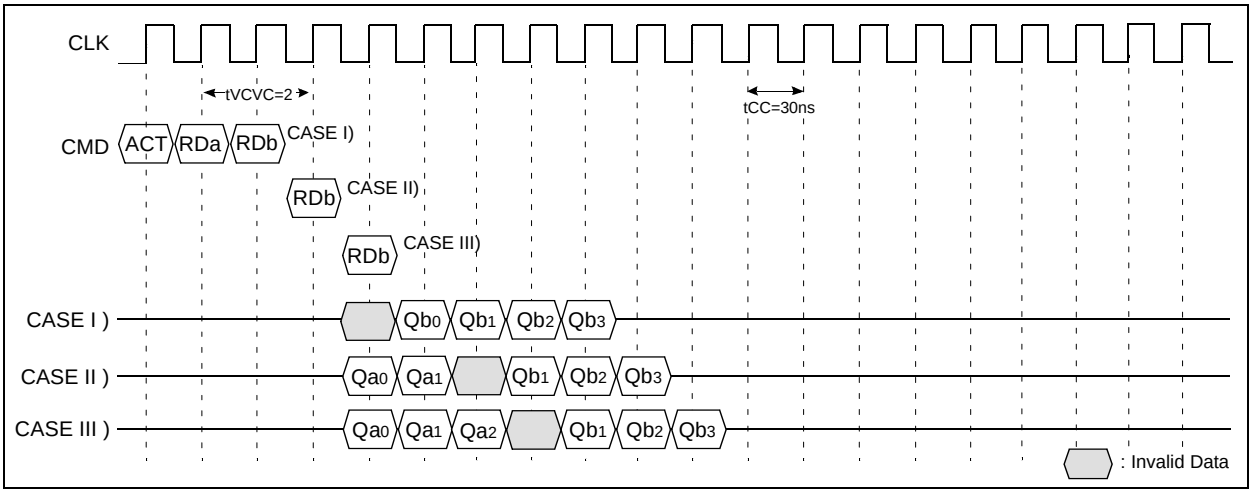
@ RL = 1, CL = 4, BL = 4 ; 66MHz



@ RL = 1, CL = 4, BL = 4 ; 50MHz

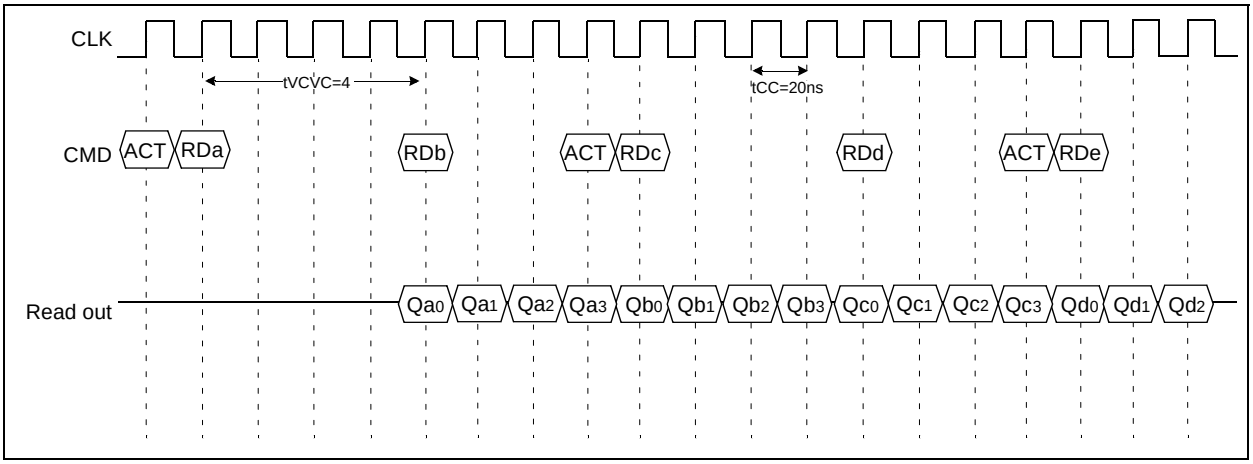


@ RL = 1, CL = 3, BL = 4 ; 33MHz

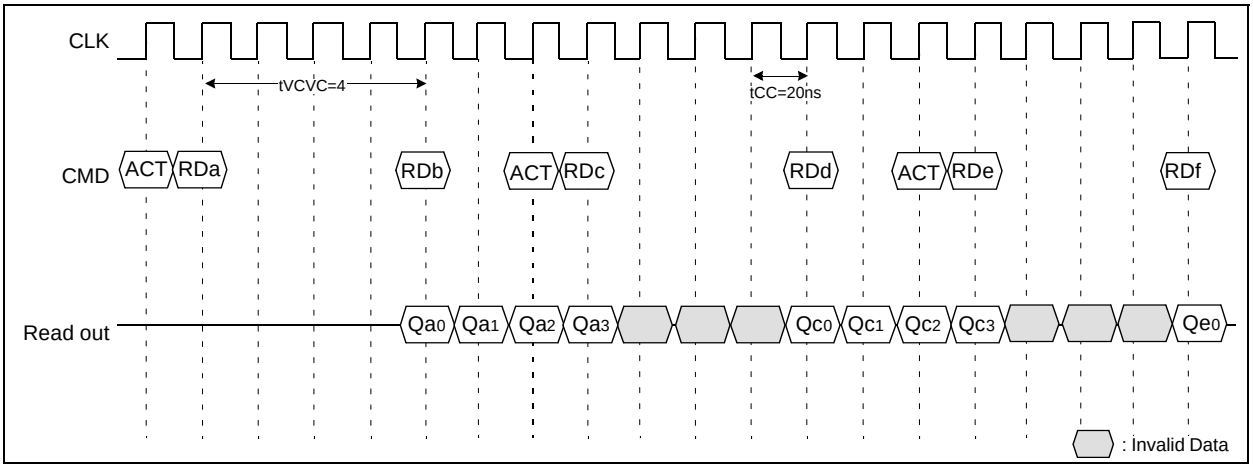


6. Read Cycle depending on tVCVC and tRC

@ RL = 1, CL = 4, BL = 4 ; 50MHz (Gapless Operation)



@ RL = 1, CL = 4, BL = 4 ; 50MHz



@ RL = 1, CL = 4, BL = 4 ; 50MHz