

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

65,536-WORD BY 16-BIT CMOS STATIC RAM

**DESCRIPTION**

The TC55V1664FT is a 1,048,576-bit high-speed static random access memory (SRAM) organized as 65,536 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed and low-voltage operation, it operates from a single 3.3 V power supply. Chip enable ( $\overline{CE}$ ) can be used to place the device in a low-power mode, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control signals (LB, UB) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTTL compatible. The TC55V1664FT is available in plastic 44-pin TSOP packages (400 mil width) for high density surface assembly.

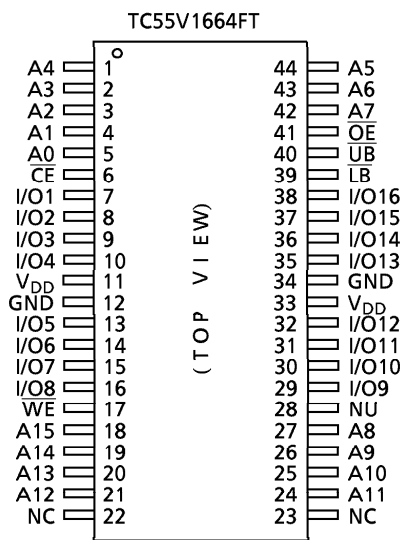
**FEATURES**

- Fast access time (the following are maximum values)
  - TC55V1664FT-12: 12 ns
  - TC55V1664FT-13: 13 ns
  - TC55V1664FT-15: 15 ns
- Low-power dissipation (the following are maximum values)
- Single power supply voltage of  $3.3 \pm 0.3$  V.
  - TC55V1664FT-12, -13:  $3.3$  V  $\pm$  5%
  - TC55V1664FT-15:  $3.3 \pm 0.3$  V
- Fully static operation
- All inputs and outputs are LVTTTL compatible
- Output buffer control using  $\overline{OE}$
- Data byte control using  $\overline{LB}$  (IO1 to IO8) and  $\overline{UB}$  (IO9 to IO16)
- Packages:
  - TSOP II 44-P-400-0.80 (Weight: 0.45 g typ)

Cycle Time	12	13	15	20	30	ns
Operation (max)	190	180	170	150	130	mA

Standby: 2 mA (all devices)

**PIN ASSIGNMENT**



(TSOP)

**PIN NAMES**

A0 to A15	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Inputs
$V_{DD}$	Power (+ 3.3 V)
GND	Ground
NC	No Connection
NU	Not Used (Input)

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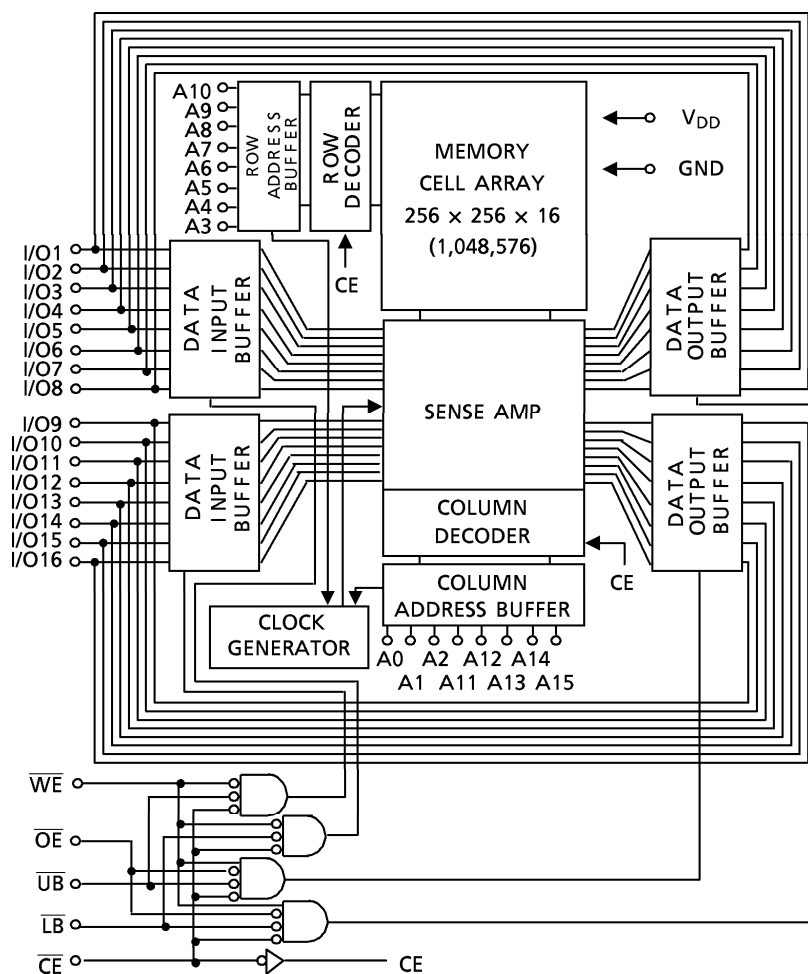
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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.5 to 4.6	V
V <sub>IN</sub>	Input Terminal Voltage	- 0.5 * to 4.6	V
V <sub>I/O</sub>	Input/Output Terminal Voltage	- 0.5 * to V <sub>DD</sub> + 0.5**	V
P <sub>D</sub>	Power Dissipation	1.2	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg</sub>	Storage Temperature	- 65 to 150	°C
T <sub>opr</sub>	Operating Temperature	- 10 to 85	°C

\*: - 1.5 V with a pulse width of 20% · t<sub>RC</sub> min (4 ns max)

\*\* : V<sub>DD</sub> + 1.5 V with a pulse width of 20% · t<sub>RC</sub> min (4 ns max)

**DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 12, - 13	3.135	3.3	3.465	V
		- 15	3.0	3.3	3.6	
V <sub>IH</sub>	Input High Voltage		2.0	-	V <sub>DD</sub> + 0.3**	V
V <sub>IL</sub>	Input Low Voltage		- 0.3*	-	0.8	V

\*: - 1.0 V with a pulse width of 20% · t<sub>RC</sub> min (4 ns max)  
 \*\*: V<sub>DD</sub> + 1.0 V with a pulse width of 20% · t<sub>RC</sub> min (4 ns max)

**DC CHARACTERISTICS (Ta = 0° to 70°C, -12, -13: V<sub>DD</sub> = 3.3 V ± 5%, -15: V<sub>DD</sub> = 3.3 ± 0.3 V)**

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current (Except NU Pin)	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	- 1	-	1	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 V to V <sub>DD</sub>	- 1	-	1	μA	
I <sub>I(NU)</sub>	Input Current (NU Pin)	V <sub>IN</sub> = 0 to 0.8 V	- 1	-	20	μA	
		V <sub>IN</sub> = 0 to 0.2 V	- 1	-	1		
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = - 2 mA	2.4	-	-	V	
		I <sub>OH</sub> = - 100 μA	V <sub>DD</sub> - 0.2	-	-		
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2 mA	-	-	0.4		
		I <sub>OL</sub> = 100 μA	-	-	0.2		
I <sub>DDO</sub>	Operating Current	$\overline{CE} = V_{IL}$ , I <sub>out</sub> = 0 mA Other Inputs = V <sub>IH</sub> or V <sub>IL</sub>	tcycle = 12 ns	-	-	190	mA
			tcycle = 13 ns	-	-	180	
			tcycle = 15 ns	-	-	170	
			tcycle = 20 ns	-	-	150	
			tcycle = 30 ns	-	-	130	
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$ , Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	-	-	20	mA	
I <sub>DDS2</sub>		$\overline{CE} = V_{DD} - 0.2$ V Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	-	-	2		

**CAPACITANCE (Ta = 25°C, f = 1.0 MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I <sub>DDO</sub>
				H	L	High Impedance	Output	I <sub>DDO</sub>
				L	H	Output	High Impedance	I <sub>DDO</sub>
Write	L	x	L	L	L	Input	Input	I <sub>DDO</sub>
				H	L	High Impedance	Input	I <sub>DDO</sub>
				L	H	Input	High Impedance	I <sub>DDO</sub>
Outputs Disable	L	H	H	x	x	High Impedance	High Impedance	I <sub>DDO</sub>
	L	x	x	H	H			
Standby	H	x	x	x	x	High Impedance	High Impedance	I <sub>DDS</sub>

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.  
 You must not apply a voltage of more than 0.8 V to the NU.

**AC CHARACTERISTICS**

(Ta = 0° to 70°C (Note 1), -12,-13: V<sub>DD</sub> = 3.3 V ± 5%, -15: V<sub>DD</sub> = 3.3 ± 0.3 V)

**READ CYCLE**

SYMBOL	PARAMETER	TC55V1664FT-12		TC55V1664FT-13		TC55V1664FT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	12	–	13	–	15	–	ns
t <sub>ACC</sub>	Address Access Time	–	12	–	13	–	15	
t <sub>CO</sub>	Chip Enable Access Time	–	12	–	13	–	15	
t <sub>OE</sub>	Output Enable Access Time	–	6	–	6	–	8	
t <sub>BA</sub>	Upper Byte, Lower Byte Access Time	–	6	–	6	–	8	
t <sub>OH</sub>	Output Data Hold Time from Address Change	3	–	3	–	3	–	
t <sub>COE</sub>	Output Enable Time from Chip Enable	3	–	3	–	3	–	
t <sub>OEE</sub>	Output Enable Time from Output Enable	1	–	1	–	1	–	
t <sub>BE</sub>	Output Enable Time from Upper Byte, Lower Byte	1	–	1	–	1	–	
t <sub>COD</sub>	Output Disable Time from Chip Enable	–	7	–	7	–	8	
t <sub>ODO</sub>	Output Disable Time from Output Enable	–	7	–	7	–	8	
t <sub>BD</sub>	Output Disable Time from Upper Byte, Lower Byte	–	7	–	7	–	8	

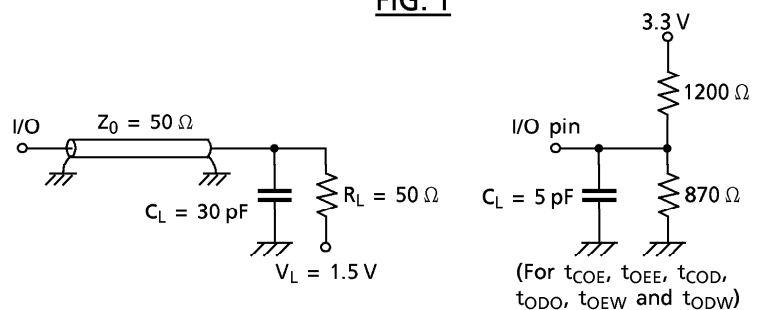
**WRITE CYCLE**

SYMBOL	PARAMETER	TC55V1664FT-12		TC55V1664FT-13		TC55V1664FT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	12	–	13	–	15	–	ns
t <sub>WP</sub>	Write Pulse Width	8	–	8	–	9	–	
t <sub>CW</sub>	Chip Enable to End of Write	10	–	10	–	12	–	
t <sub>BW</sub>	Upper Byte, Lower Byte Enable to End of Write	10	–	10	–	11	–	
t <sub>AW</sub>	Address Valid to End of Write	10	–	10	–	11	–	
t <sub>AS</sub>	Address Setup Time	0	–	0	–	0	–	
t <sub>WR</sub>	Write Recovery Time	0	–	0	–	0	–	
t <sub>DS</sub>	Data Setup Time	7	–	7	–	8	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	0	–	
t <sub>OE<sub>W</sub></sub>	Output Enable Time from Write Enable	1	–	1	–	1	–	
t <sub>OD<sub>W</sub></sub>	Output Disable Time from Write Enable	–	7	–	7	–	8	

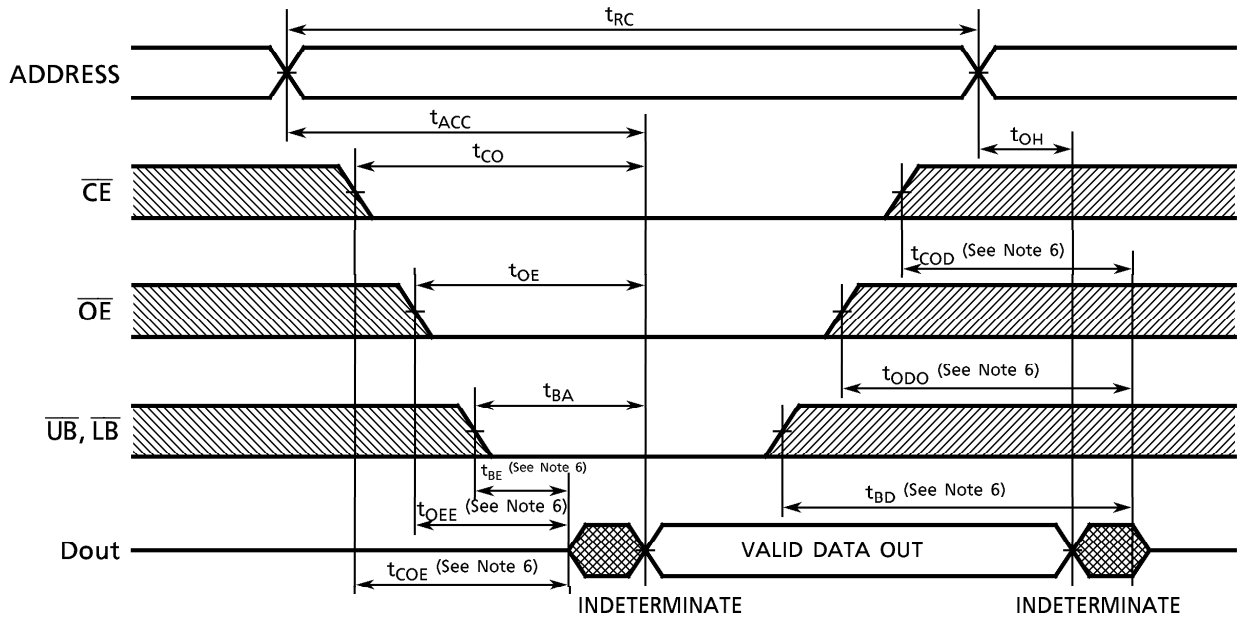
**AC TEST CONDITIONS**

Input Pulse Level	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig. 1

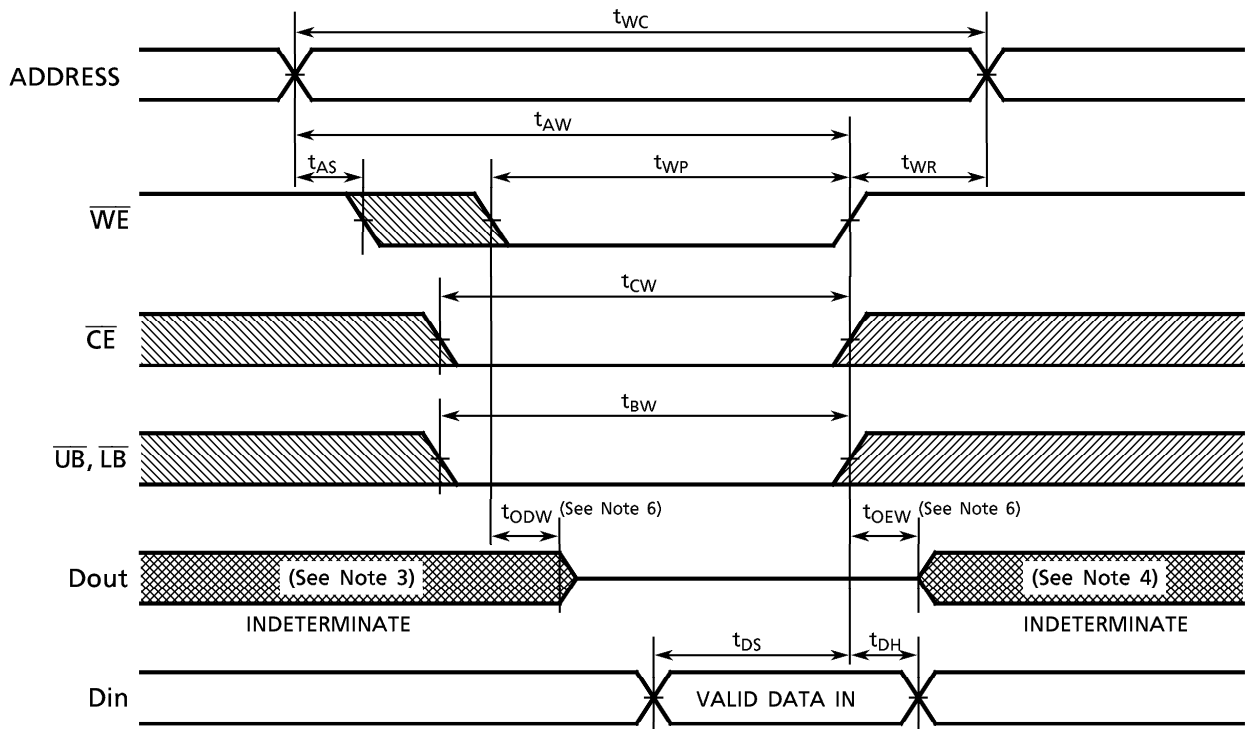
**FIG. 1**



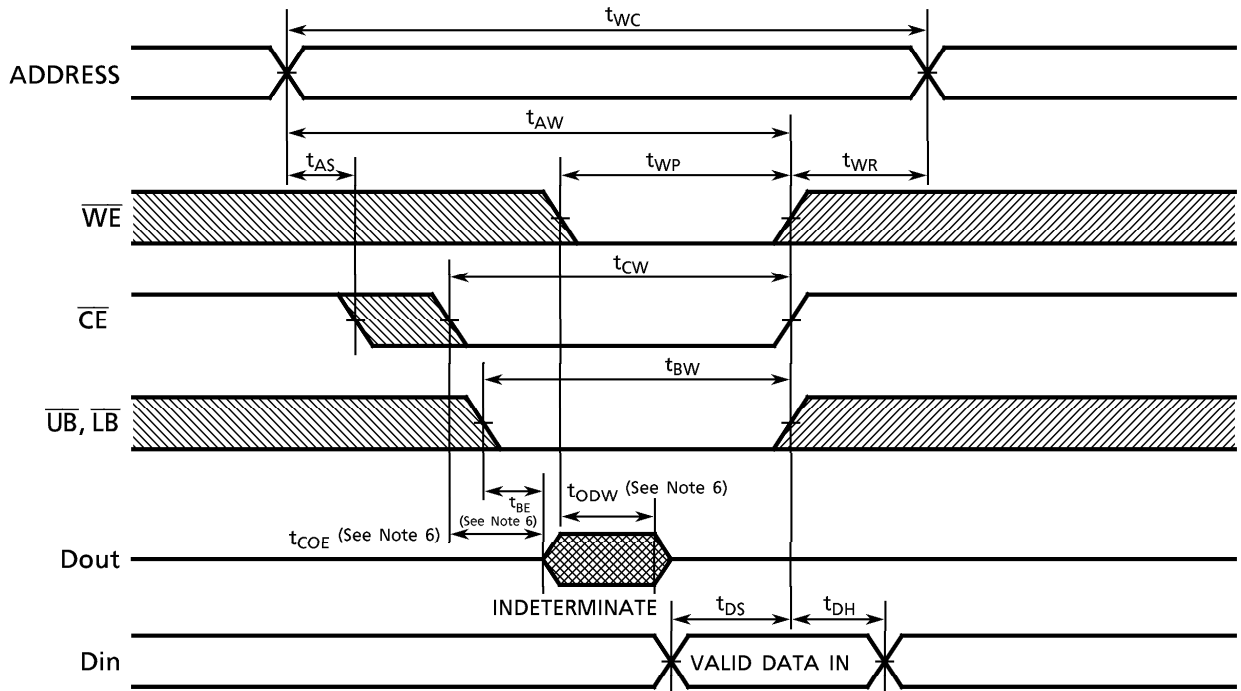
**TIMING DIAGRAMS**  
READ CYCLE (See Note 2)



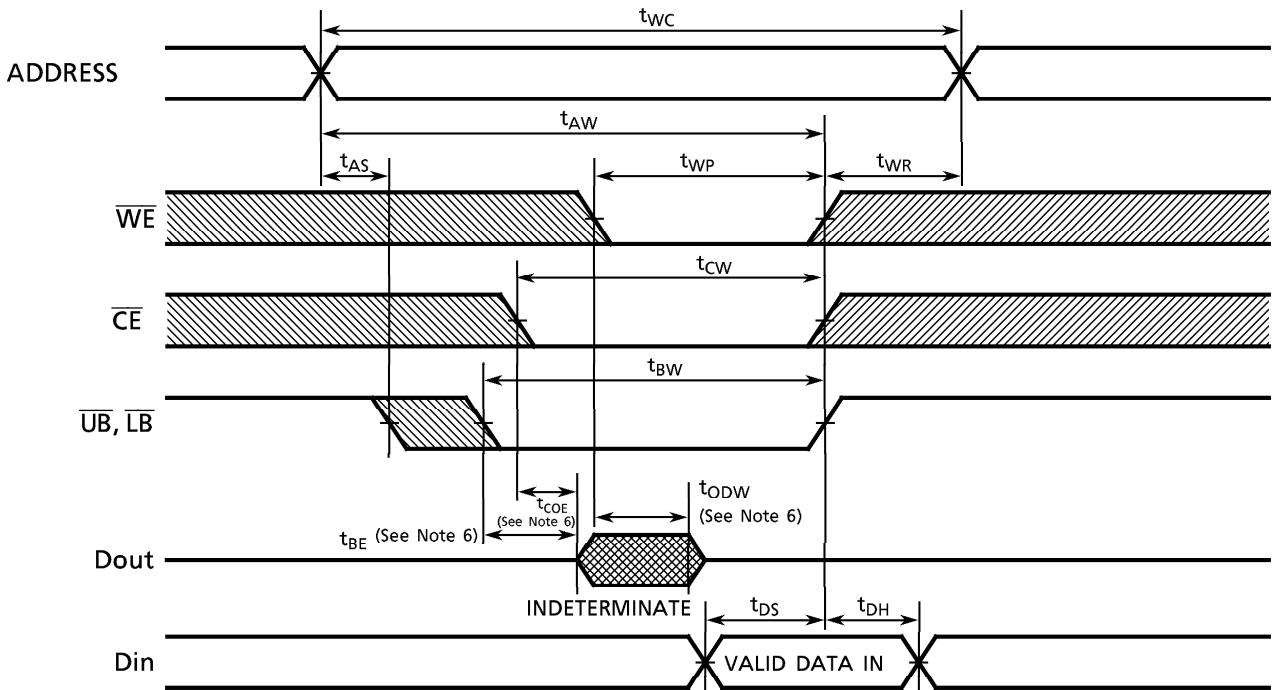
WRITE CYCLE 1 ( $\overline{WE}$  CONTROLLED) (Note 5)



WRITE CYCLE 2 ( $\overline{CE}$  CONTROLLED) (See Note 5)



WRITE CYCLE 3 ( $\overline{UB}$ ,  $\overline{LB}$  CONTROLLED) (See Note 5)



Note: (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2)  $\overline{WE}$  remains High for the Read Cycle.

(3) If  $\overline{CE}$  goes LOW coincident with or after  $\overline{WE}$  goes LOW, the outputs will remain at high impedance.

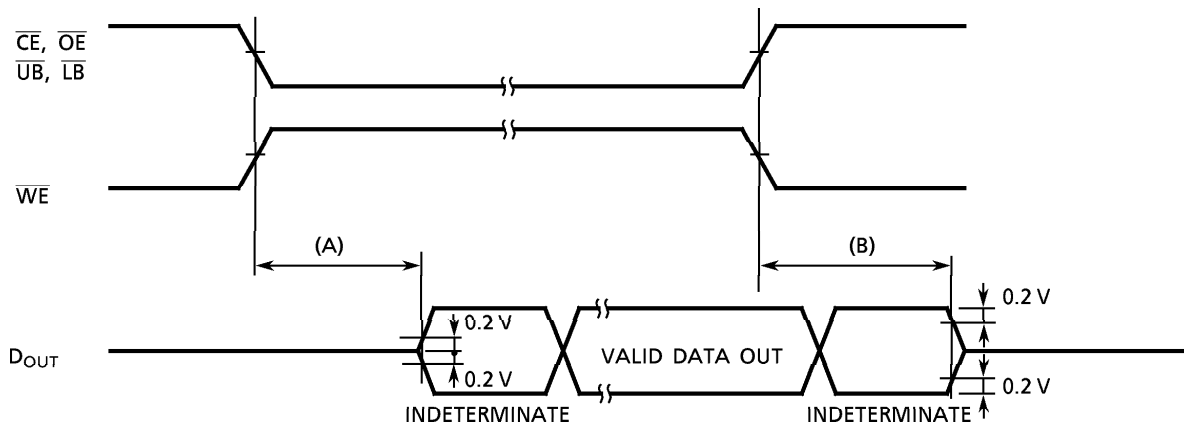
(4) If  $\overline{CE}$  goes HIGH coincident with or before  $\overline{WE}$  goes HIGH, the outputs will remain at high impedance.

(5) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1

(A)  $t_{COE}, t_{OEE}, t_{BE}, t_{OEw}$  ..... Output Enable Time

(B)  $t_{COD}, t_{ODO}, t_{BD}, t_{ODw}$  ..... Output Disable Time

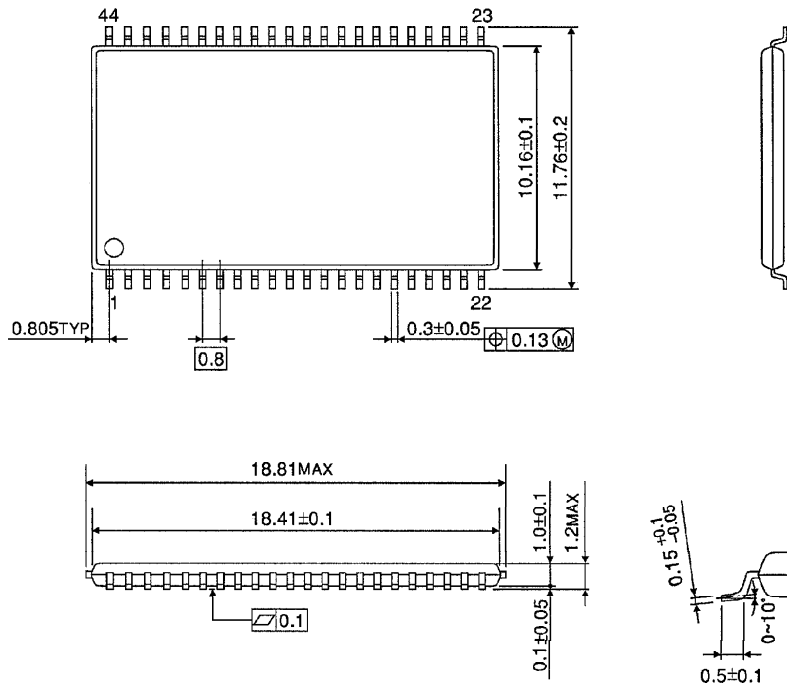




PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 44-P-400-0.80)

Units in mm



Weight: 0.45 g (typ)