

OKI semiconductor**MSC23836B-xxBS20/DS20****8,388,608 Word By 36 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE****GENERAL DESCRIPTION**

The Oki MSC23836B-xxBS20/DS20 is a fully decoded, 8,388,608 word X 36 bit CMOS dynamic random access memory composed of sixteen 16Mb DRAMs(4Mx4) in SOJ and four 8Mb DRAMs(4Mx2) in SOJ.

The mounting of twenty DRAMs together with decoupling capacitors on a 72-pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required.

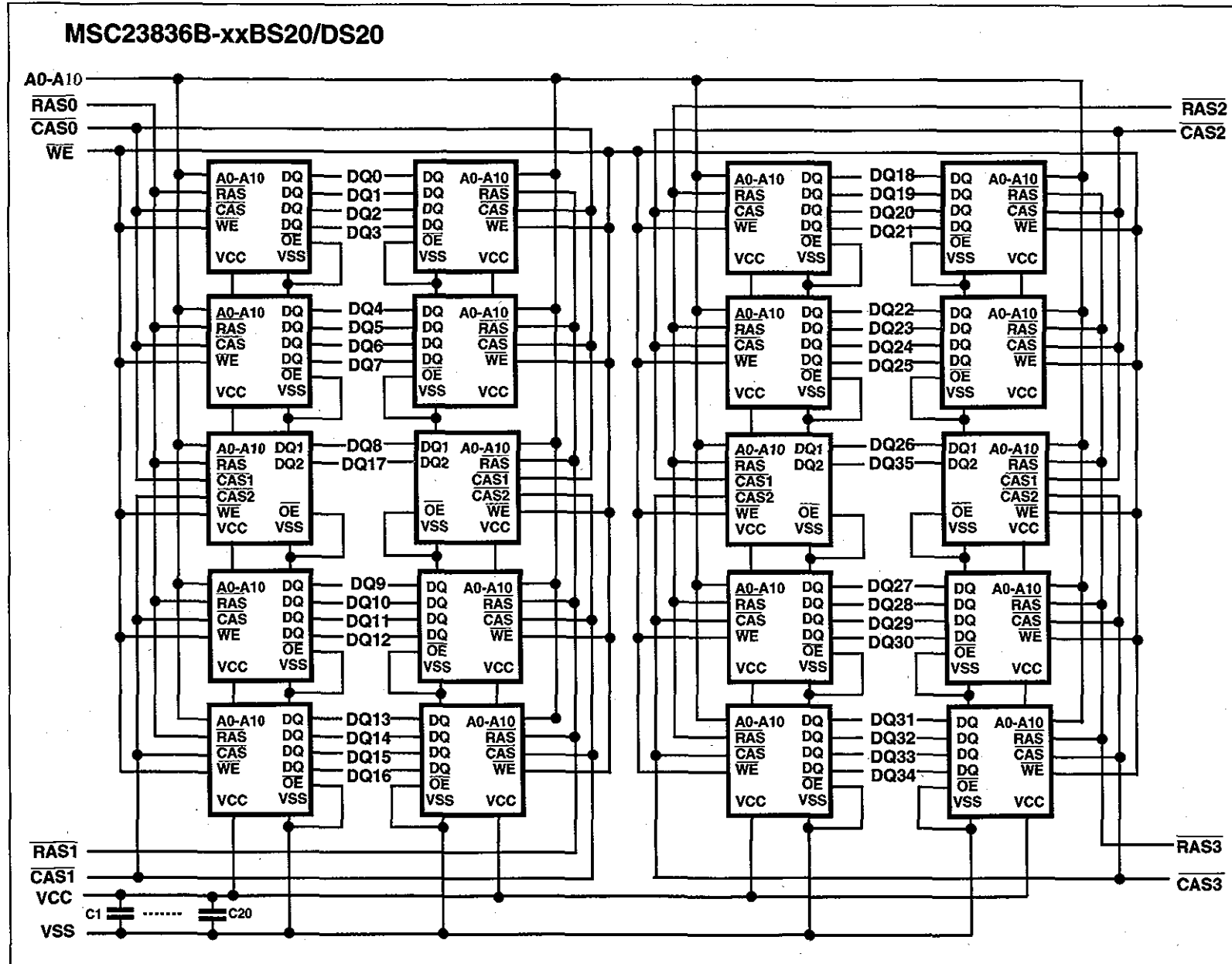
FEATURES

- 8,388,608 word X 36 bit Parity organization
- 72-pin socket insertable module
 - MSC23836B-xxBS20 : Gold tab
 - MSC23836B-xxDS20 : Solder tab
- Single +5 V supply $\pm 10\%$ tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 2048 cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ only refresh capability

FAMILY ORGANIZATION

FAMILY	ACCESS TIME (MAX)			Cycle Time (MAX)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (Max)
MSC23836B-60BS20/DS20	60ns	30ns	15ns	110ns	5995mW	110mW
MSC23836B-70BS20/DS20	70ns	35ns	20ns	130ns	5445mW	(MOS level)

BLOCK DIAGRAM



PIN CONFIGURATION**MSC23836B-xxBS20/DS20**

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	Vss	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	CAS0	58	DQ31
5	DQ19	23	DQ23	41	CAS2	59	Vcc
6	DQ2	24	DQ6	42	CAS3	60	DQ32
7	DQ20	25	DQ24	43	CAS1	61	DQ14
8	DQ3	26	DQ7	44	RAS0	62	DQ33
9	DQ21	27	DQ25	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	RAS3	51	DQ10	69	PD3
16	A4	34	RAS2	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

PRESENCE DETECT PINS

Pin No.	Pin name	-60	-70
67	PD1	NC	NC
68	PD2	Vss	Vss
69	PD3	NC	Vss
70	PD4	NC	NC

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	- 1.0 ~ + 7.0	V
Voltage V _{CC} supply relative to V _{SS}	V _{CC}	- 1.0 ~ + 7.0	V
Short circuit output current	I _{OS}	50	mA
Power dissipation	P _D	20	W
Operating temperature	T _{OPR}	- 0 ~ + 70	°C
Storage temperature	T _{STG}	- 40 ~ + 125	°C

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted within the limits as specified in this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYPE	MAX	UNIT	Operating temperature
Supply Voltage	V _{CC}	4.5	5.0	5.5	V	
	V _{SS}	0	0	0	V	
Input high voltage	V _{IH}	2.4	-	V _{CC} +0.5	V	
Input low voltage	V _{IL}	-0.5	-	0.8	V	

CAPACITANCE

Parameter	Symbol	Typ.	MAX	Unit
Input Capacitance(A0-A10)	C _{IN1}	-	119	pF
Input Capacitance(WE)	C _{IN2}	-	155	pF
Input Capacitance(RAS0-RAS3)	C _{IN3}	-	43	pF
Input Capacitance(CAS0-CAS3)	C _{IN4}	-	50	pF
I/O Capacitance(DQ0-35)	C _{DQ}	-	26	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS(V_{CC} = 5V ± 5%, T_a = 0 ~ +70 °C)

Parameter	Symbol	Condition	MSC23836B-60BS20/DS20		MSC23836B-70BS20/DS20		Unit	Note	
			Min	Max	Min	Max			
Input Leakage Current	I _{LI}	0V ≤ V _{in} ≤ 6.5V: All other pins not under test = 0V	-200	200	-200	200	μA		
Output Leakage Current	I _{LO}	Data out is disable 0V ≤ V _{out} ≤ 5.5V	-20	20	-20	20	μA		
Output High Voltage	V _{OH}	I _{OH} = -5.0mA	2.4	V _{CC}	2.4	V _{CC}	V		
Output Low Voltage	V _{OL}	I _{OL} = 4.2mA	0	0.4	0	0.4	V		
Average power supply current (Operating)	I _{CC1}	RAS cycling, CAS cycling t _{RC} = min	-	1090	-	1000	mA	1,2	
Power supply current (Standby)	I _{CC2}	RAS = V _{IH} CAS = V _{IH}	TTL	-	40	-	40	mA	
			MOS	-	20	-	20	mA	
Average power supply current (RAS only refresh)	I _{CC3}	RAS cycling, CAS = V _{IL} t _{RC} = min	-	1090	-	1000	mA	1	
Average power supply current (CAS before RAS refresh)	I _{CC6}	t _{RC} = min.	-	1090	-	1000	mA	1	
Average power supply current (Fast page)	I _{CC7}	RAS = V _{IL} , CAS cycling t _{PC} = min.	-	970	-	880	mA	1,3	

NOTE:

- I_{CC} is dependent on output loading and cycles rates. Specified values are obtained with the output open.
- Address can be changed once or less while RAS = V_{IL}
- Address can be changed once or less while CAS = V_{IH}

AC CHARACTERISTIC(V_{cc} = 5V ± 10 %, T_a = 0 ~70 °C)

NOTE 1.2.3

Parameter	Symbol	MSC23836B-60BS20/DS20		MSC23836B-70BS20/DS20		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t _{RC}	110	-	130	-	ns	
Fast page mode cycle time	t _{PC}	40	-	45	-	ns	
Access time from RAS	t _{RAC}	-	60	-	70	ns	4,5
Access time from CAS	t _{CAC}	-	15	-	20	ns	4,5
Access time from column address	t _{AA}	-	30	-	35	ns	4,6
Access time from CAS precharge	t _{CPA}	-	35	-	40	ns	4
CAS to output in Low-Z	t _{CLZ}	0	-	0	-	ns	4
Output buffer turn-off delay	t _{OFF}	0	15	0	20	ns	7
Transition time	t _T	3	50	3	50	ns	3
Refresh period	t _{REF}	-	32	-	32	ms	
RAS precharge time	t _{RP}	40	-	50	-	ns	
RAS pulse width	t _{RAS}	60	10K	70	10K	ns	
RAS pulse width (Fast page mode)	t _{RASP}	60	100K	70	100K	ns	
RAS hold time	t _{RSH}	15	-	20	-	ns	
CAS precharge time	t _{CP}	10	-	10	-	ns	
CAS pulse width	t _{CAS}	15	10K	20	10K	ns	
CAS hold time	t _{CSH}	60	-	70	-	ns	
CAS to RAS precharge time	t _{CRP}	10	-	10	-	ns	
RAS to column address delay time	t _{RAD}	15	30	15	35	ns	6
Row address set-up time	t _{ASR}	0	-	0	-	ns	
Row address hold time	t _{RAH}	10	-	10	-	ns	
Column address set-up time	t _{ASC}	0	-	0	-	ns	
Column address hold time	t _{CAH}	15	-	15	-	ns	
Column address to RAS lead time	t _{RAL}	30	-	35	-	ns	

AC CHARACTERISTICS (Continued)
 (V_{cc} = 5V ± 10 %, T_a = 0 ~70 °C)

Parameter	Symbol	MSC23836B-60BS20/DS20		MSC23836B-70BS20/DS20		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Read command set-up time	t _{RCS}	0	-	0	-	ns	
Read command hold time	t _{RCH}	0	-	0	-	ns	8
Read command hold time reference to RAS	t _{RRH}	0	-	0	-	ns	8
Write command set-up time	t _{WCS}	0	-	0	-	ns	
Write command hold time	t _{WCH}	10	-	13	-	ns	
Write command pulse width	t _{WP}	10	-	10	-	ns	
Write command to RAS read time	t _{RWL}	15	-	20	-	ns	
Write command to CAS read time	t _{CWL}	15	-	20	-	ns	
Data-in set-up time	t _{DS}	0	-	0	-	ns	
Data-in hold time	t _{DH}	10	-	15	-	ns	
CAS active delay time from RAS precharge	t _{RPC}	5	-	5	-	ns	
RAS to CAS set-up time (CAS before RAS)	t _{CSR}	10	-	10	-	ns	
CAS hold time (CAS before RAS)	t _{CHR}	10	-	10	-	ns	
WE to RAS precharge time (CAS before RAS)	t _{WRP}	10	-	10	-	ns	
WE hold time from RAS (CAS before RAS)	t _{WRH}	10	-	10	-	ns	
RAS to WE set-up time(test mode)	t _{WTS}	10	-	10	-	ns	
RAS to WE hold time(test mode)	t _{WTH}	10	-	10	-	ns	

- NOTES: 1. A start-up delay of 200 μ s is required after power-up followed by a minimum of 8 initialisation cycles ($\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
When using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
2. AC measurement assume $t_T = 5$ ns.
 3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring input signals. Transition times are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA} .
 7. t_{OFF} defines the time at which time the output achieves an open circuit condition and is not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. The test mode is initiated by performing a WE and before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
The test mode specified in this data sheets is an 8-bit parallel test function. CA10, CA1 and CA0 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level.
If any internal bits are not equal, the DQ pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 10. In a test mode read cycle, the access time parameters are delayed by 5 ns.
The test mode parameters are obtained by adding 5 ns to the normal read cycle values.