

**Diagonal 8.933mm (Type 1/1.8) Frame Readout CCD Image Sensor with Square Pixel for Color Cameras**

**Description**

The ICX252AK is a diagonal 8.933mm (Type 1/1.8) interline CCD solid-state image sensor with a square pixel array and 3.24M effective pixels. Frame readout allows all pixels' signals to be output independently within approximately 1/4.28 second. Also, number of vertical pixels decimation allows output of 30 frames per second in high frame rate readout mode. Ye, Cy, Mg, G complementary color mosaic filters are used as the color filters, and at the same time high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

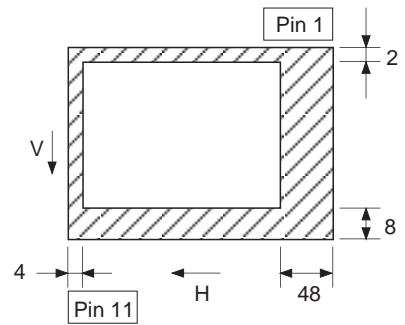
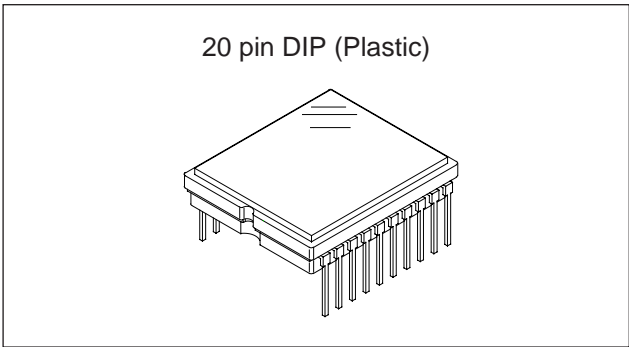
This chip is suitable for applications such as electronic still cameras, etc.

**Features**

- Supports frame readout
- High horizontal and vertical resolution
- Supports high frame rate readout mode: 30 frames/s, AF1 mode: 60 frames/s, 50 frames/s, AF2 mode: 120 frames/s, 100 frames/s
- Square pixel
- Horizontal drive frequency: 18MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- Ye, Cy, Mg, G complementary color mosaic filters on chip
- High sensitivity, low dark current
- Continuous variable-speed shutter
- Excellent anti-blooming characteristics
- 20-pin high-precision plastic package

**Device Structure**

- Interline CCD image sensor
- Total number of pixels: 2140 (H) × 1560 (V) approx. 3.34M pixels
- Number of effective pixels: 2088 (H) × 1550 (V) approx. 3.24M pixels
- Number of active pixels: 2080 (H) × 1542 (V) approx. 3.21M pixels diagonal 8.933mm
- Number of recommended record pixels: 2048 (H) × 1536 (V) approx. 3.15M pixels diagonal 8.832mm aspect ratio 4:3
- Chip size: 8.10mm (H) × 6.64mm (V)
- Unit cell size: 3.45µm (H) × 3.45µm (V)
- Optical black: Horizontal (H) direction: Front 4 pixels, rear 48 pixels  
Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28  
Vertical 1 (even fields only)
- Substrate material: Silicon



**Optical black position (Top View)**

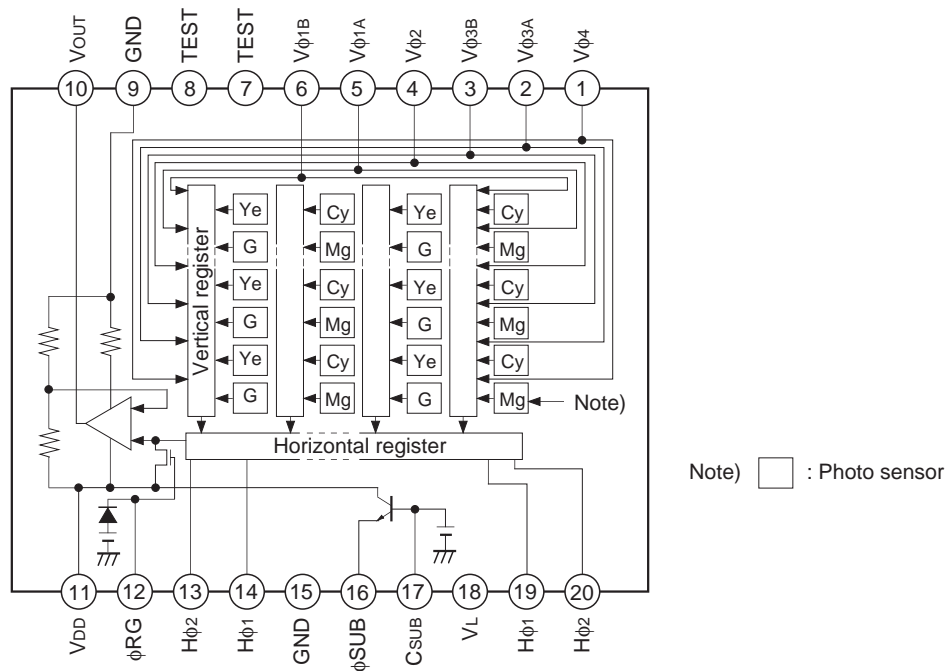
**Super HAD CCD™**

\*Super HAD CCD is a registered trademark of Sony Corporation. Super HAD CCD is a CCD that drastically improves sensitivity by introducing newly developed semiconductor technology by Sony Corporation into Sony's high-performance HAD (Hole-Accumulation Diode) sensor

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**Block Diagram and Pin Configuration**

(Top View)



**Pin Description**

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VDD	Supply voltage
2	Vφ3A	Vertical register transfer clock	12	φRG	Reset gate clock
3	Vφ3B	Vertical register transfer clock	13	Hφ2	Horizontal register transfer clock
4	Vφ2	Vertical register transfer clock	14	Hφ1	Horizontal register transfer clock
5	Vφ1A	Vertical register transfer clock	15	GND	GND
6	Vφ1B	Vertical register transfer clock	16	φSUB	Substrate clock
7	TEST	Test pin*1	17	CSUB	Substrate bias*2
8	TEST	Test pin*1	18	VL	Protective transistor bias
9	GND	GND	19	Hφ1	Horizontal register transfer clock
10	VOUT	Signal output	20	Hφ2	Horizontal register transfer clock

\*1 Leave this pin open.

\*2 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1μF.

## Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against $\phi$ SUB	$V_{DD}$ , $V_{OUT}$ , $\phi$ RG – $\phi$ SUB	–40 to +12	V	
	$V\phi_{1A}$ , $V\phi_{1B}$ , $V\phi_{3A}$ , $V\phi_{3B}$ – $\phi$ SUB	–50 to +15	V	
	$V\phi_2$ , $V\phi_4$ , $V_L$ – $\phi$ SUB	–50 to +0.3	V	
	$H\phi_1$ , $H\phi_2$ , GND – $\phi$ SUB	–40 to +0.3	V	
	$C_{SUB}$ – $\phi$ SUB	–25 to	V	
Against $\phi$ SUB	$V_{DD}$ , $V_{OUT}$ , $\phi$ RG, $C_{SUB}$ – GND	–0.3 to +22	V	
	$V\phi_{1A}$ , $V\phi_{1B}$ , $V\phi_2$ , $V\phi_{3A}$ , $V\phi_{3B}$ , $V\phi_4$ – GND	–10 to +18	V	
	$H\phi_1$ , $H\phi_2$ – GND	–10 to +6.5	V	
Against $V_L$	$V\phi_{1A}$ , $V\phi_{1B}$ , $V\phi_{3A}$ , $V\phi_{3B}$ – $V_L$	–0.3 to +28	V	
	$V\phi_2$ , $V\phi_4$ , $H\phi_1$ , $H\phi_2$ , GND – $V_L$	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–6.5 to +6.5	V	
	$H\phi_1$ , $H\phi_2$ – $V\phi_4$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

\*1 +24V (Max.) when clock width < 10 $\mu$ s, clock duty factor < 0.1%.  
+16V (Max.) is guaranteed for turning on or off power supply.

**Bias Conditions**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	14.55	15.0	15.45	V	
Protective transistor bias	V <sub>L</sub>	*1				
Substrate clock	φ <sub>SUB</sub>	*2				
Reset gate clock	φ <sub>RG</sub>	*2				

\*1 V<sub>L</sub> setting is the V<sub>VL</sub> voltage of the vertical transfer clock waveform, or the same voltage as the V<sub>L</sub> power supply for the V driver should be used.

\*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

**DC Characteristics**

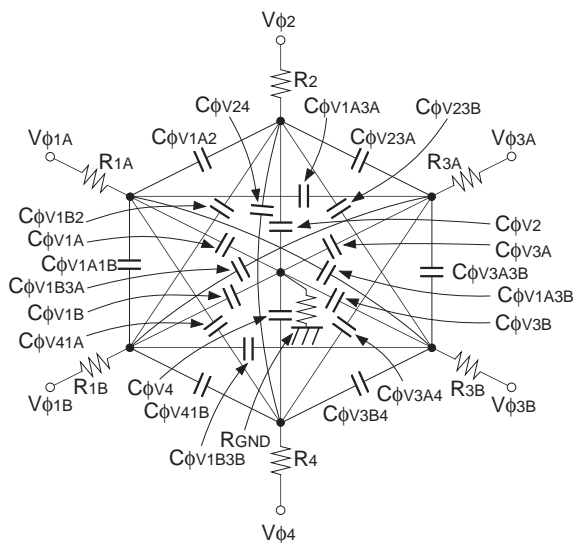
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I <sub>DD</sub>	2.0	4.5	7.0	mA	

**Clock Voltage Conditions**

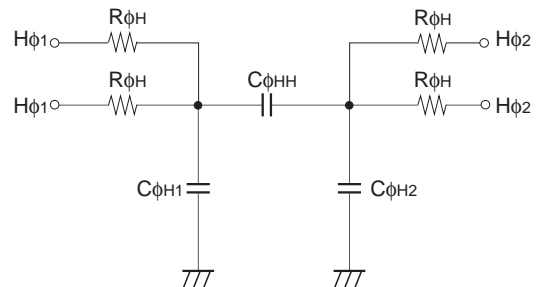
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V <sub>VT</sub>	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V <sub>VH1</sub> , V <sub>VH2</sub>	-0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V <sub>VH3</sub> , V <sub>VH4</sub>	-0.2	0	0.05	V	2	
	V <sub>VL1</sub> , V <sub>VL2</sub> , V <sub>VL3</sub> , V <sub>VL4</sub>	-8.0	-7.5	-7.0	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	V <sub>φV</sub>	6.8	7.5	8.05	V	2	$V_{φV} = V_{VnH} - V_{VnL} (n = 1 \text{ to } 4)$
	V <sub>VH3</sub> - V <sub>VH</sub>	-0.25		0.1	V	2	
	V <sub>VH4</sub> - V <sub>VH</sub>	-0.25		0.1	V	2	
	V <sub>VHH</sub>			0.6	V	2	High-level coupling
	V <sub>VHL</sub>			0.9	V	2	High-level coupling
	V <sub>VLH</sub>			0.9	V	2	Low-level coupling
	V <sub>VLL</sub>			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	V <sub>φH</sub>	4.75	5.0	5.25	V	3	
	V <sub>H</sub> L	-0.05	0	0.05	V	3	
	V <sub>CR</sub>	0.8	2.5		V	3	Cross-point voltage
Reset gate clock voltage	V <sub>φRG</sub>	3.0	3.3	5.25	V	4	
	V <sub>RGLH</sub> - V <sub>RGLL</sub>			0.4	V	4	Low-level coupling
	V <sub>RGL</sub> - V <sub>RGLm</sub>			0.5	V	4	Low-level coupling
Substrate clock voltage	V <sub>φSUB</sub>	21.5	22.5	23.5	V	5	

**Clock Equivalent Circuit Constant**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1A, C\phi V3A$		1500		pF	
	$C\phi V1B, C\phi V3B$		5600		pF	
	$C\phi V2, C\phi V4$		2700		pF	
Capacitance between vertical transfer clocks	$C\phi V1A2, C\phi V3A4$		390		pF	
	$C\phi V1B2, C\phi V3B4$		470		pF	
	$C\phi V23A, C\phi V41A$		120		pF	
	$C\phi V23B, C\phi V41B$		180		pF	
	$C\phi V1A3A$		39		pF	
	$C\phi V1B3B$		220		pF	
	$C\phi V1A3B, C\phi V1B3A$		62		pF	
	$C\phi V24$		75		pF	
	$C\phi V1A1B, C\phi V3A3B$		68		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1, C\phi H2$		36.5		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		88.5		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		8		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		1000		pF	
Vertical transfer clock series resistor	$R1A, R1B, R2, R3A, R3B, R4$		62		$\Omega$	
Vertical transfer clock ground resistor	$R_{GND}$		18		$\Omega$	
Horizontal transfer clock series resistor	$R\phi H$		15		$\Omega$	



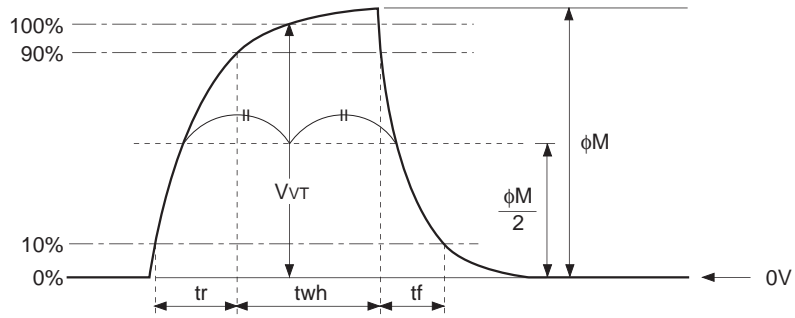
**Vertical transfer clock equivalent circuit**



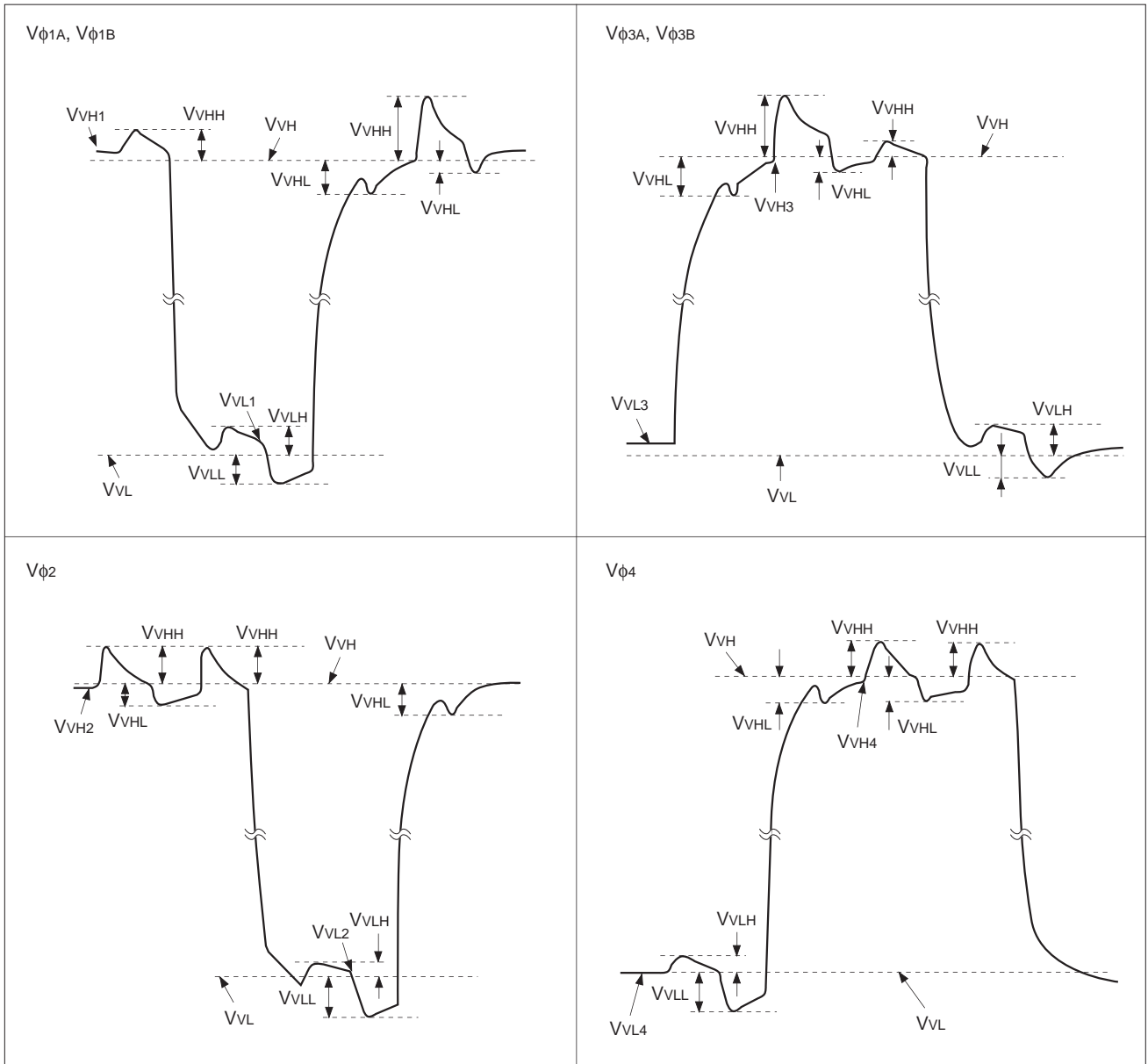
**Horizontal transfer clock equivalent circuit**

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

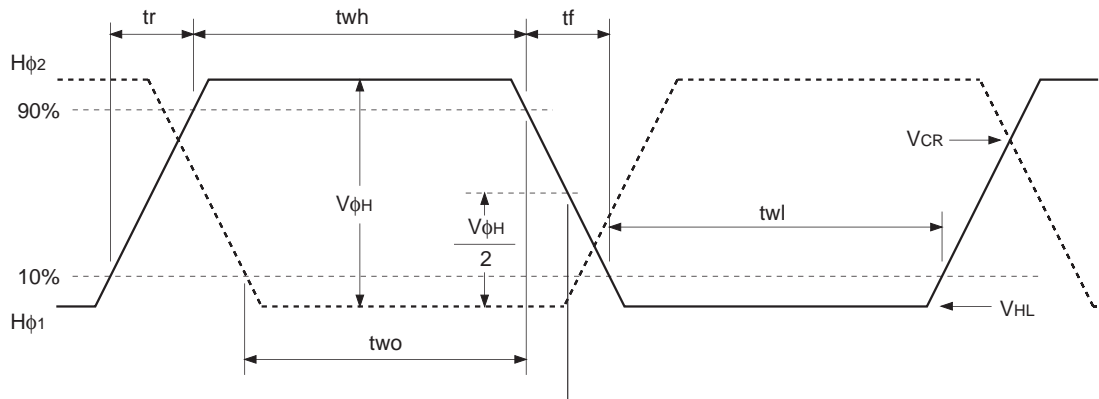


$$V_{VH} = (V_{VH1} + V_{VH2})/2$$

$$V_{VL} = (V_{VLL3} + V_{VLL4})/2$$

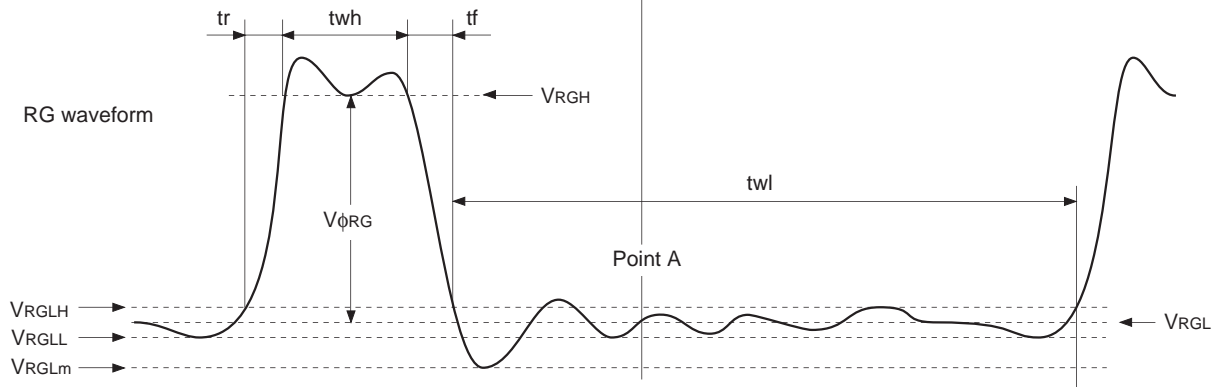
$$V_{\phi V} = V_{VHn} - V_{VLn} \quad (n = 1 \text{ to } 4)$$

**(3) Horizontal transfer clock waveform**



Cross-point voltage for the H $\phi_1$  rising side of the horizontal transfer clocks H $\phi_1$  and H $\phi_2$  waveforms is V<sub>CR</sub>. The overlap period for t<sub>wh</sub> and t<sub>wl</sub> of horizontal transfer clocks H $\phi_1$  and H $\phi_2$  is two.

**(4) Reset gate clock waveform**



VR<sub>GLH</sub> is the maximum value and VR<sub>GLL</sub> is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.

In addition, VR<sub>G</sub>L is the average value of VR<sub>GLH</sub> and VR<sub>GLL</sub>.

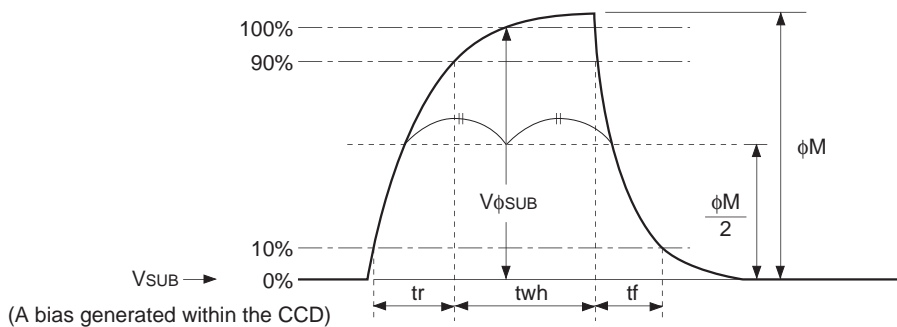
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VR<sub>GH</sub> is the minimum value during the interval t<sub>wh</sub>, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VR<sub>G</sub>L<sub>m</sub>.

**(5) Substrate clock waveform**



**Clock Switching Characteristics** (Horizontal drive frequency: 18MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V <sub>T</sub>	2.63	2.83						0.5			0.5		μs	During readout
Vertical transfer clock	V <sub>φ1A</sub> , V <sub>φ1B</sub> , V <sub>φ2</sub> , V <sub>φ3A</sub> , V <sub>φ3B</sub> , V <sub>φ4</sub>										15		250	ns	When using CXD3400N
Horizontal transfer clock	During imaging	H <sub>φ1</sub>	14	19.5		14	19.5		8.5	14		8.5	14	ns	tf ≥ tr – 2ns
		H <sub>φ2</sub>	14	19.5		14	19.5		8.5	14		8.5	14		
	During parallel-serial conversion	H <sub>φ1</sub>		6.67					0.01			0.01		μs	
		H <sub>φ2</sub>					5.56		0.01			0.01			
Reset gate clock	φ <sub>RG</sub>	7	10			37		4			5		ns		
Substrate clock	φ <sub>SUB</sub>	1.7	3.06							0.5			0.5	μs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H <sub>φ1</sub> , H <sub>φ2</sub>	12	19.5		ns	

**Spectral Sensitivity Characteristics** (excludes lens characteristics and light source characteristics)

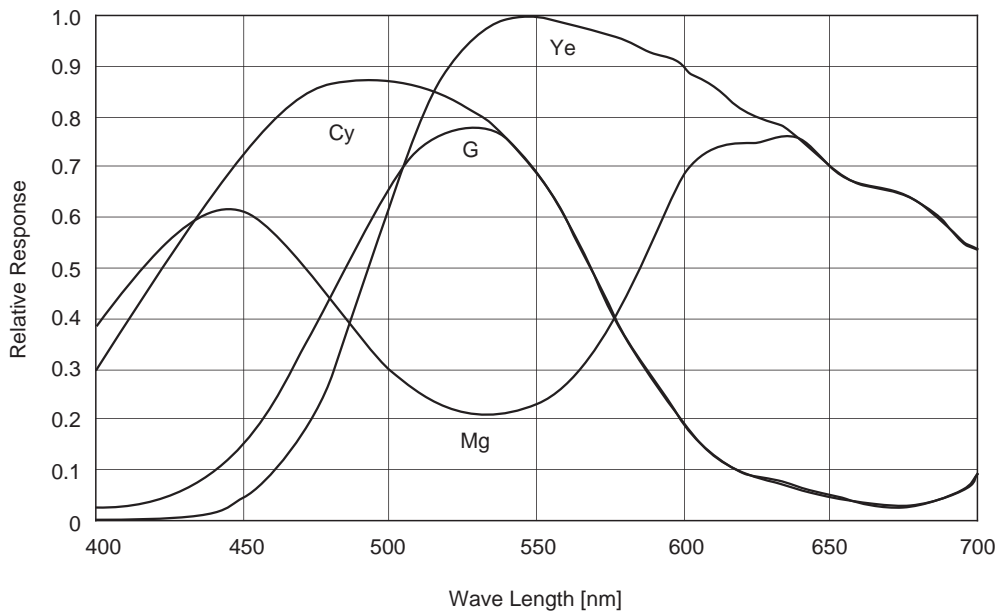




Image Sensor Characteristics (Horizontal drive frequency: 18MHz)

(Ta = 25°C)

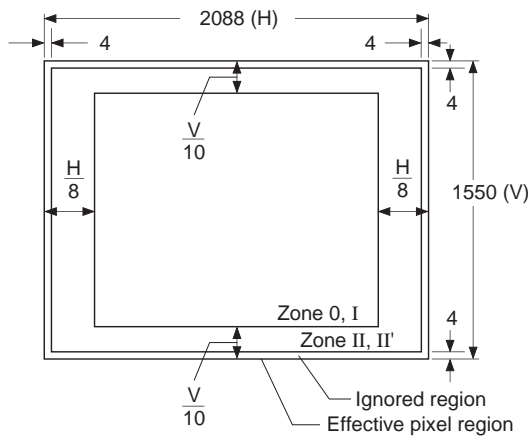
Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	256	320		mV	1	1/30s accumulation
Sensitivity comparison	RMgG	0.75		1.35		2	
	RYeCy	1.15		1.48			
Saturation signal	Vsat	400			mV	3	Ta = 60°C, *1
Smear	Sm		-89.1	-81.2	dB	4	Frame readout mode, *2
			-79.6	-71.6			High frame rate readout mode
Video signal shading	SH			20	%	5	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			12	mV	6	Ta = 60°C, 7.5frame/s
Dark signal shading	$\Delta Vdt$			6	mV	7	Ta = 60°C, 7.5frame/s, *3
Lag	Lag			0.5	%	8	

\*1 The saturation signal level is 450mV or more by performing pull-down C<sub>SUB</sub> pin at 1.3kΩ resistor. For high frame rate readout mode, it is 800mV.

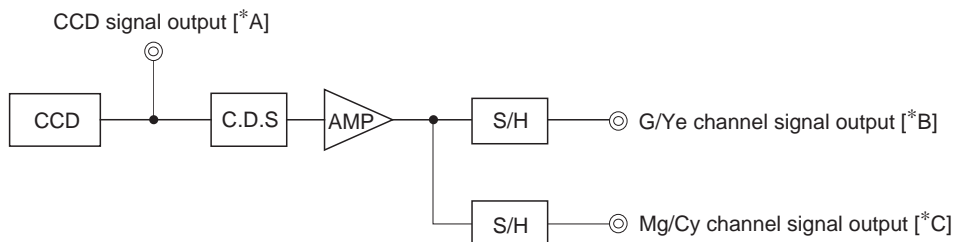
\*2 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation.

\*3 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System



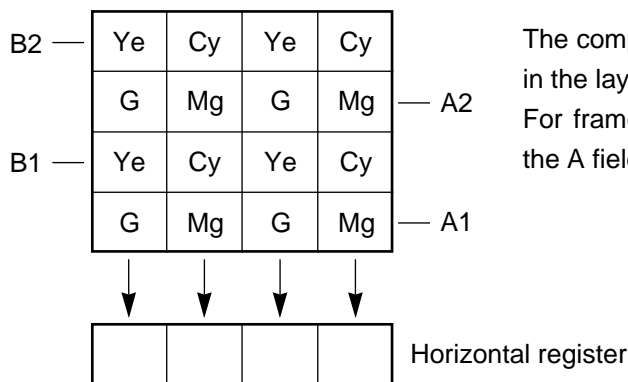
Note) Adjust the amplifier gain so that the gain between [\*A] and [\*B], and between [\*A] and [\*C] equals 1.

**Image Sensor Characteristics Measurement Method**

◎ **Measurement conditions**

- 1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used.
- 2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the G/Ye channel signal output or the Mg/Cy channel signal output of the measurement system.

◎ **Color coding of this image sensor & Readout**



The complementary color filters of this image sensor are arranged in the layout shown in the figure on the left. For frame readout, the A1 and A2 lines are output as signals in the A field, and the B1 and B2 lines in the B field.

**Color Coding Diagram**

These signals are processed to form the Y signal and chroma (color difference) signal as follows.

The approximation:

$$Y = \{G + Mg + Ye + Cy\} \times 1/4$$

$$= 1/4 \{2B + 3G + 2R\}$$

is used for the Y signal, and the approximation:

$$R - Y = \{(Mg + Ye) - (G + Cy)\}$$

$$= \{2R - G\}$$

$$B - Y = \{(Mg + Cy) - (G + Ye)\}$$

$$= \{2B - G\}$$

are used for the chroma (color difference) signal.

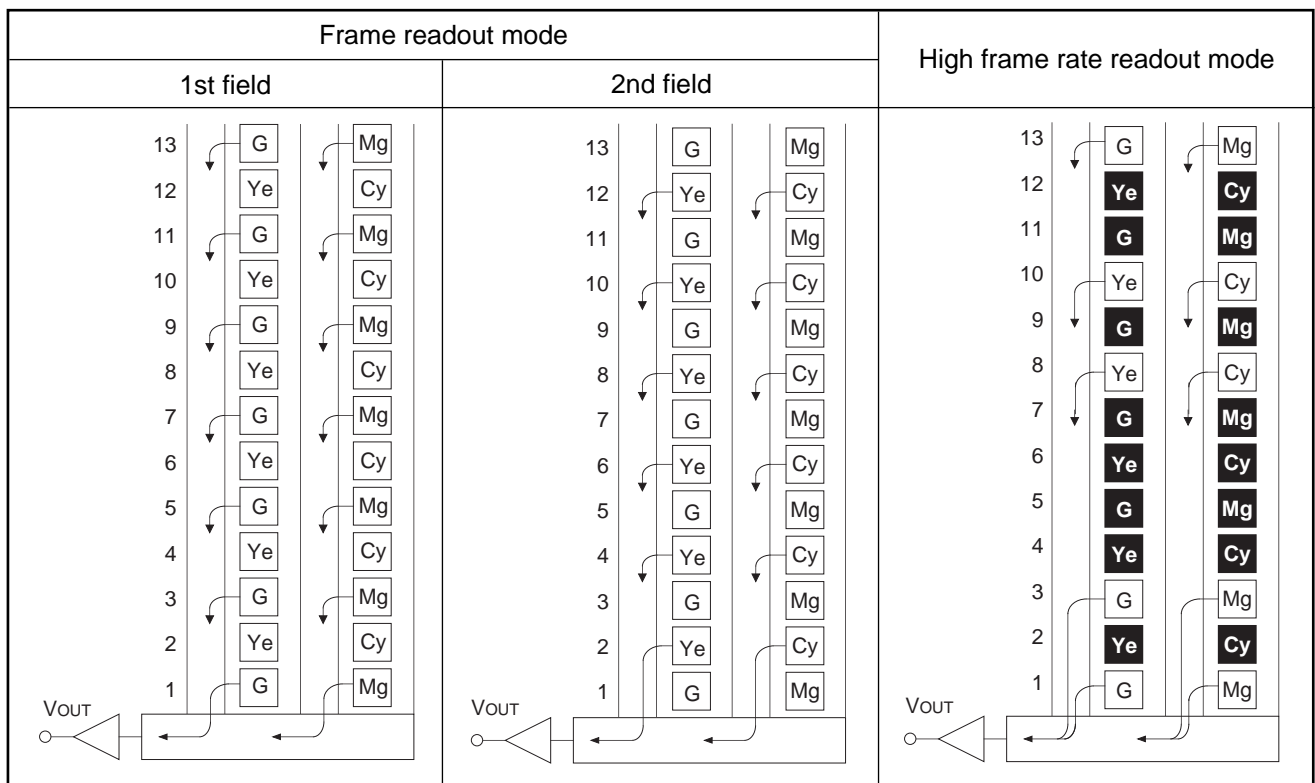
© Readout modes

1. Readout modes list

The following readout modes are possible by driving the image sensor at the timing specifications noted in this Data Sheet.

Mode name		Frame rate	Number of output effective lines
Frame readout mode	NTSC mode	4.28 frame/s	1550 (Odd 775, Even 775)
	PAL mode	4.16 frame/s	1550 (Odd 775, Even 775)
High frame rate readout mode	NTSC mode	30 frame/s	258
	PAL mode	25 frame/s	258
AF1 mode	NTSC mode	60 frame/s	See Page.12
	PAL mode	50 frame/s	See Page.12
AF2 mode	NTSC mode	120 frame/s	See Page.12
	PAL mode	100 frame/s	See Page.12

2. Frame readout mode, high frame rate readout mode



**Note)** Blacked out portions in the diagram indicate pixels which are not read out.

1. Frame readout mode

In this mode, all pixel signals are divided into two fields and output.

All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode

Output is performed at 30 frames per second by reading out 4 pixels for every 12 vertical pixels and adding 2 pixels in the horizontal CCD.

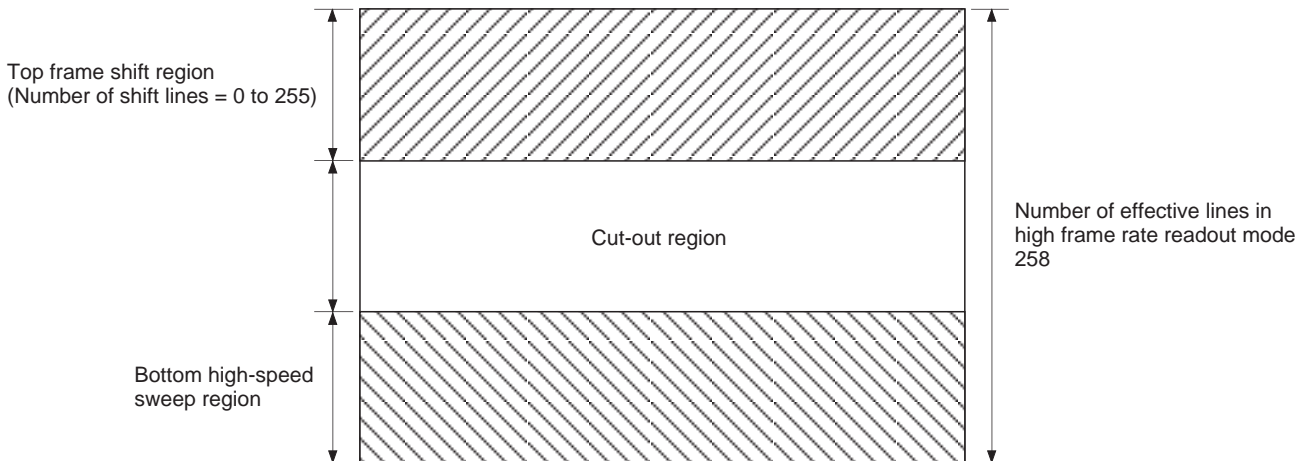
The number of output lines is 258 lines.

This readout mode emphasizes processing speed over vertical resolution.

**3. AF1 mode, AF2 mode**

The AF modes increase the frame rate by cutting out a portion of the picture through high-speed elimination of the top and bottom of the picture in high frame rate readout mode. AF1 allows 1/60s and 1/50s output, and AF2 allows 1/120s and 1/100s output, so these modes are effective for raising the auto focus (AF) speed.

In addition, the cut-out can begin from an optional line by controlling the number of frame shift lines that sweep the top of the picture. The relation between the number of frame shift lines, the output start position and number of output lines is shown in the table below.



	AF1 mode		AF2 mode	
	NTSC	PAL	NTSC	PAL
Frame rate	1/60s	1/50s	1/120s	1/100s
Output start position on timing chart	26H	26H	30H	30H
Number of frame shift lines	i = 0 to 255			
Output lines*1	i + 3 to i + 108	i + 3 to i + 134	i + 3 to i + 38	i + 3 to i + 47

\*1 Output line is Up to 258 lines.

The i + 1 and i + 2 line signals may be disrupted by elimination of the picture top, so these lines should not be used.

For example, if the picture top is eliminated with i = 100 in AF1 mode (NTSC), lines 103 to 208 in high frame rate readout mode are output from 26H of the timing chart.

If the picture top is eliminated with i = 160 in AF1 mode (NTSC), lines 163 to 258 in high frame rate readout mode are output from 26H of the timing chart.

## ◎ Definition of standard imaging conditions

### 1) Standard imaging condition I:

Use a pattern box (luminance: 706cd/m<sup>2</sup>, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

### 2) Standard imaging condition II:

Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

### 1. Sensitivity

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs ( $V_G$ ,  $V_{Mg}$ ,  $V_{Ye}$  and  $V_{Cy}$ ) at the center of each G, Mg, Ye and Cy channel screen, and substitute the values into the following formulas.

$$V = (V_G + V_{Mg} + V_{Ye} + V_{Cy})/4$$

$$S = V \times \frac{100}{30} \text{ [mV]}$$

### 2. Sensitivity comparison

Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the G/Mg/Ye/Cy channel signal output is 150mV, and then measure the Mg signal output ( $S_{Mg}$  [mV]) and G signal output ( $S_G$  [mV]), and the Ye signal output ( $S_{Ye}$  [mV]) and Cy signal output ( $S_{Cy}$  [mV]) at the center of the screen. Substitute the values into the following formulas.

$$R_{MgG} = S_{Mg}/S_G$$

$$R_{YeCy} = S_{Ye}/S_{Cy}$$

### 3. Saturation signal

Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the G/Mg/Ye/Cy channel signal output, 150mV, measure the minimum values of the G, Mg, Ye and Cy signal outputs.

### 4. Smear

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of the G/Mg/Ye/Cy channel signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value ( $V_{sm}$  [mV]) independent of the G, Mg, Ye and Cy signal outputs, and substitute the values into the following formula.

$$S_m = 20 \times \log \left( \frac{V_{sm}}{150} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB]} \text{ (1/10V method conversion value)}$$

5. Video signal shading

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the G/Mg/Ye/Cy channel signal output is 150mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the G/Mg/Ye/Cy channel signal output and substitute the values into the following formula.

$$SH = (V_{max} - V_{min}) / 150 \times 100 [\%]$$

6. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading

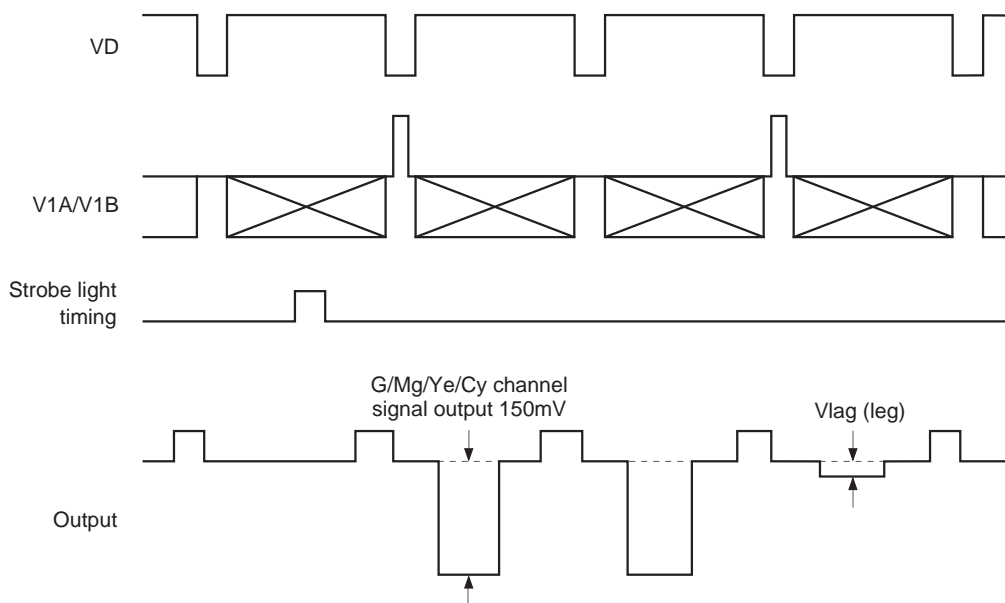
After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} [mV]$$

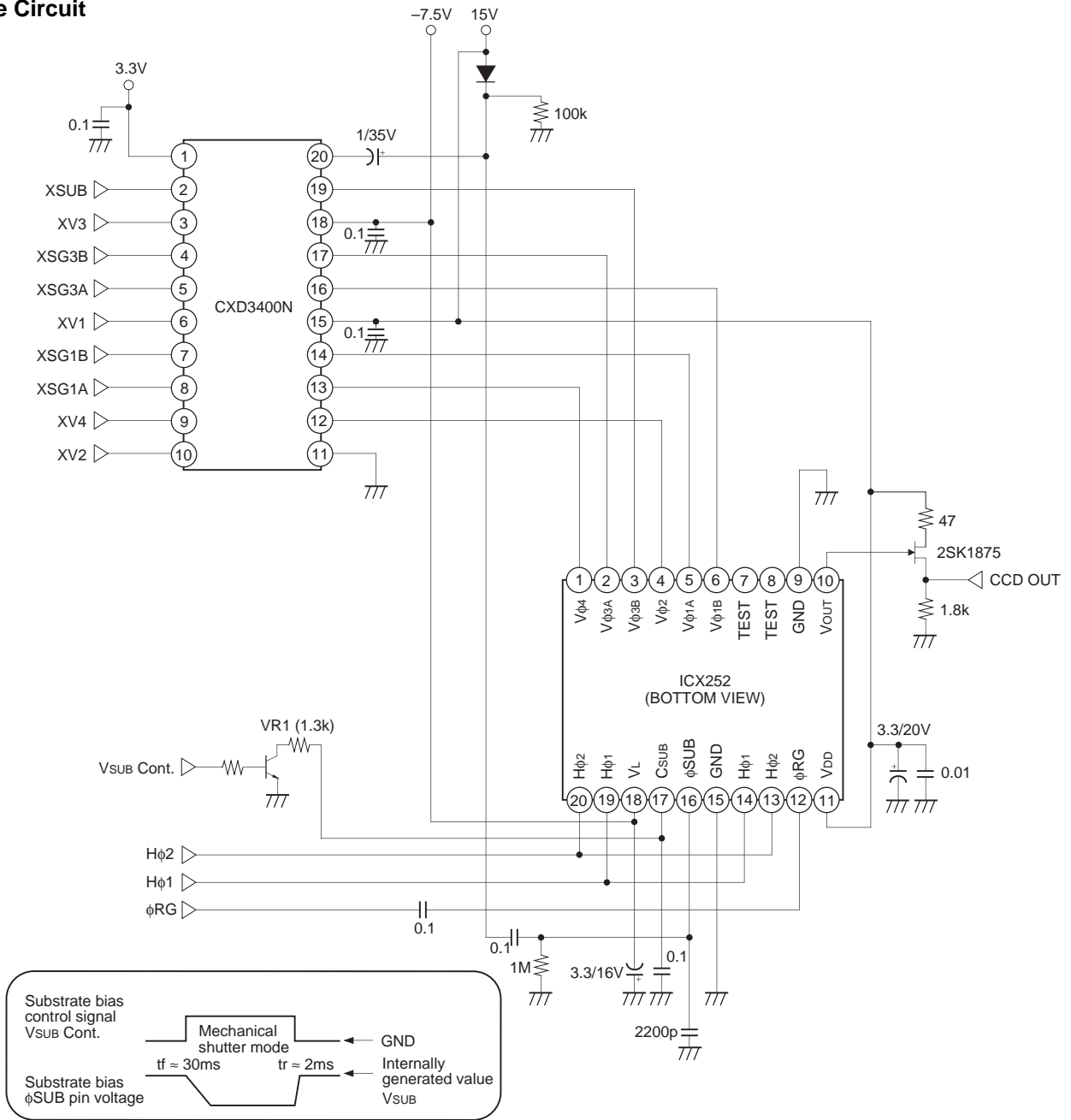
8. Lag

Adjust the G/Mg/Ye/Cy channel signal output generated by strobe light to 150mV. After setting the strobe light so that it strobos with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

$$Lag = (V_{lag}/150) \times 100 [\%]$$



Drive Circuit



Notes)

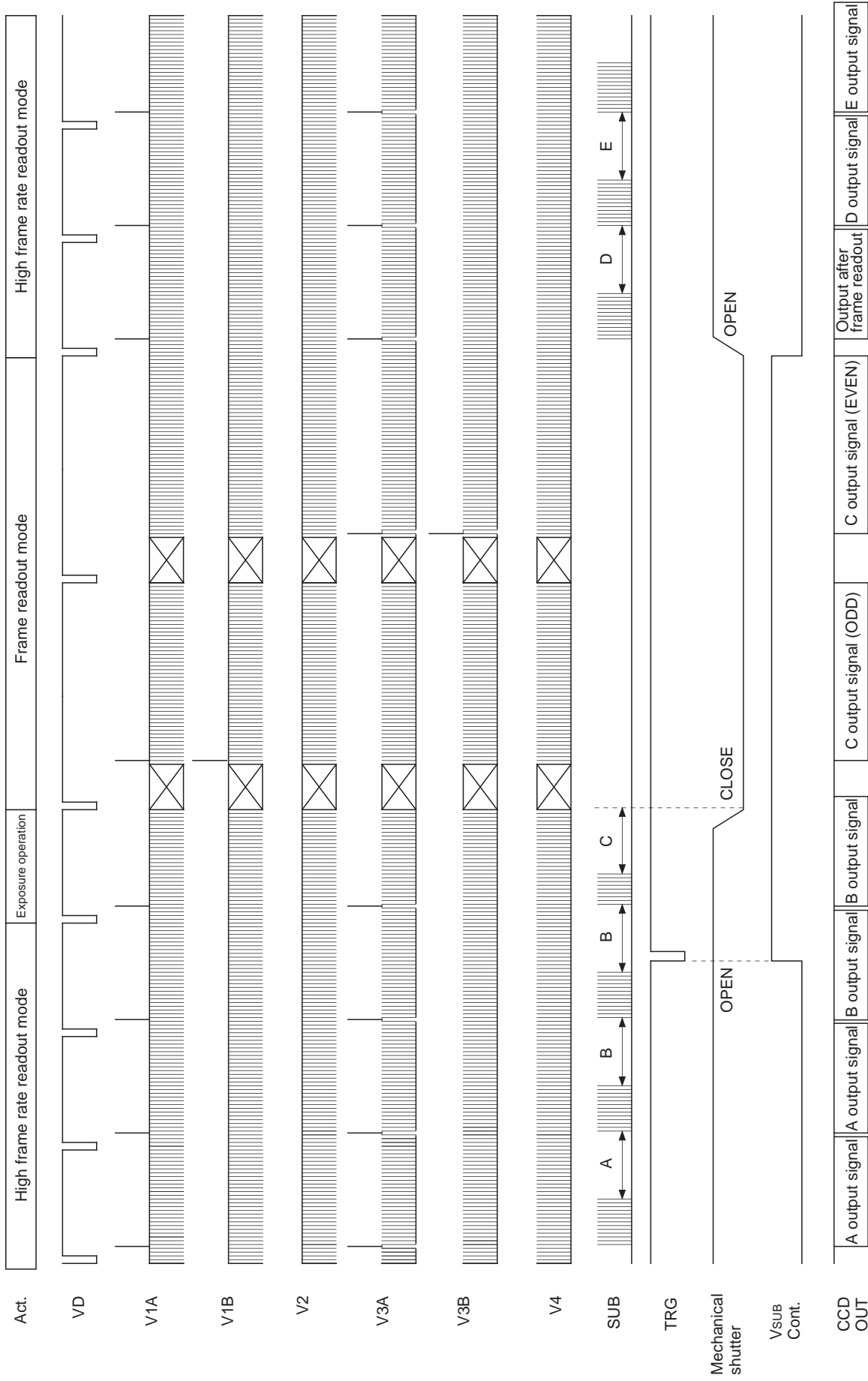
Substrate bias control

1. The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.
2. A saturation signal level equivalent to that for continuous exposure can be assured by connecting a 1.3kΩ grounding resistor to the CCD CSUB pin.

Drive timing precautions

1. Blooming occurs in modes (high frame rate readout, etc.) that do not use the mechanical shutter, so do not ground the connected 1.3kΩ resistor.
2. tf is slow, so the internally generated voltage VsUB may not drop to a sufficiently low level if the substrate bias control signal is not set to high level 40ms before entering the exposure period and the 1.3kΩ resistor connected to the CSUB pin is not grounded.
3. The blooming signal generated during exposure in mechanical shutter mode is swept by providing one field or more of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the VL potential and the φSUB pin DC voltage sag at this time.

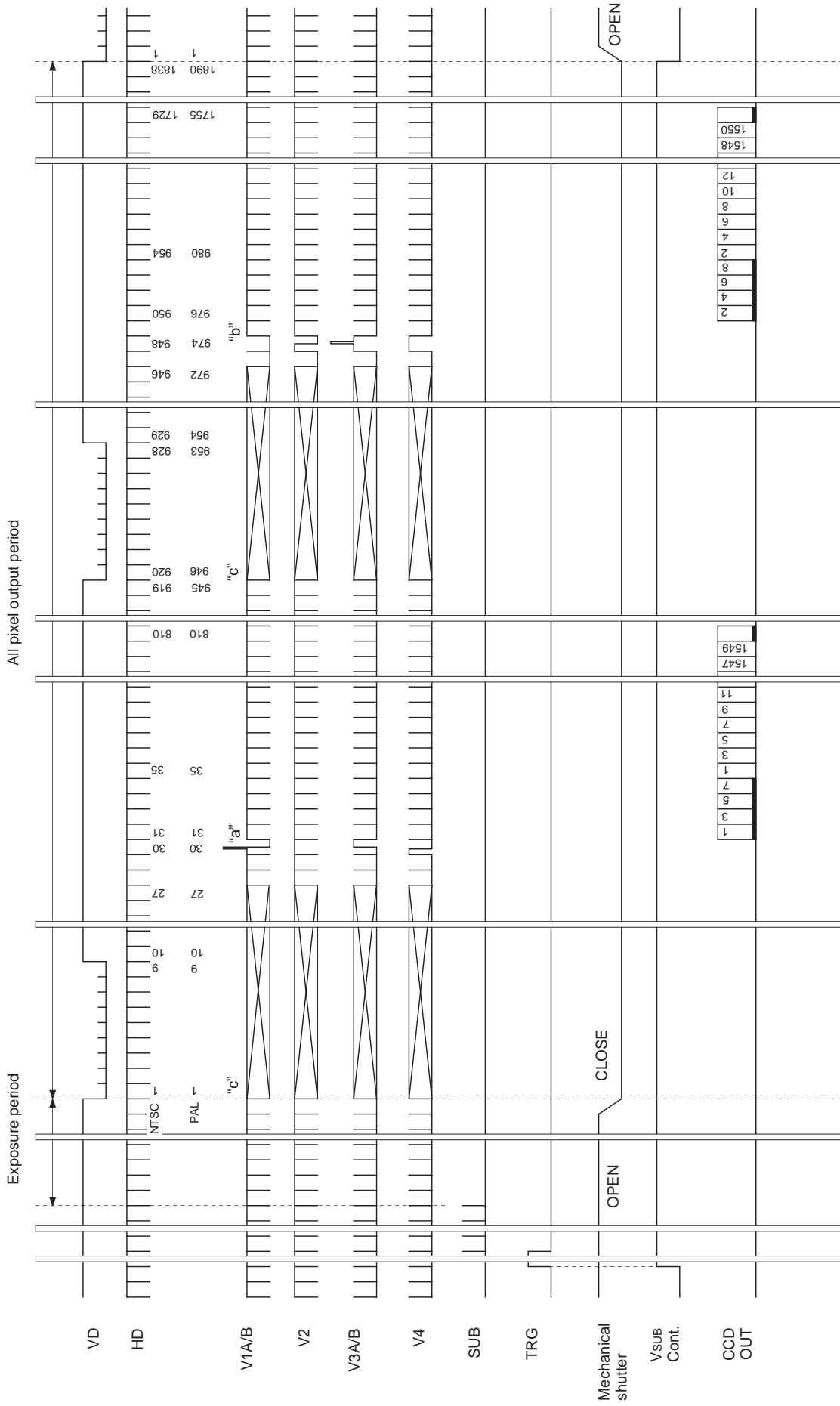
Drive Timing Chart (Vertical Sequence) High Frame Rate Readout Mode → Frame Readout Mode/Electronic Shutter Normal Operation



**Note)** The B output signal contains a blooming component and should therefore not be used.

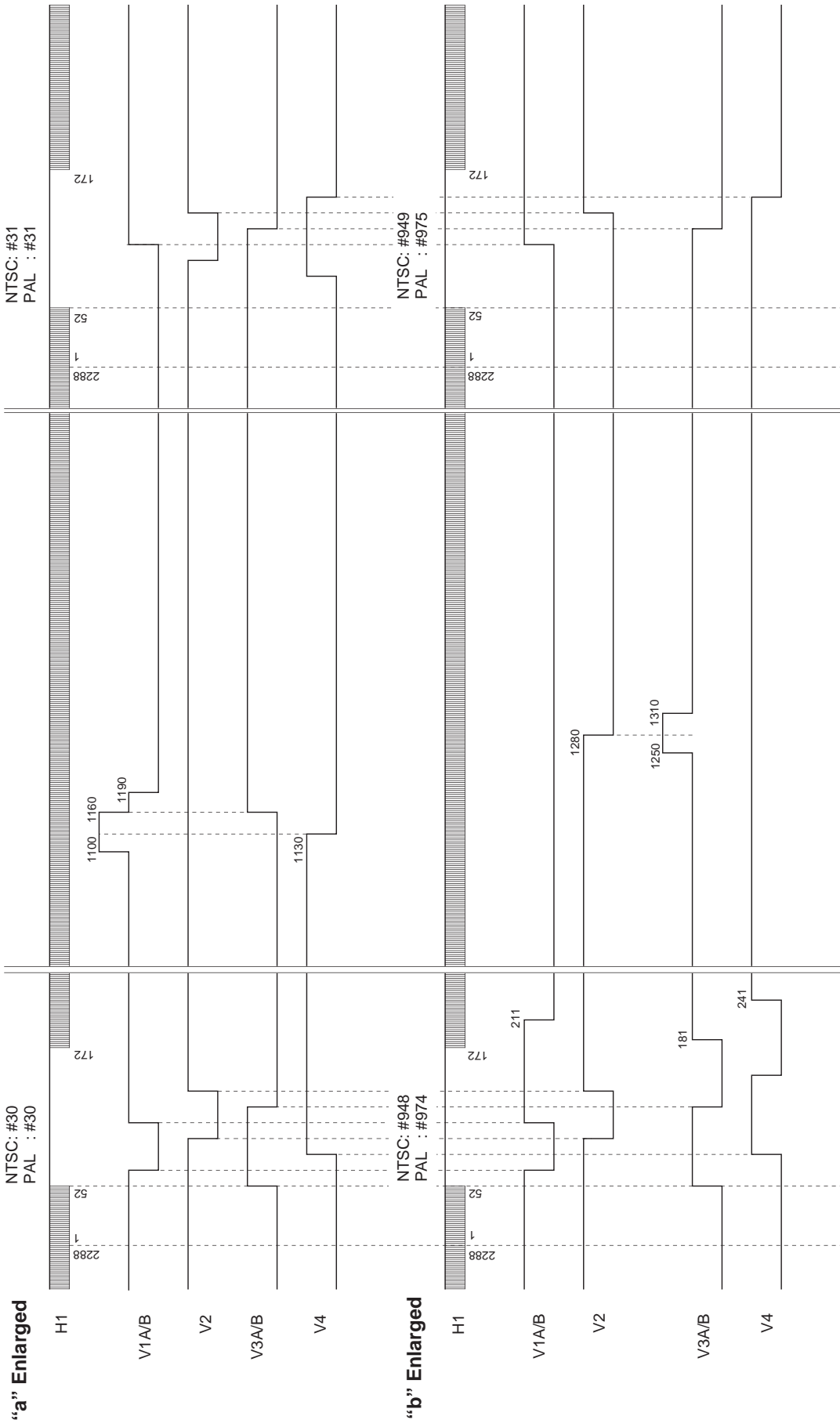


**Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode**  
**NTSC: 4.28 frame/s, PAL: 4.17 frame/s**

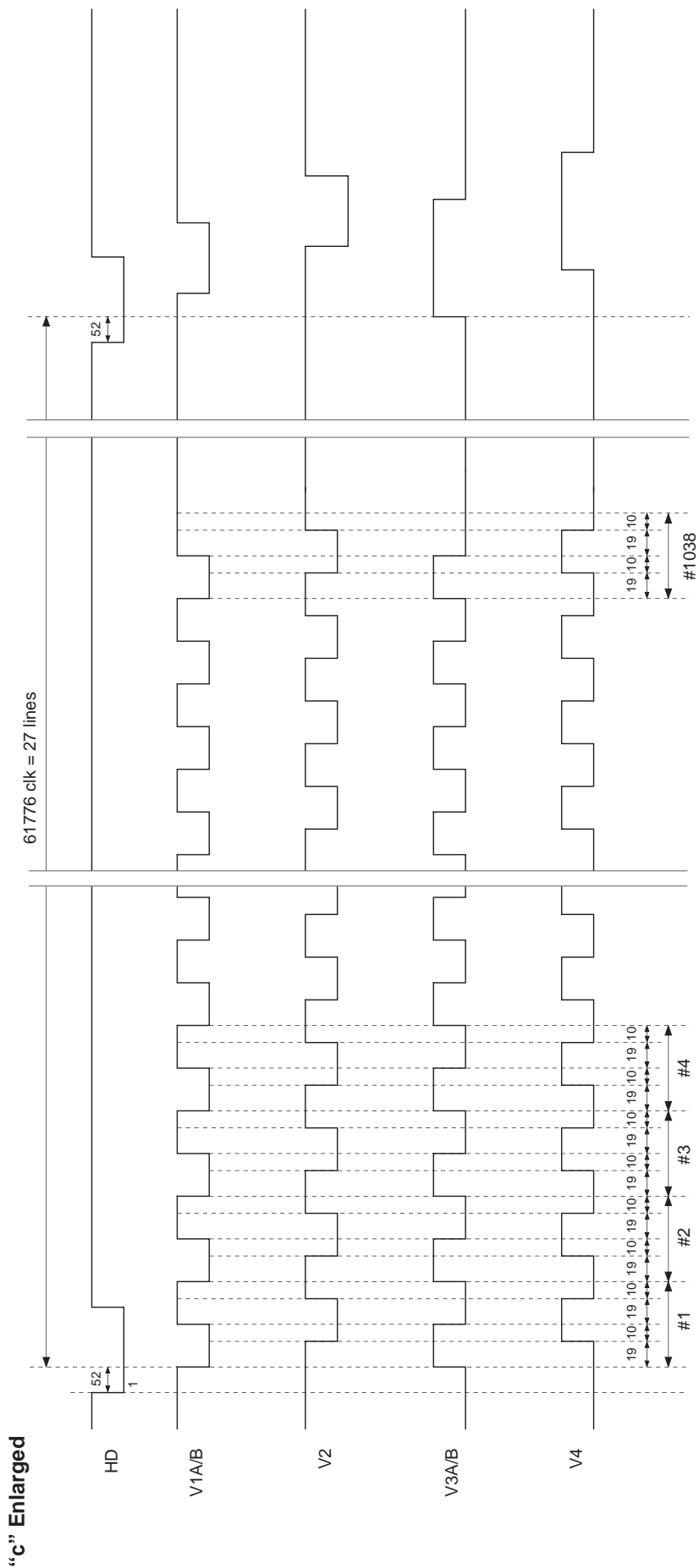


**Note)** 2288fH, However, 919H and 1828H in NTSC mode are 1716 clk, and 944H, 945H, 1889H and 1890H in PAL mode are 1208 clk.

Drive Timing Chart (Readout) NTSC/PAL Frame Readout Mode

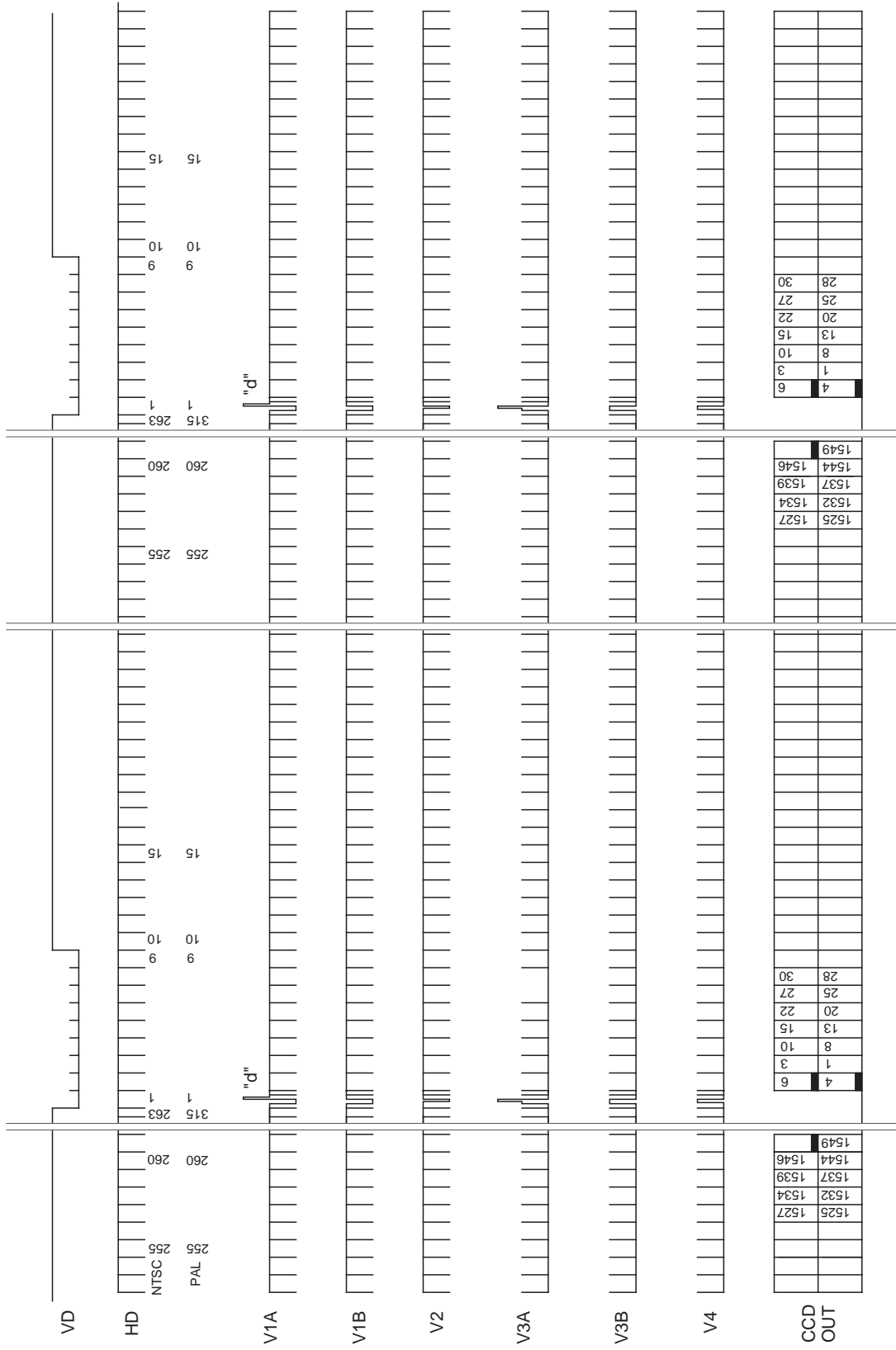


Drive Timing Chart (High-speed Sweep Operation) NTSC/PAL Frame Readout Mode





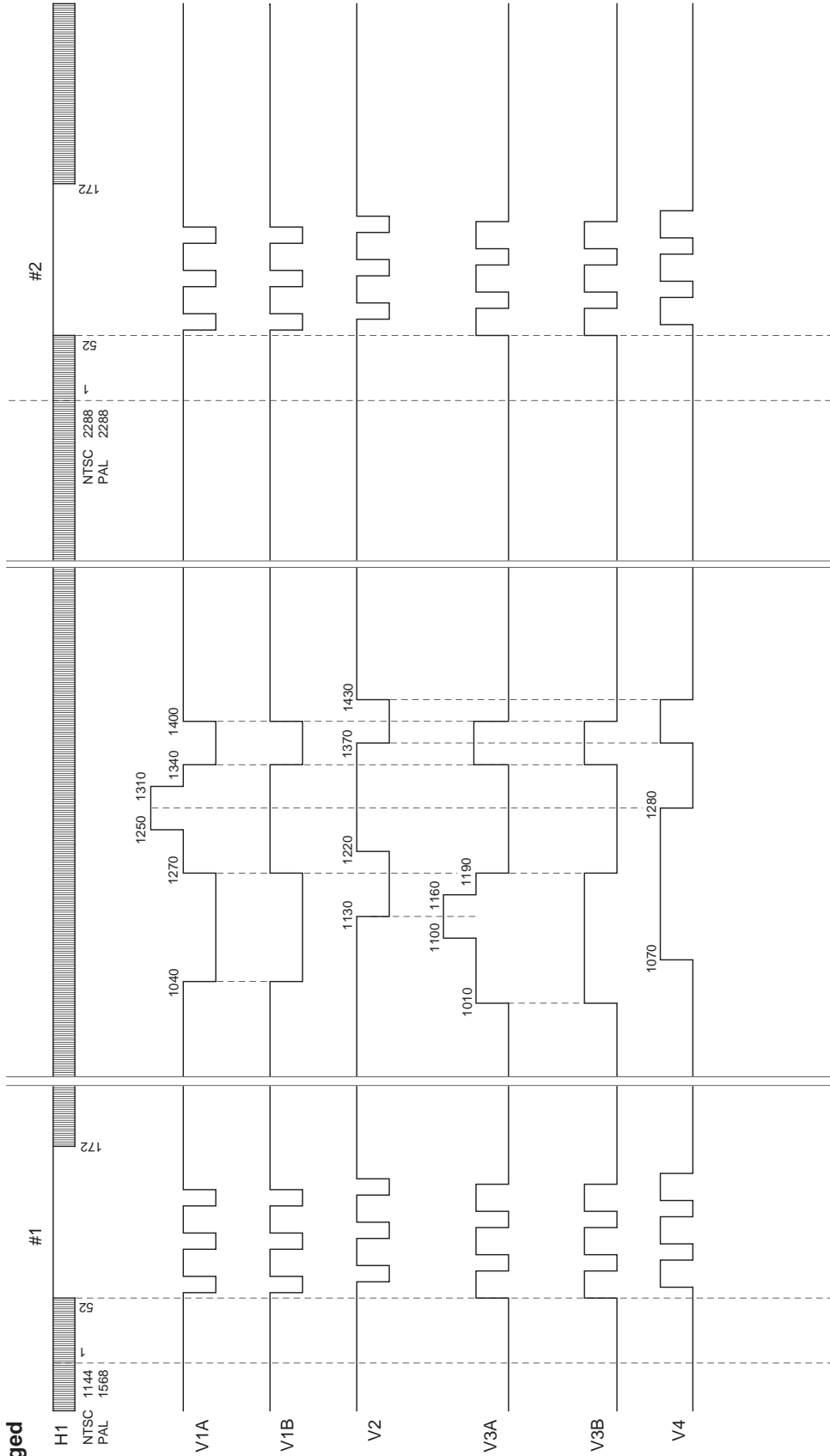
Drive Timing Chart (Vertical Sync) NTSC/PAL High Frame Rate Readout Mode  
 NTSC: 30 frame/s, PAL: 25 frame/s



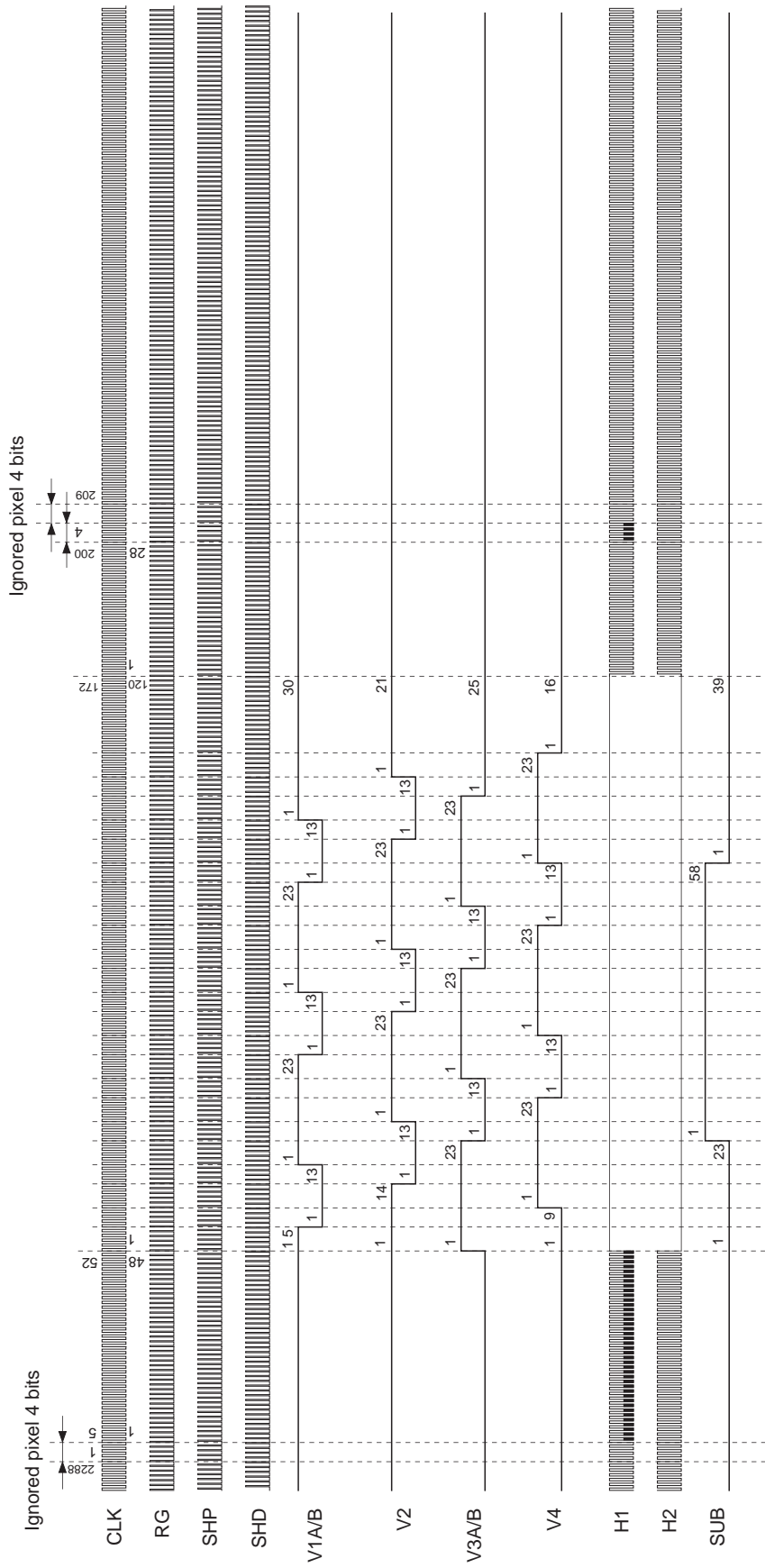
**Note)** 2288fH, However, 263H in NTSC mode is 1144 clk, and 315H in PAL mode is 1568 clk.

Drive Timing Chart (Readout) NTSC/PAL High Frame Rate Readout Mode

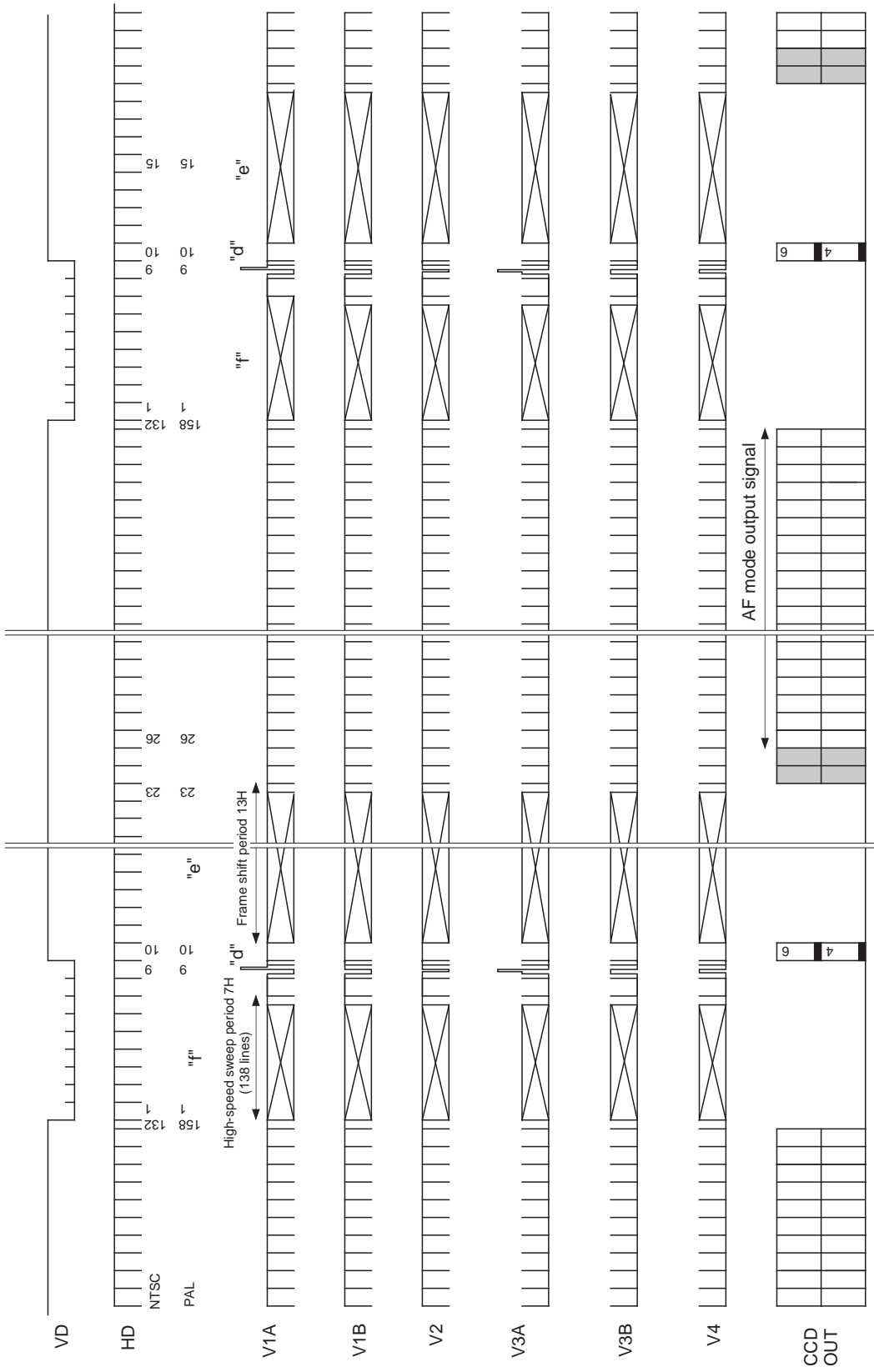
“d” Enlarged



Drive Timing Chart (Horizontal Sync) NTSC/PAL High Frame Rate Readout Mode, AF1 Mode, AF2 Mode



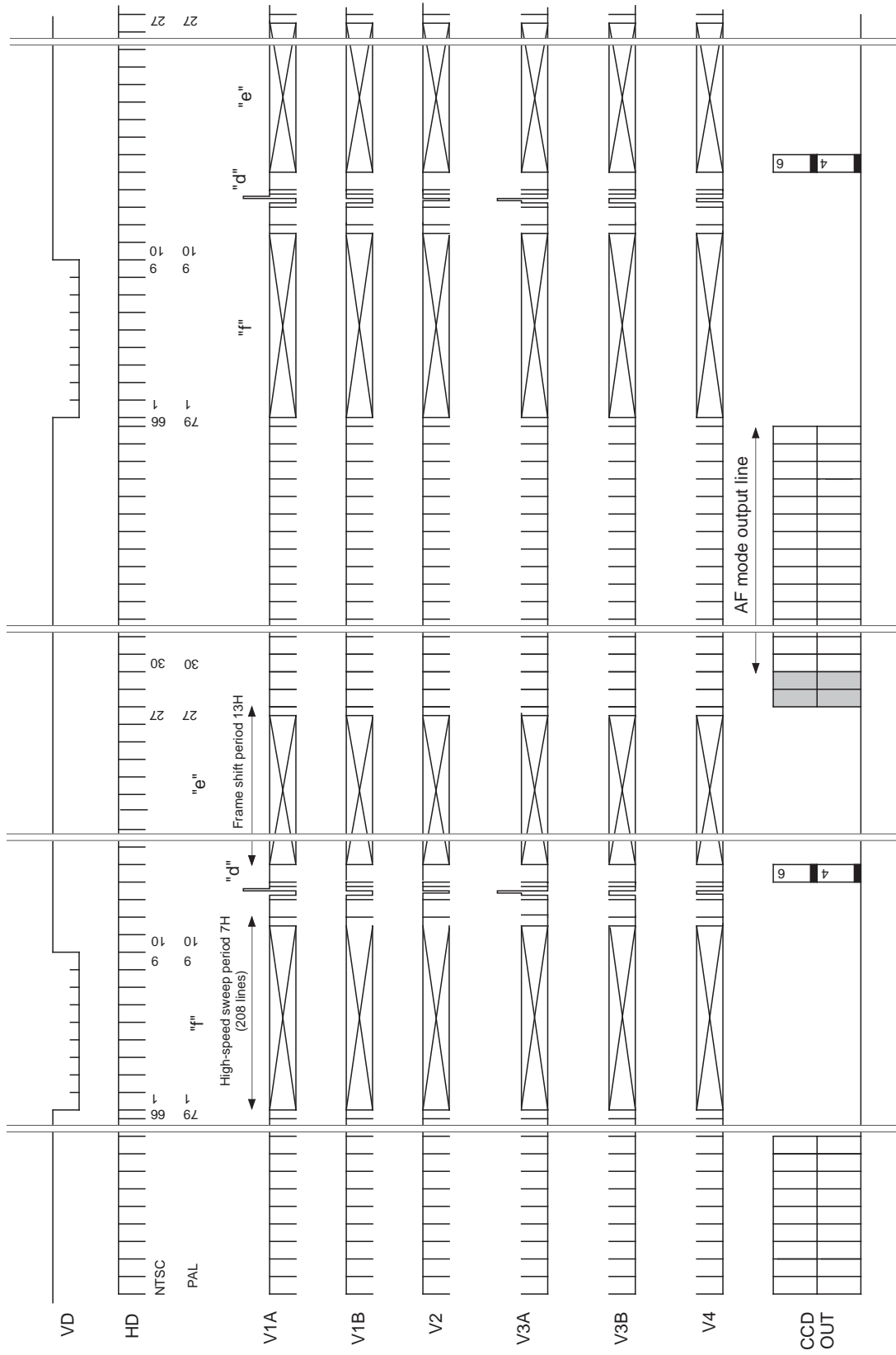
**Drive Timing Chart (Vertical Sync) NTSC/PAL AF1 Mode**  
**NTSC: 60 frame/s, PAL: 50 frame/s**



**Note)** 2288fH, However, 182H in NTSC mode is 572 clk, and 158H in PAL mode is 784 clk.



**Drive Timing Chart (Vertical Sync) NTSC/PAL AF2 Mode**  
**NTSC: 120 frame/s, PAL: 100 frame/s**

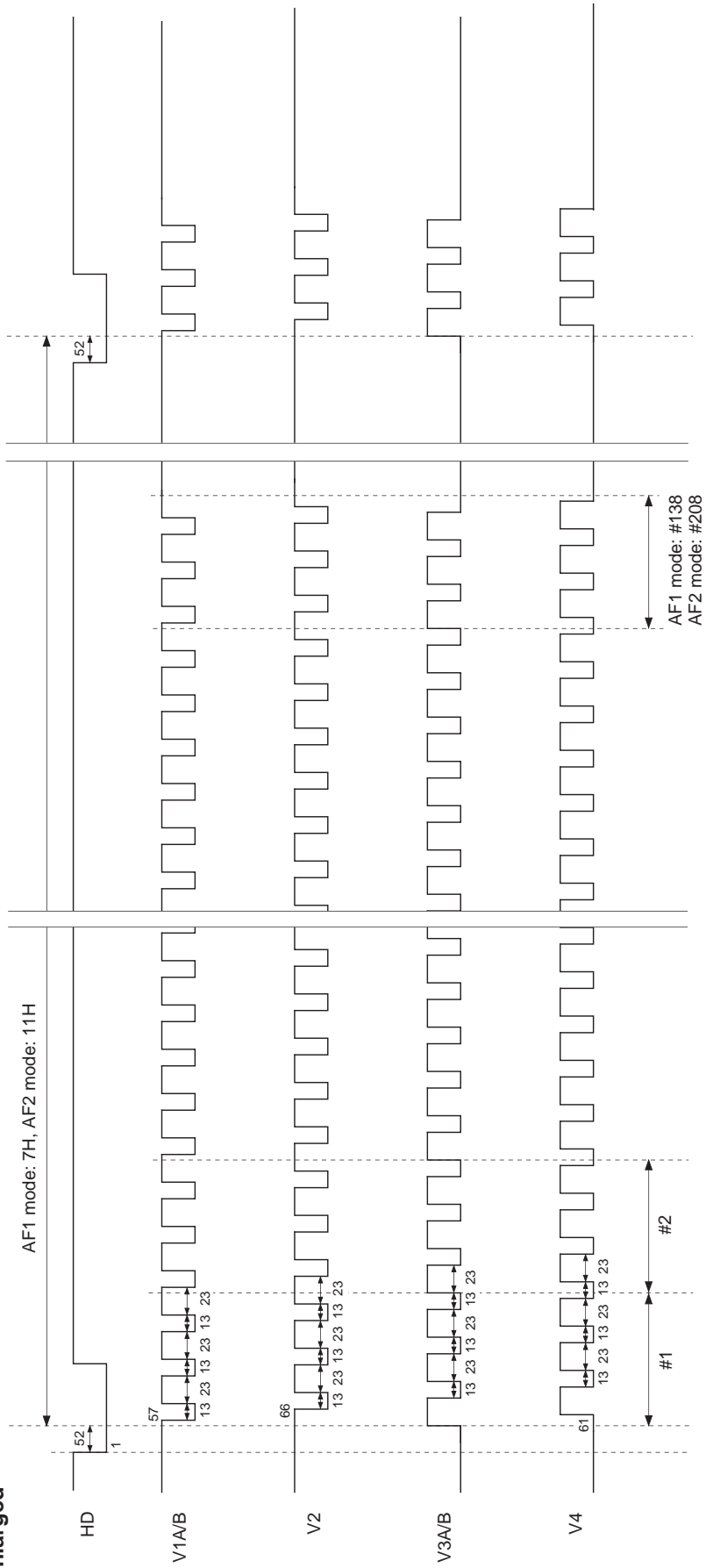


**Note)** 2288fH, However, 66H in NTSC mode is 1430 clk, and 79H in PAL mode is 1356 clk.



Drive Timing Chart (High-speed Sweep Operation) NTSC/PAL AF1 Mode, AF2 Mode

“f” Enlarged



## Notes on Handling

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material.  
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensors.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

### 2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

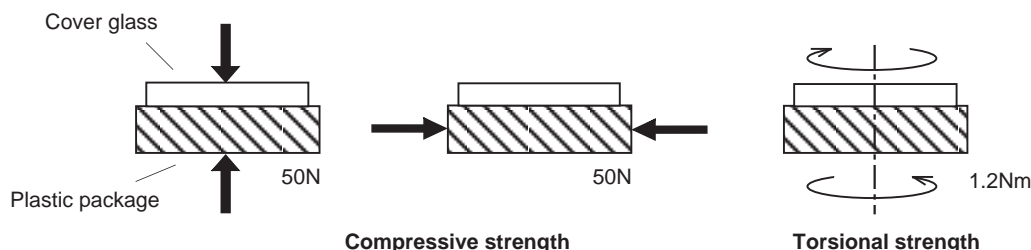
### 3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.

- a) Perform all assembly operations in a clean room (class 1000 or less).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

### 4) Installing (attaching)

- a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



- b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

- c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
- d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
- e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
- f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

#### 5) Others

- a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
- b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

