DATA SHEET

CGY2106TS
High dynamic range dual LNA MMIC

Preliminary specification
File under Integrated Circuits, IC17

2000 Aug 28

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FEATURES

- Dual Low Noise Amplifier (LNA) Monolithic Microwave Integrated Circuit (MMIC)
- Typical noise figure 0.5 dB
- Typical gain of 16.1 dB at 860 MHz
- Input IP3 of 14 dBm at 860 MHz
- Low current (78 mA per channel at 2.0 V)
- Low cost SSOP16 plastic package.

APPLICATIONS

- GSM base station.

GENERAL DESCRIPTION

The CGY2106TS is a dual Gallium Arsenide (GaAs) MMIC amplifier designed for very low noise figure applications, where high linearity is also required.

Excellent tracking between the two amplifiers is obtained. Gain and noise figure variations are well controlled with temperature.

The device is suitable for use in GSM base stations and other applications where high gain linearity and very low noise are required.

The application board might need to be rematched for optimum performance.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2106TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

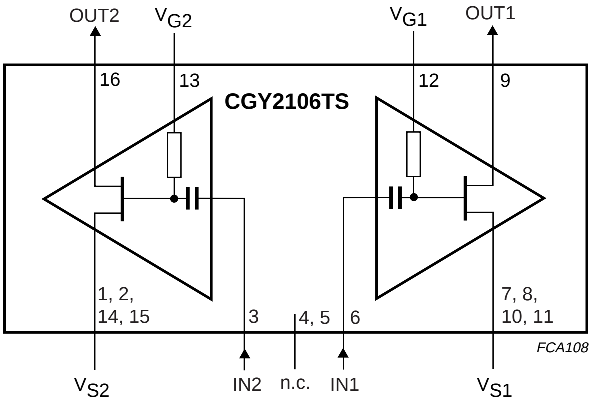


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{S2}	1, 2, 14 and 15	amplifier 2 source
IN2	3	amplifier 2 input
n.c.	4, 5	not connected
IN1	6	amplifier 1 input
V_{S1}	7, 8, 10 and 11	amplifier 1 source
OUT1	9	amplifier 1 drain and output
V_{G1}	12	amplifier 1 gate bias
V_{G2}	13	amplifier 2 gate bias
OUT2	16	amplifier 2 drain and output

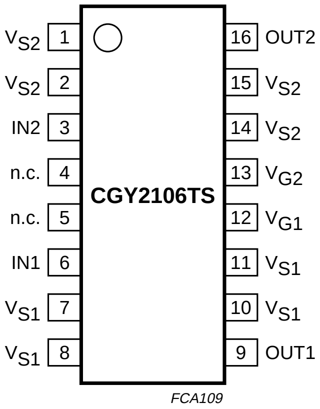


Fig.2 Pin configuration.

LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	voltage difference between OUT1 drain (OUT2 resp.) and V_{S1} source (V_{S2} resp.) pins		–	5	V
V_{GS}	voltage difference between V_{G1} gate (V_{G2} resp.) and V_{S1} source (V_{S2} resp.) pins		–3	+1	V
V_{GD}	voltage difference between gate V_{G1} (V_{G2} resp.) and OUT1 drain (OUT2 resp.) pins		–	7	V
V_{supply}	positive supply voltage	see Chapter “Test and application information”	–	6	V
V_{neg}	negative supply voltage	see Chapter “Test and application information”	–6	–	V
T_{amb}	ambient temperature		–40	+85	°C
T_{ch}	operating channel temperature		–	150	°C
T_{stg}	storage temperature		–	150	°C
P_{tot}	total power dissipation	T_{amb} < 85 °C	–	430	mW

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	150	K/W

DC CHARACTERISTICS FROM JUNCTION TO AMBIENT

T_{amb} = 25 °C; unless otherwise specified. Parameters are guaranteed when using external components and application board shown in Chapter “Test and application information”.

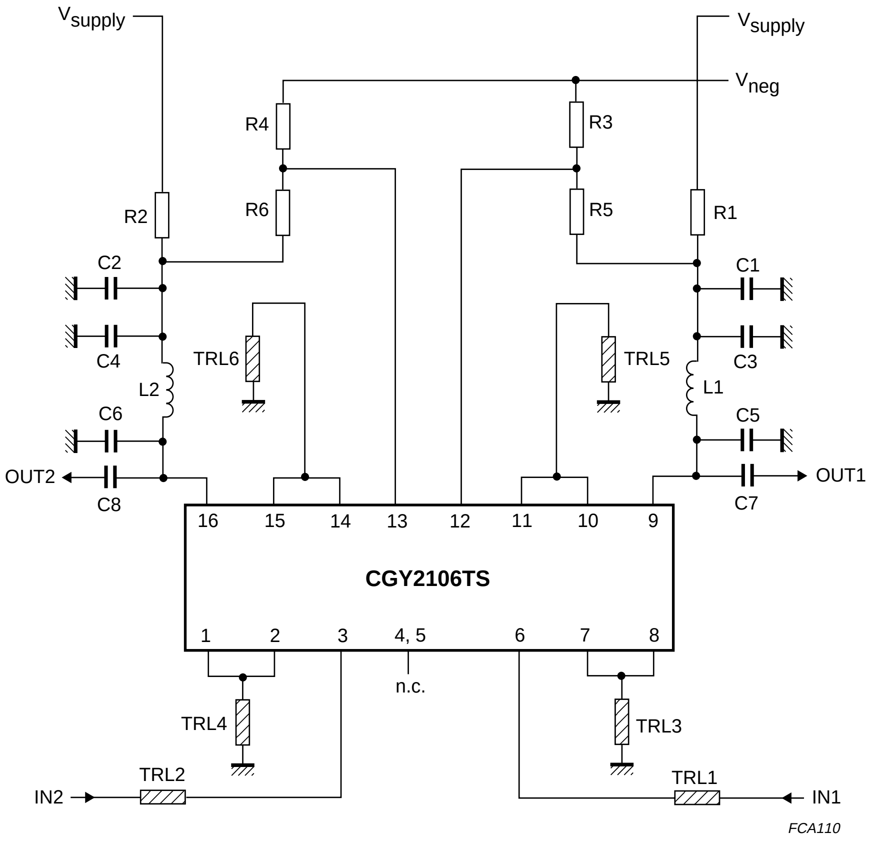
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{supply}	positive supply voltage currents (for each LNA)	V_{supply} = 5.0 V; V_{neg} = –5.0 V	64	78	86	mA
I_{neg}	negative supply voltage currents (for each LNA)	V_{supply} = 5.0 V; V_{neg} = –5.0 V	–	0.8	1.1	mA

AC CHARACTERISTICS

V_{supply} = 5.0 V; V_{neg} = –5.0 V; both LNAs biased and Z_o = 50 Ω; duty cycle 100%; T_{amb} = 25 °C. Parameters are guaranteed when using external components and application board shown in chapter “Test and application information”; unless otherwise specified.

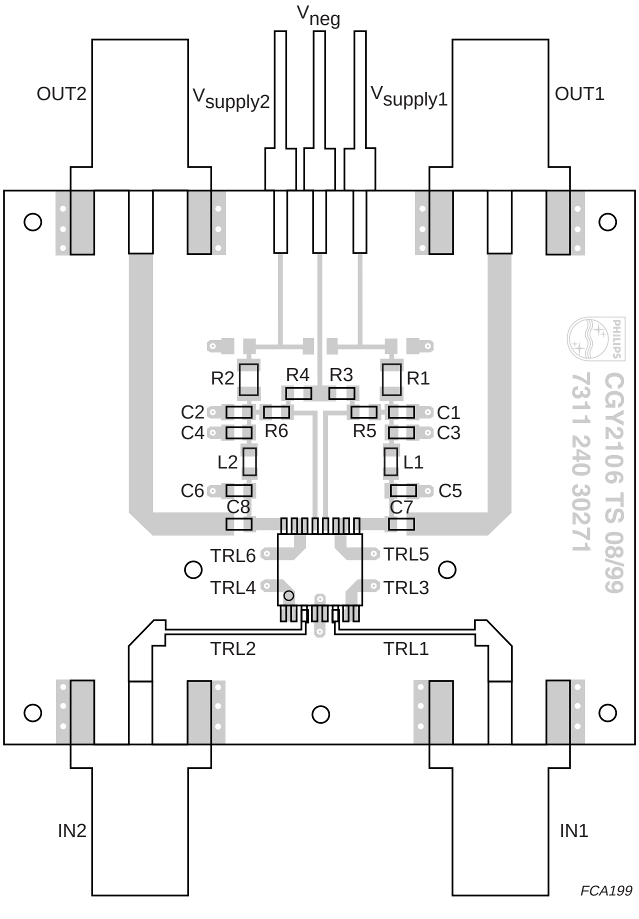
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency		800	–	920	MHz
G	small signal gain		14.6	16.1	17.6	dB
G_{800}	small signal gain at f = 800 MHz		15.8	16.7	17.6	dB
ISO_r	reverse isolation		18	20	–	dB
$ISO_{i\text{-}i}$	isolation between inputs		25	28	–	dB
NF	noise figure		–	0.5	0.7	dB
$IP3_i$	input third order intercept point	Δf = ±0.5 MHz	11.5	14	–	dBm
S_{11}	input reflection coefficient	50 Ω source	–	–8.5	–	dB
S_{22}	output reflection coefficient	50 Ω load	–	–20	–	dB
$\Delta S_{21(T)}$	small signal gain variation with temperature	–40 °C T_{amb} < +85 °C	–	±0.5	–	dB
$\Delta NF_{(T)}$	noise figure variation with temperature	–40 °C < T_{amb} +85 °C	–	±0.20	–	dB
$\Delta IP3_{i(T)}$	input third order intercept point variation with temperature	–40 °C < T_{amb} < +85 °C	–	±0.40	–	dB

TEST AND APPLICATION INFORMATION



The demonstration board has been optimized for a centre frequency of 0.9 GHz.
The MMIC s-parameters (typical values) are available in a range from 0.1 to 6 GHz on request.

Fig.3 Application board schematic.



Designed for a frequency of 0.9 GHz.

Fig.4 Application board layout.

Table 1 Components for layout; see Figs 3 and 4.

COMPONENT	VALUE	REFERENCE	FUNCTION
C1; C2	1 nF	Philips; NPO; 0603	decoupling
C3; C4	100 pF	Philips; NPO; 0603	decoupling
C5; C6	2.2 pF	Philips; NPO; 0603	decoupling
C7; C8	100 pF	Philips; NPO; 0603	decoupling
R1; R2	39 Ω	Bourns; 0805	drain biasing resistor
R3; R4	5.6 kΩ	Philips; 0603	gate biasing resistor
R5; R6	3.3 kΩ	Philips; 0603	gate biasing resistor
L1; L2	39 nH	Coilcraft; 0603	drain biasing inductor

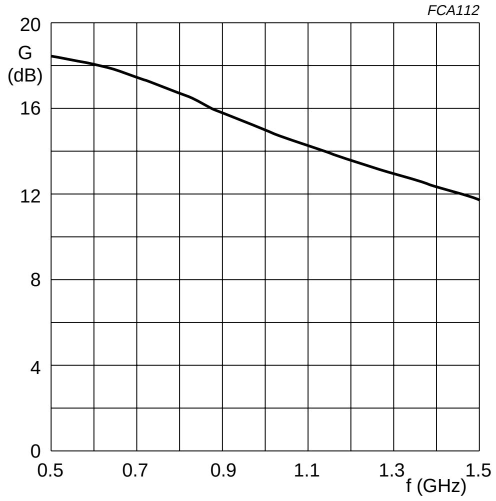
Table 2 Transmission lines for layout; see Figs 3 and 4.

COMPONENT	Z_O	LENGTH	LENGTH(1)	WIDTH(1)
TRL1; TRL2	100 Ω	0.040λ at 900 MHz	10 mm	0.25 mm
TRL3; TRL4	70 Ω	0.033λ at 900 MHz	5 mm	0.80 mm
TRL5; TRL6	70 Ω	0.035λ at 900 MHz	4.4 mm	0.80 mm

Note

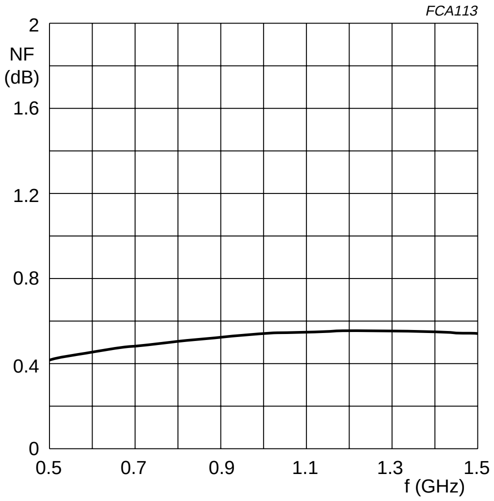
1. Transmission line lengths and widths in mm are valid for a double sided PCB; thickness 0.8 mm in FR4 material ($\varepsilon = 4.7$).

Measured performance of the demonstration board (designed for a centre frequency of 0.9 GHz).



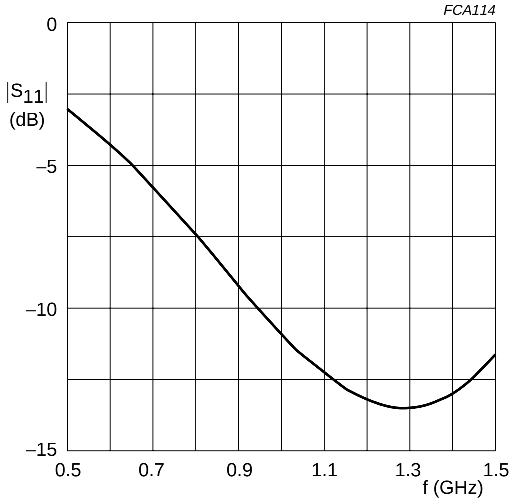
V_{supply} = 5 V; V_{neg} = –5 V.

Fig.5 Gain as a function of frequency.



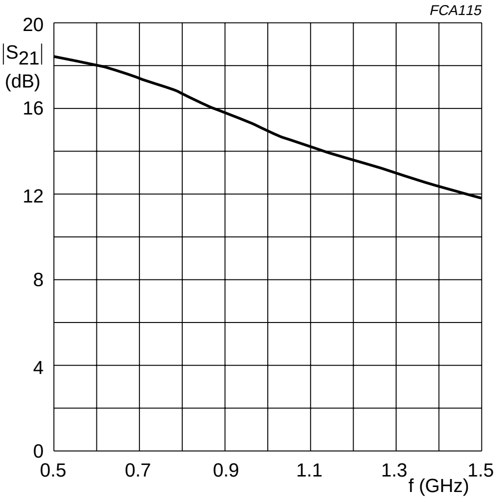
V_{supply} = 5 V; V_{neg} = –5 V.

Fig.6 Noise figure as a function of frequency.



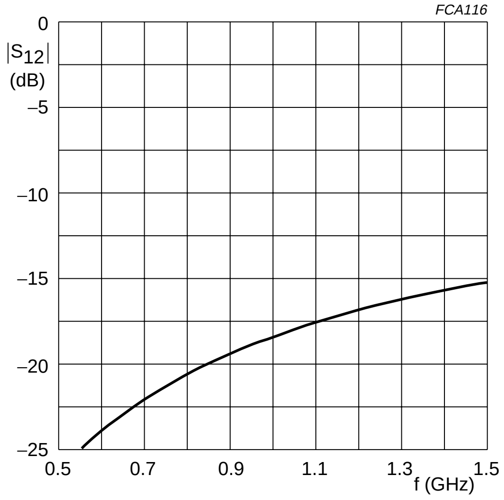
V_{supply} = 5 V; V_{neg} = –5 V.

Fig.7 S_{11} as a function of frequency.



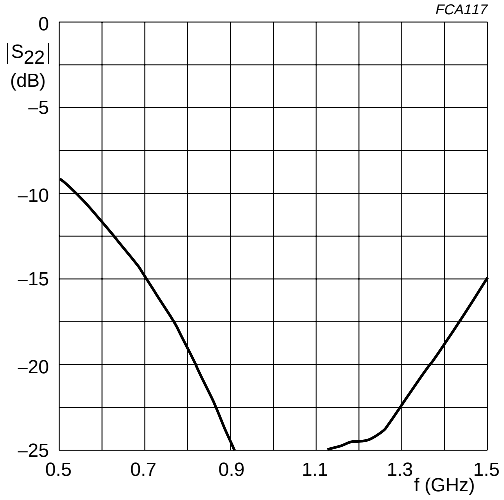
V_{supply} = 5 V; V_{neg} = –5 V.

Fig.8 S_{21} as a function of frequency.



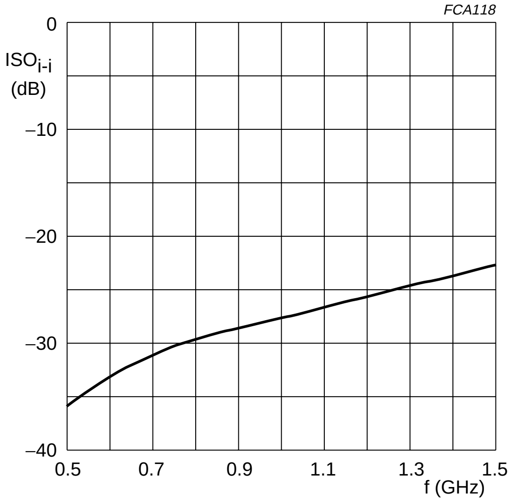
V_{supply} = 5 V; V_{neg} = −5 V.

Fig.9 S_{12} as a function of frequency.



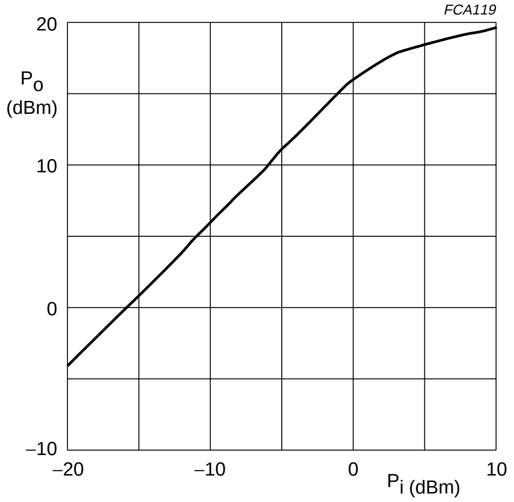
V_{supply} = 5 V; V_{neg} = −5 V.

Fig.10 S_{22} as a function of frequency.



V_{supply} = 5 V; V_{neg} = −5 V.

Fig.11 Isolation between RF inputs as a function of frequency.

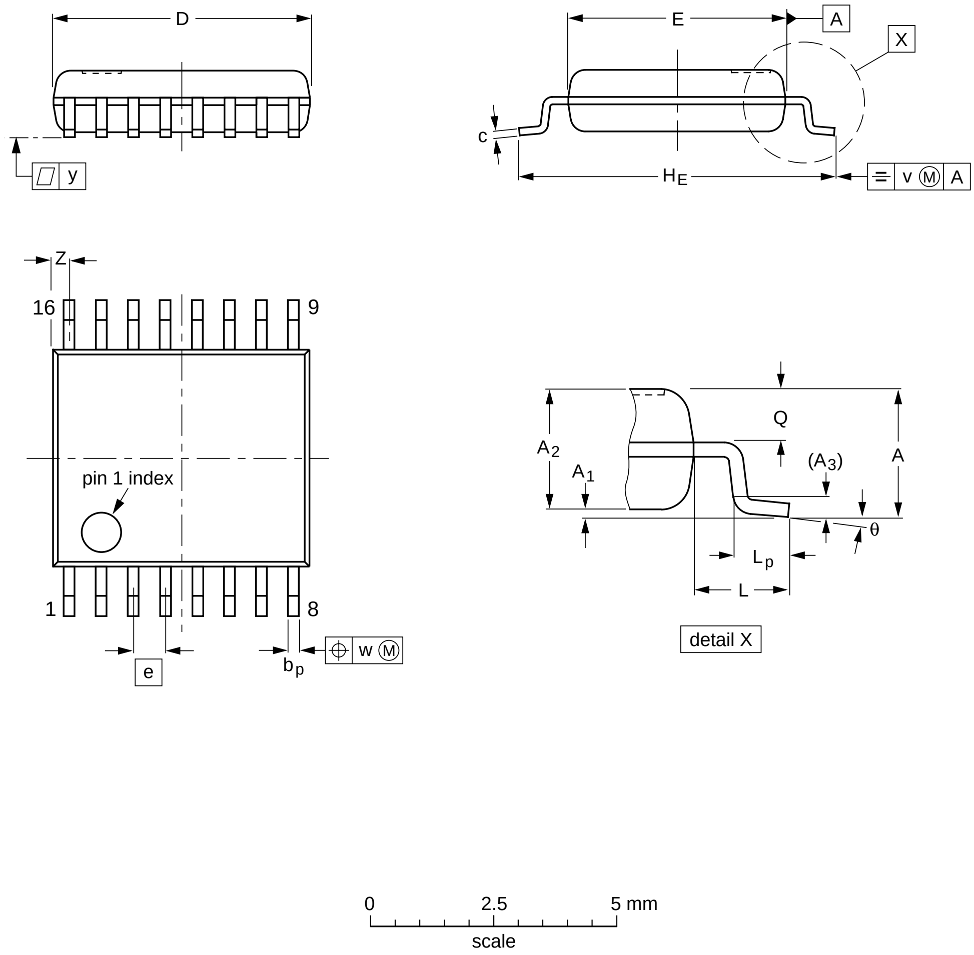


V_{supply} = 5 V; V_{neg} = −5 V.

Fig.12 RF output power as a function of RF input power.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm SOT369-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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