SONY

CXP83408/83412/83416
CXP83409/83413/83417

CMOS 8-bit Single Chip Microcomputer

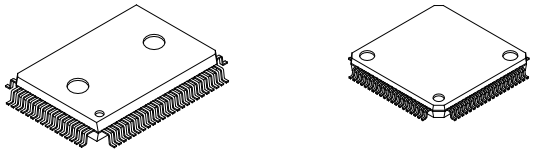
Description

The CXP83408/83412/83416 and CXP83409/83413/83417 are a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, 32kHz timer/counter, LCD controller/driver, remote control receiving circuit and PWM output, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP83408/83412/83416 and CXP83409/83413/83417 sleep/ stop function which enables to lower power consumption.

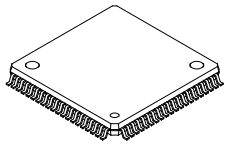
CXP83408/83412/83416

80 pin QFP (Plastic) 80 pin LQFP (Plastic)



CXP83409/83413/83417

80 pin QFP (Plastic)



Features

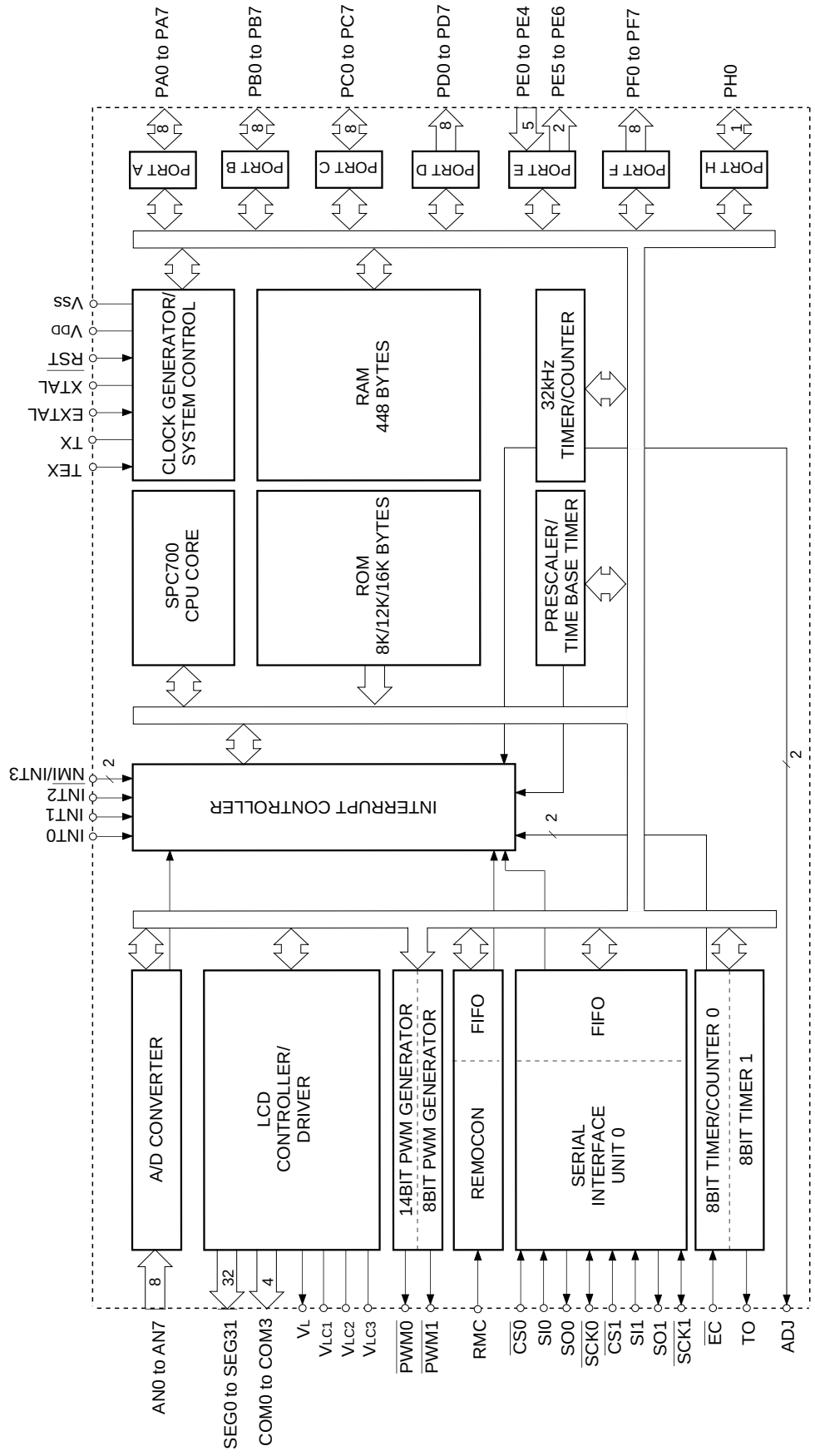
- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit arithmetic/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle: 400ns at 10MHz operation (4.5 to 5.5V)
  122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity: 8K bytes (CXP83408, 83409)
  12K bytes (CXP83412, 83413)
  16K bytes (CXP83416, 83417)
- Incorporated RAM capacity: 448 bytes (LCD display data area included)
- Peripheral functions
  - A/D converter: 8 bits, 8 channels, successive approximation system
    (Conversion time: 32µs/10MHz)
  - Serial interface: Incorporated 8-bit and 8-stage FIFO
    (1 to 8 bytes auto transfer), 1 circuit 2 channels
  - Timer: 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - LCD controller/driver: Maximum 128 segments display possible (During 1/4 duty)
    4 common outputs, 32 segment outputs
    Display method: Static, 1/2, 1/3 and 1/4 duty
    Bias method: 1/2 and 1/3 bias
  - Remote control receiving circuit: 8-bit pulse measurement counter, 6-stage FIFO
  - PWM output: 14 bits 1 channel, 8 bits 1 channel
- Interruption: 12 factors, 12 vectors, multi-interruption possible
- Standby mode: SLEEP/STOP
- Package: 80-pin plastic QFP/LQFP
- Piggyback/evaluator: CXP83400 (CXP83408, 83412, 83416)
  CXP83401 (CXP83409, 83413, 83417)

Structure

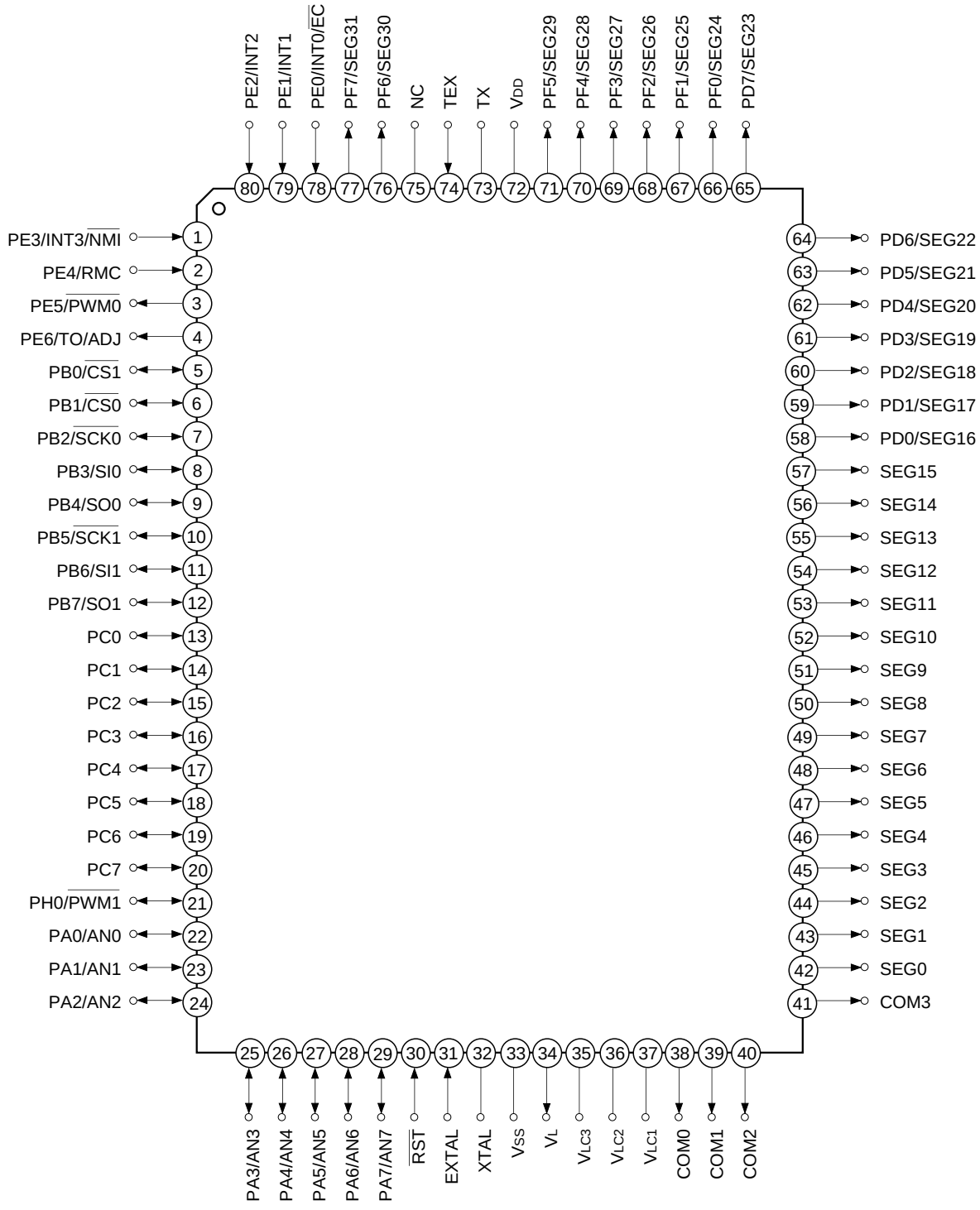
Silicon gate CMOS IC

E93Z15C72-PS

Block Diagram

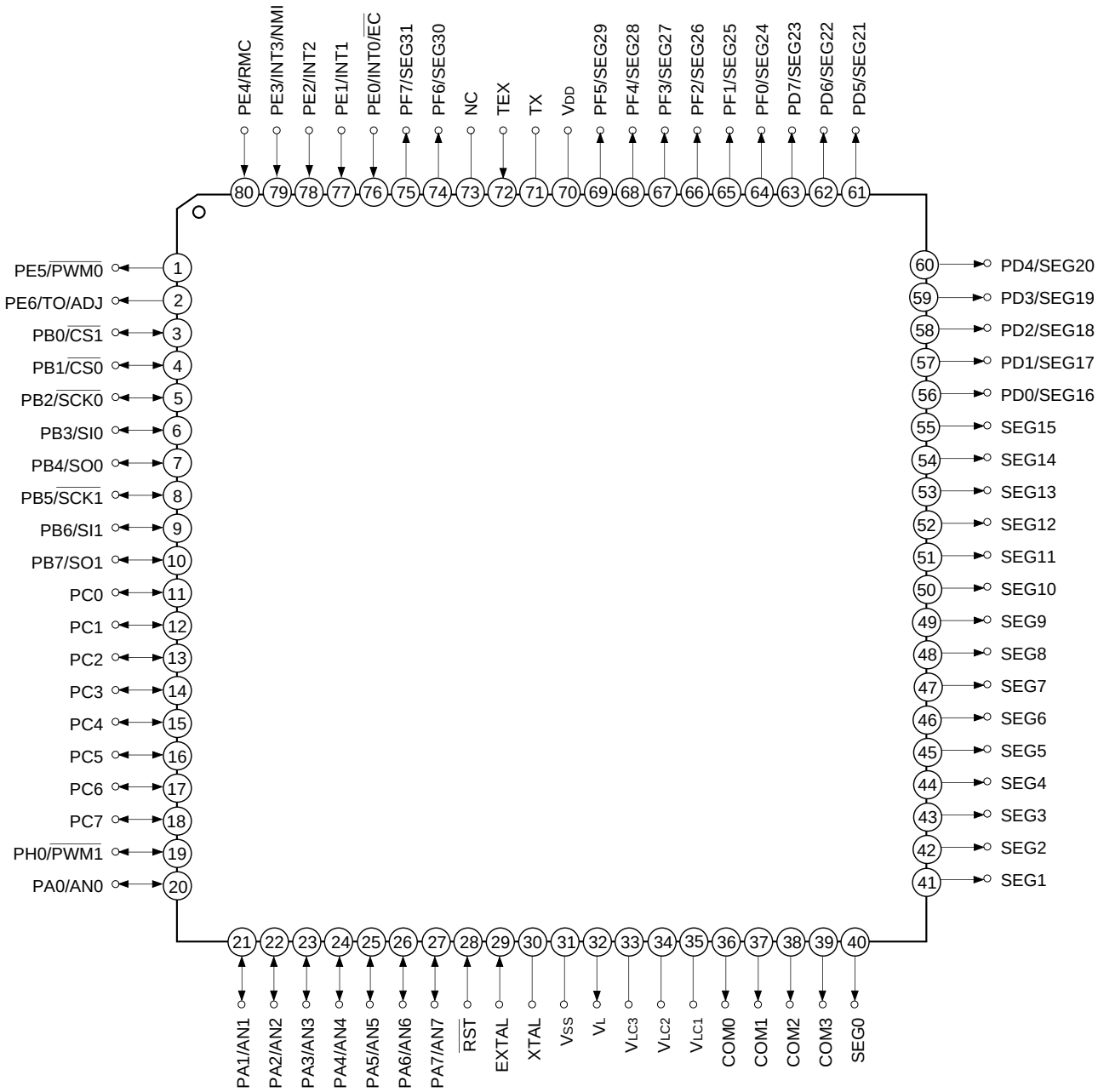


Pin Assignment (Top View) CXP83408/83412/83416 (QFP package)



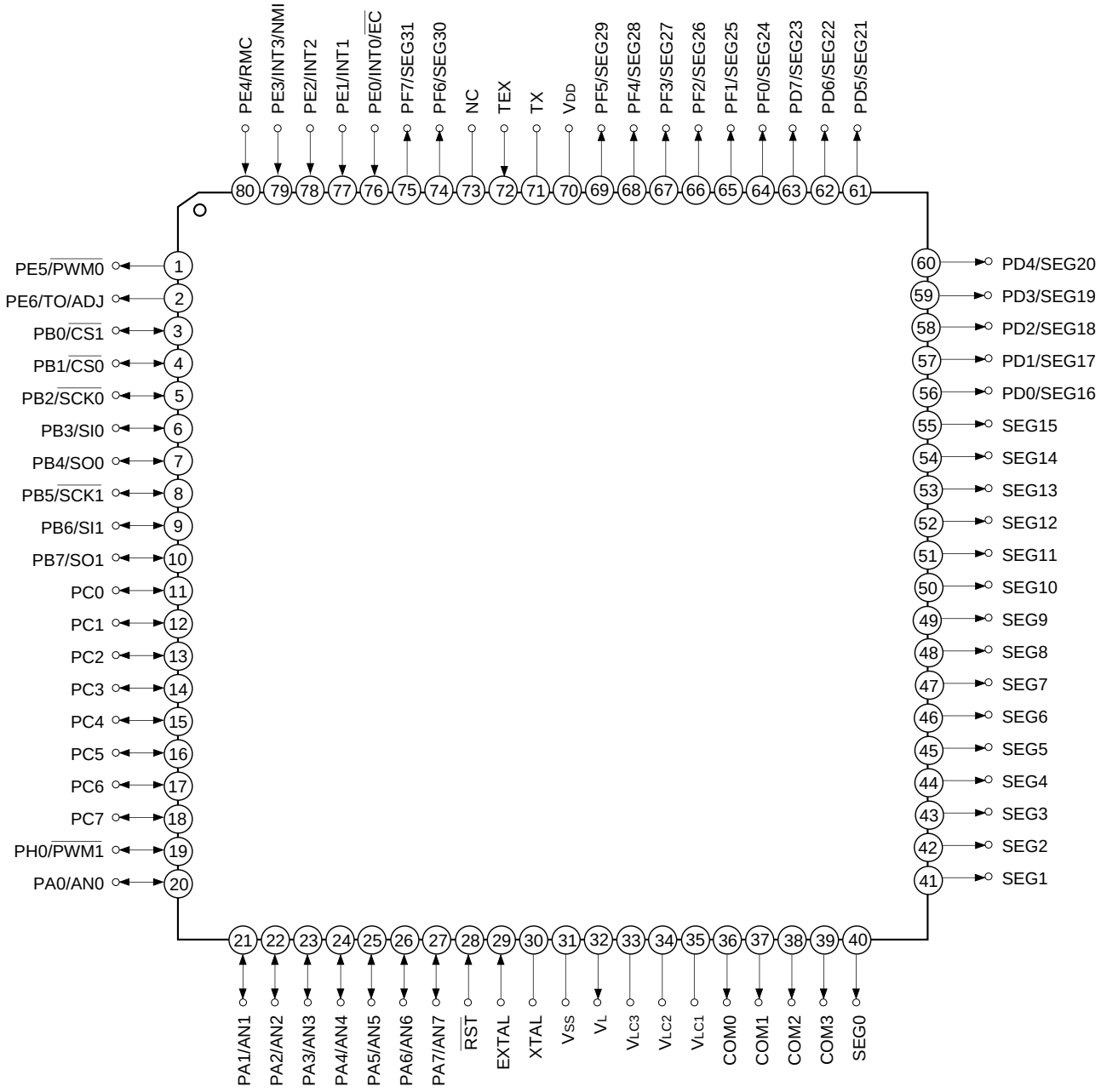
Note) NC (Pin 75) is always connected to V_{DD}.

Pin Assignment (Top View) CXP83408/83412/83416 (LQFP package)



Note) NC (Pin 73) is always connected to V_{DD}.

Pin Assignment (Top View) CXP83409/83413/83417 (QFP package)



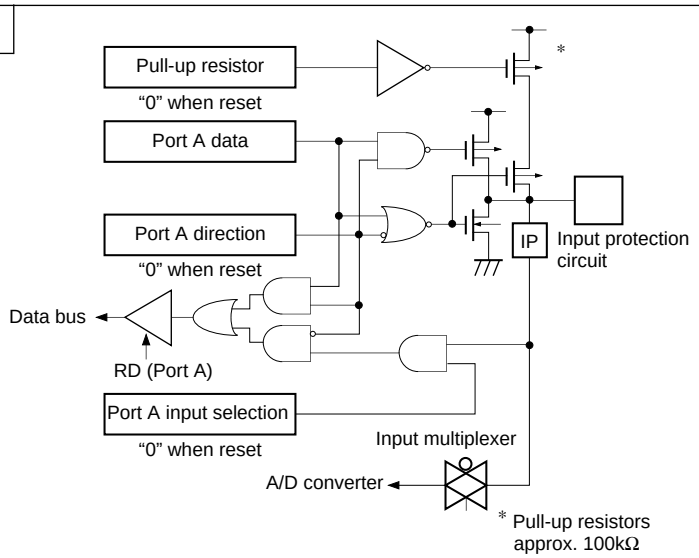
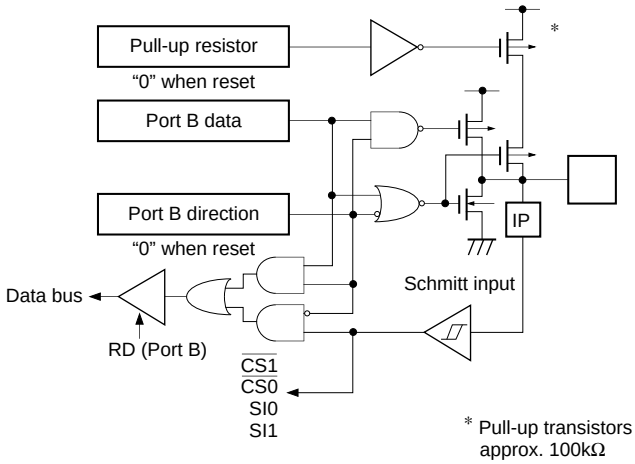
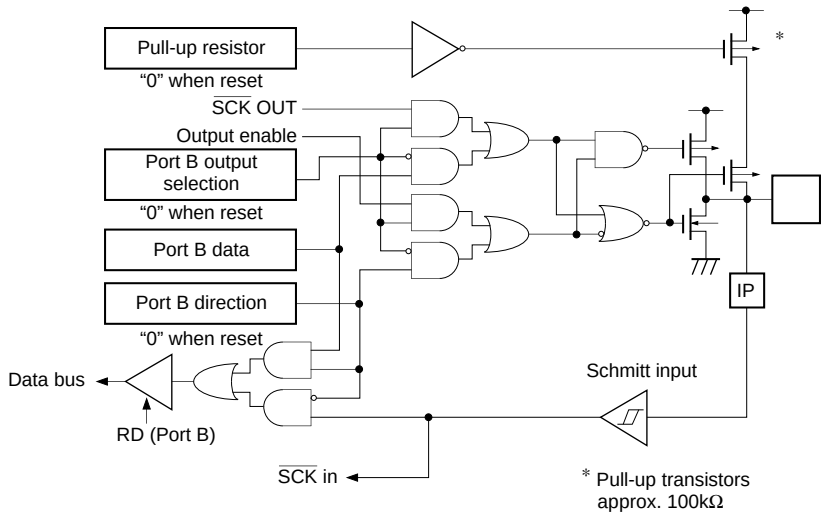
Note) NC (Pin 73) is always connected to V_{DD}.

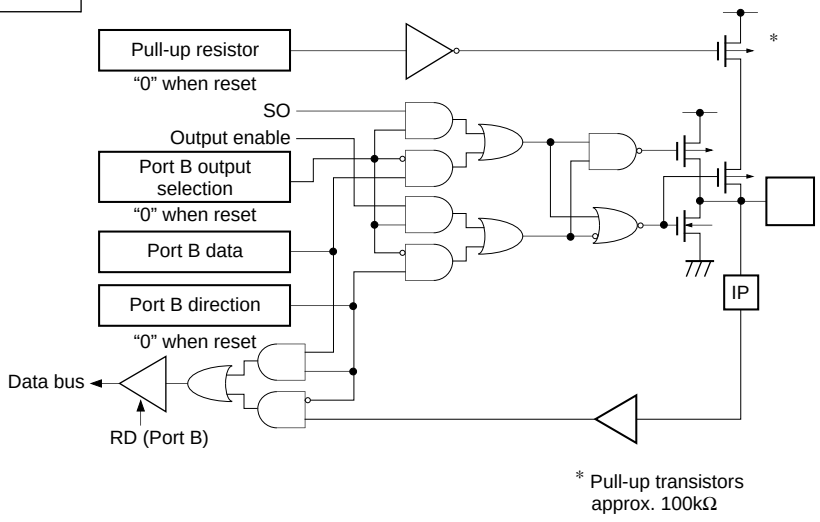
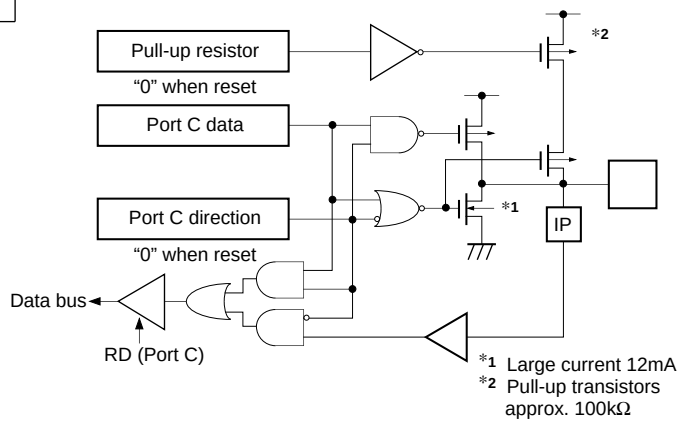
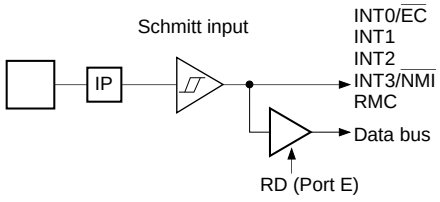
Pin Description

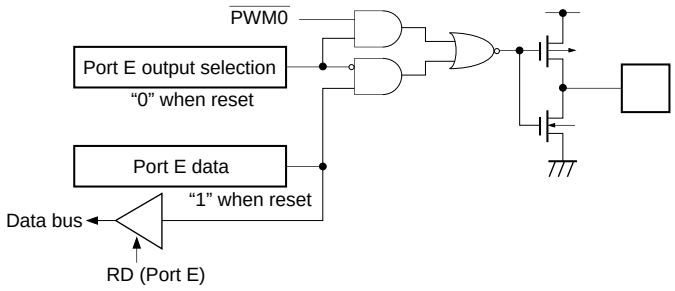
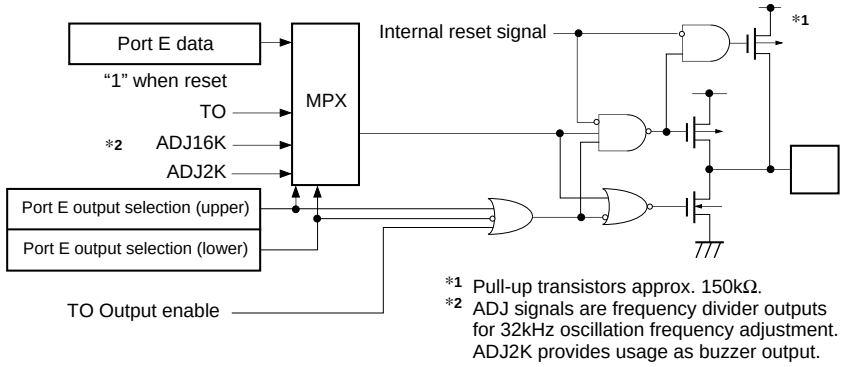
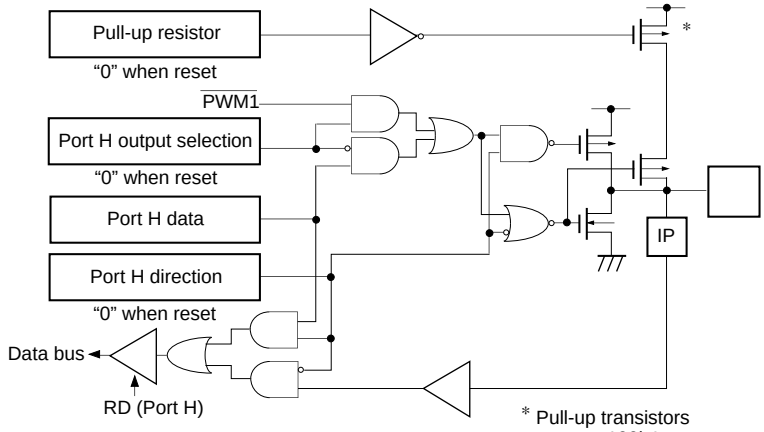
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/$\overline{CS1}$	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/INT0/$\overline{EC}$	Input/Input/Input	(Port E) 7-bit port. Lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External event inputs for timer/counter.
PE1/INT1	Input/Input		External interruption request input. (4 pins)
PE2/INT2	Input/Input		
PE3/INT3/$\overline{NMI}$	Input/Input/Input		Non-maskable intrruption request input.
PE4/RMC	Input/Input		Remote control receiving circuit input.
PE5/$\overline{PWM0}$	Output/Output		14-bit PWM output.
PE6/TO/ADJ	Output/Output/ Output		Rectangular wave output for 8-bit timer/ counter and 32kHz oscillation frequency divider output.
PH0/$\overline{PWM1}$	I/O/Output	(Port H) 1-bit I/O port. Incorporation of pull-up resistor can be set through the software. (1 pin)	8-bit PWM output.

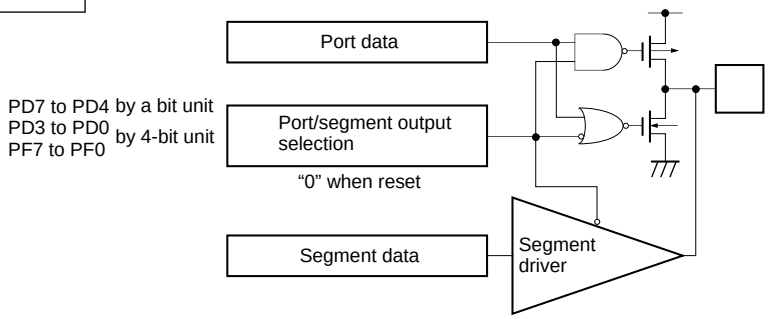
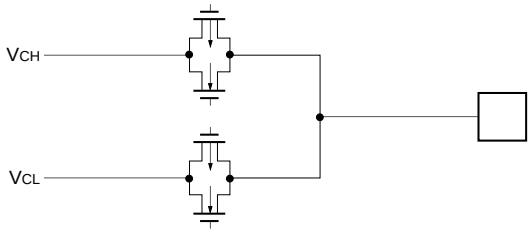
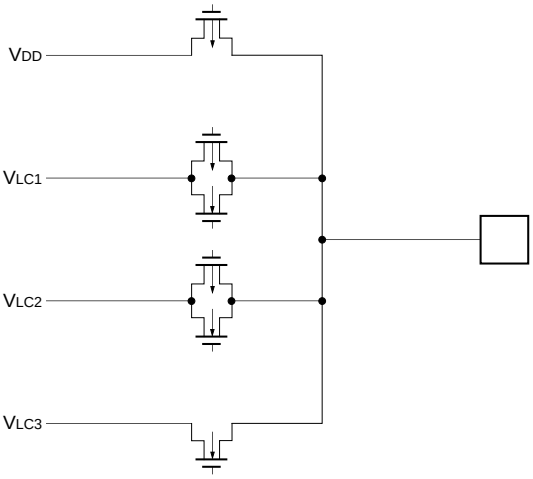
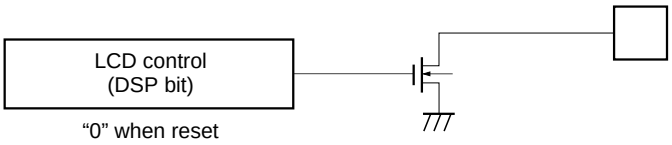
Symbol	I/O	Functions	
PD0/SEG16 to PD7/SEG23	Output/Output	(Port D) 8-bit output port. (8 pins)	LCD segment signal output. (16 pins)
PF0/SEG24 to PF7/SEG31	Output/Output	(Port F) 8-bit output port. (8 pins)	
SEG0 to SEG15	Output	LCD segment signal output.	
COM0 to COM3	Output	LCD common signal output.	
V_{LC1} to V_{LC3}		LCD bias power supply.	
V_L	Output	Control pin to cutt off the current flowing to external LCD bias resistor during standby.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. For usage as event counter, connect clock oscillation source to TEX, and leave TX open.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V_{DD}.	
V_{DD}		Positive power supply.	
Vss		GND.	

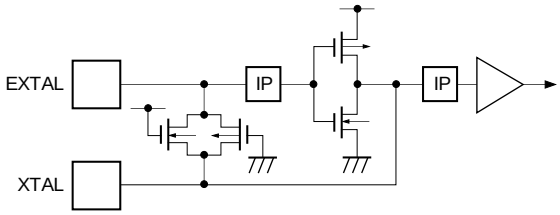
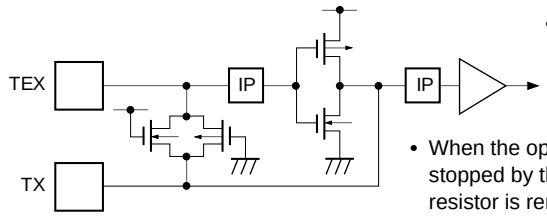
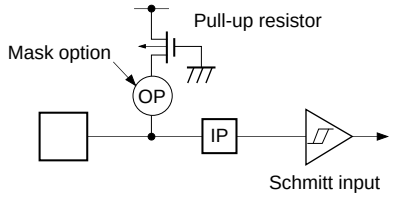
I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/$\overline{CS1}$ PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	Port B 	Hi-Z
PC0 to PC7 8 pins	Port C 	Hi-Z
PE0/INT0/$\overline{EC}$ PE1/INT1 PE2/INT2 PE3/INT3/$\overline{NMI}$ PE4/RMC 5 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE5/$\overline{\text{PWM0}}$ 1 pin	Port E 	High level
PE6/TO/ADJ 1 pin	Port E  *1 Pull-up transistors approx. 150kΩ. *2 ADJ signals are frequency divider outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.	High level (with pull-up transistor ON resistor when reset)
PH0/$\overline{\text{PWM1}}$ 1 pin	Port H  * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PD0 to PD7 PF0 to PF7 24 pins	Port D Port F 	Segment output (V_{DD} level)
SEG0 to SEG15 16 pins	Segment 	V_{DD} level
COM0 to COM3 4 pins	Common 	V_{DD} level
V_L 1 pin		Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes “High” level.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed and TEX and TX become “Low” level and “High” level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
LCD bias voltage	V_{LC1}, V_{LC2}, V_{LC3}	–0.3 to +7.0*1	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	All pins excluding large current output (value per pin)
	I_{OLC}	20	mA	Large current outputs (value per pin*2)
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP-80P-L01
		380	mW	LQFP-80P-L01
		380	mW	QFP-80P-L03

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	During 1/2 and 1/4 frequency division operating modes guaranteed operation range
		3.5	5.5		During 1/16 frequency division operating mode or sleep mode quaranteed operation range
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
LCD bias voltage	V_{LC1}	Vss	V_{DD}	V	LCD power supply range*4
	V_{LC2}				
	V_{LC3}				
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*1
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL*3
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*1
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input*2
	V_{ILEX}	–0.3	0.4	V	EXTAL*3
Operating temperature	Topr	–20	+75	°C	

*1 Value for each pin of normal input ports (PA, PB4, PB7, PC and PH0).

*2 Value of the following pins: $\overline{RST}$, $\overline{CS0}$, $\overline{CS1}$, SI0, SI1, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}$/INT0, INT1, INT2, $\overline{NMI}$/INT3, and RMC.

*3 Specifies only during external clock input.

*4 Optimal values are determined by LCD used.

Electrical Characteristics

DC Characteristics

(Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA, PB, PC, PD*1, PE5, PE6, PF, PH0, V_L (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output current	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	V
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*2		–1.5		–400	mA
	I_{IL}	PA to PC*3, PH*3, PE0 to PE4, $\overline{RST}$*2				–45	µA
	I_{IH}		V_{DD} = 4.5V, V_{IH} = 4.0V	–2.78			µA
I/O leakage current	I_{IZ}		V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Common output impedance	R_{COM}	COM0 to COM3	V_{DD} = 5V, V_{LC1} = 3.75V, V_{LC2} = 2.5V, V_{LC3} = 1.25V		3	5	kΩ
Segment output impedance	R_{SEG}	SEG0 to SEG15, SEG16 to SEG31*1			5	15	kΩ
Supply current*4	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency divider clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		18	40	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		35	100	µA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		1.1	8	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V termination of 10MHz and 32kHz crystal oscillation			10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}	PA to PC, PE1 to PE4, $\overline{EXT}$AL, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24, PF7/SEG31, PD and PF are the case when the common pin is selected as port; SEG16 to SEG31 is when the common pin is selected as segment output.

*2 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*3 PA to PC, and PH0 specify the input current when pull-up resistor has been selected; leakage current when no resistor has been selected. (PE0 to PE4 specify the leakage current.)

*4 When all output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	$t_{sys} + 50$*1			ns
Event count input clock rise and fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise and fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control registor (CLC: 00FE$_H$).

t_{sys} (ns) = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Fig. 1. Clock timing

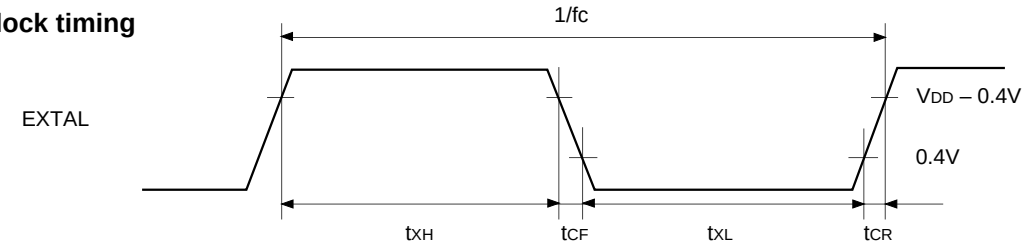


Fig. 2. Clock applied conditions

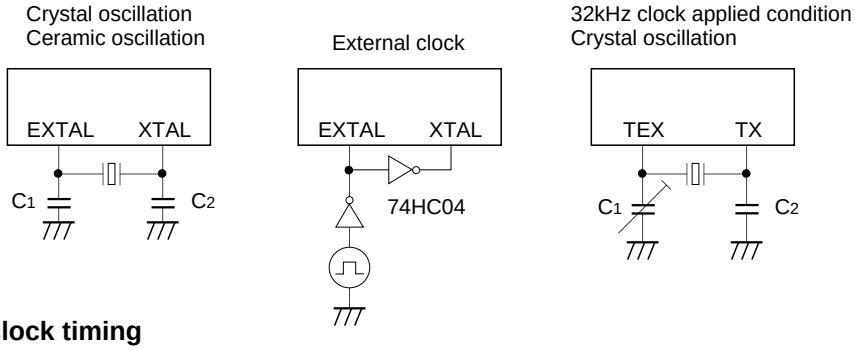
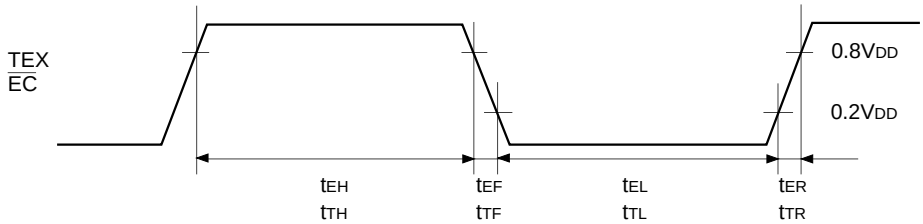


Fig. 3. Event count clock timing



(2) Serial transfer (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

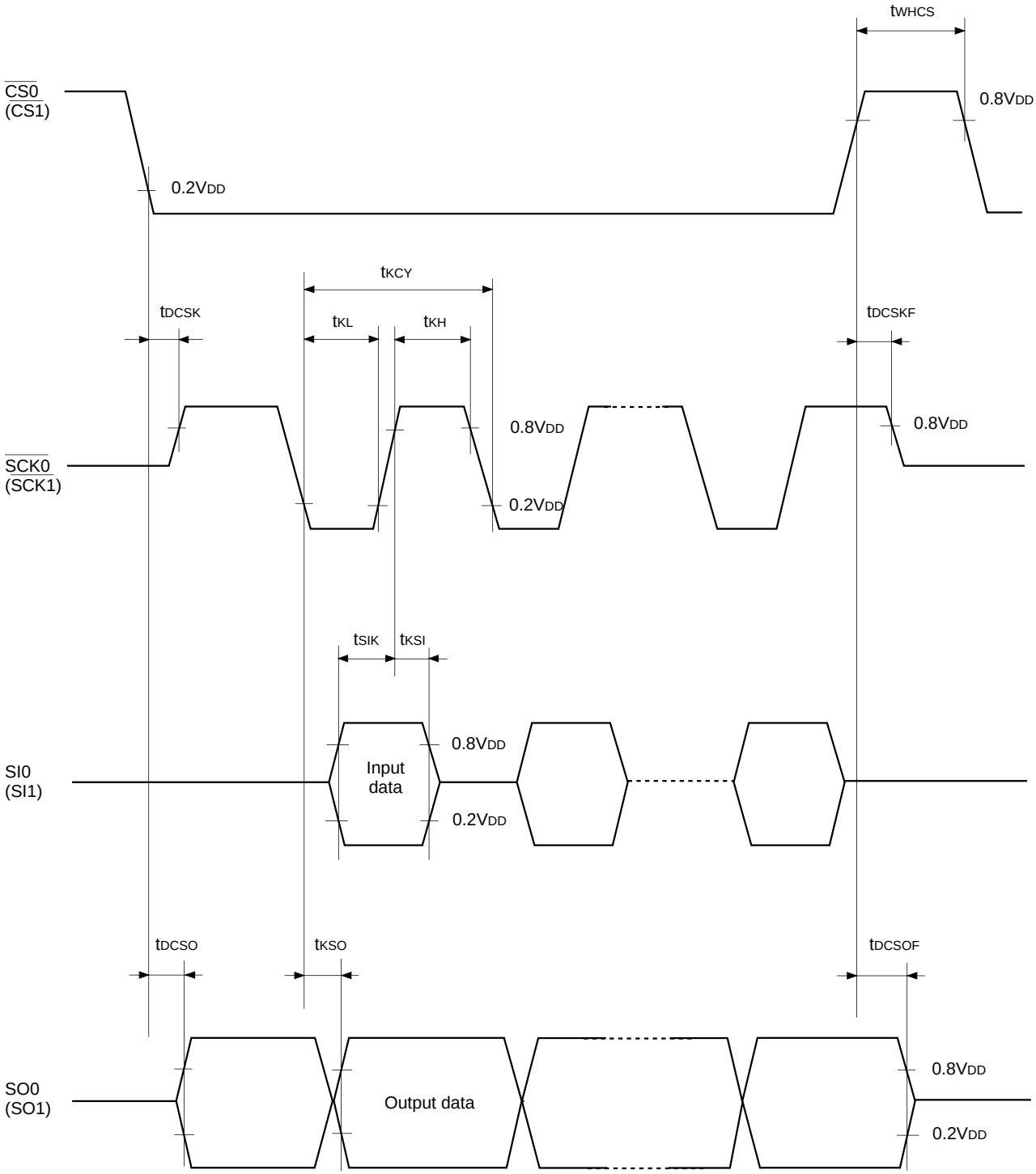
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS0}\downarrow\rightarrow\overline{SCK0}$ ($\overline{CS1}\downarrow\rightarrow\overline{SCK1}$) delay time	t_{DCSK}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow\overline{SCK0}$ ($\overline{CS1}\uparrow\rightarrow\overline{SCK1}$) floating delay time	t_{DCSKF}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow\rightarrow$ SO0 ($\overline{CS1}\downarrow\rightarrow$ SO1) delay time	t_{DCSO}	SO0 (SO1)	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow$ SO0 ($\overline{CS1}\uparrow\rightarrow$ SO1) floating delay time	t_{DCSOF}	SO0 (SO1)	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ ($\overline{CS1}$) high level width	t_{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t_{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ ($\overline{SCK1}$) high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 (SI1) input setup time (for $\overline{SCK0}\uparrow$ ($\overline{SCK1}\uparrow$))	t_{SIK}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
SI0 (SI1) input hold time (for $\overline{SCK0}\uparrow$ ($\overline{SCK1}\uparrow$))	t_{KSI}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	tsys + 200		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 ($\overline{SCK1}\downarrow\rightarrow$ SO1) delay time	t_{KSO}	SO0 (SO1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		tsys + 200	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FE$_H$).

tsys (ns) = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

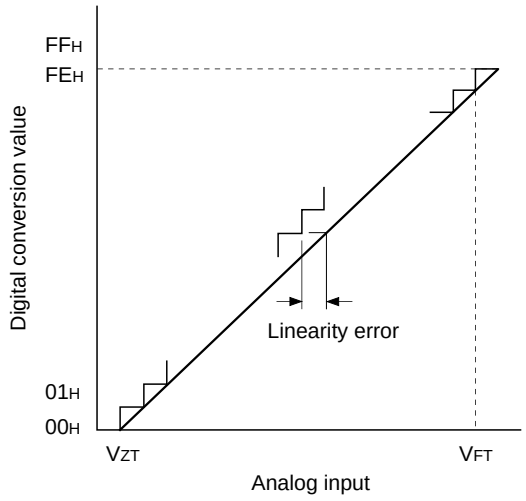


(3) A/D converter characteristics

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V V_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD} + 0.3	V

Fig. 5. Definition of A/D converter terms



*1 V_{ZT}: Value atwhich the digital conversion value changes from 00_H to 01_H and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FE_H to FF_H and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CK3) of the A/D control registor (ADC: $00F9_H$) and bit 7 (PCK1) and bit 6 (PCK0) of the clock control resistor (CLC: $00FE_H$).

CKS / PCK1, PCK0	0 (ϕ/2 selection)	0 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = fc/2	f_{ADC} = fc
01 (ϕ = f_{EX}/4)	f_{ADC} = fc/4	f_{ADC} = fc/2
11 (ϕ = f_{EX}/16)	f_{ADC} = fc/16	f_{ADC} = fc/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 $\overline{\text{NMI}}$/INT3		1		µs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		32/fc		µs

Fig 6. Interruption input timing

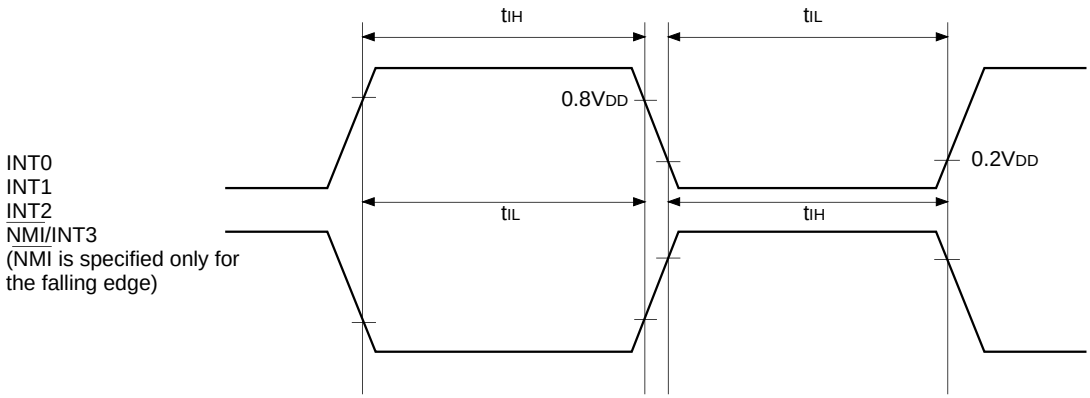
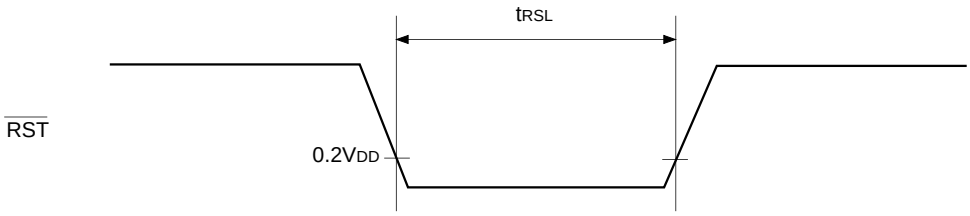


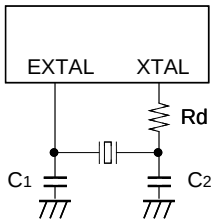
Fig. 7. $\overline{\text{RST}}$ input timing



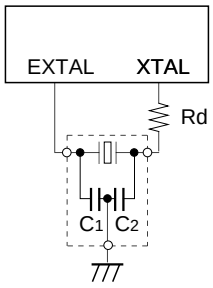
Appendix

Fig. 8. SPC700 Series recommended oscillation circuit

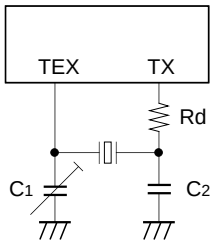
(i) Main clock



(ii) Main clock



(iii) Sub clock



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MG	8.00				
	CSA10.0MT	10.00				
	CST4.19MGW*1	4.19				(ii)
	CST8.00MTW*1	8.00				
	CST10.00MTW*1	10.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	15	15	2.2k	(i)
		8.00				
		10.00			470	
KINSEKI LTD.	HC-49/U (-S)	4.19	22	22	560	
		8.00	18	18	0	
		10.00				

Models with an asterisk (*1) have the built-in ground capacitance (C_1, C_2).

Mask Option Table

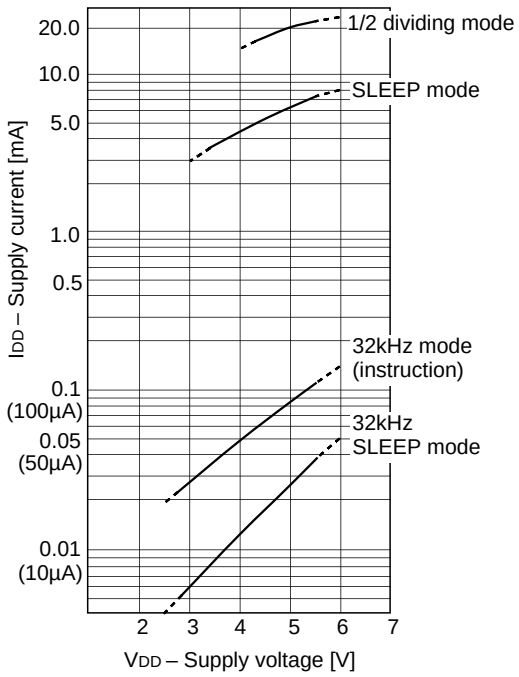
Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Package Table

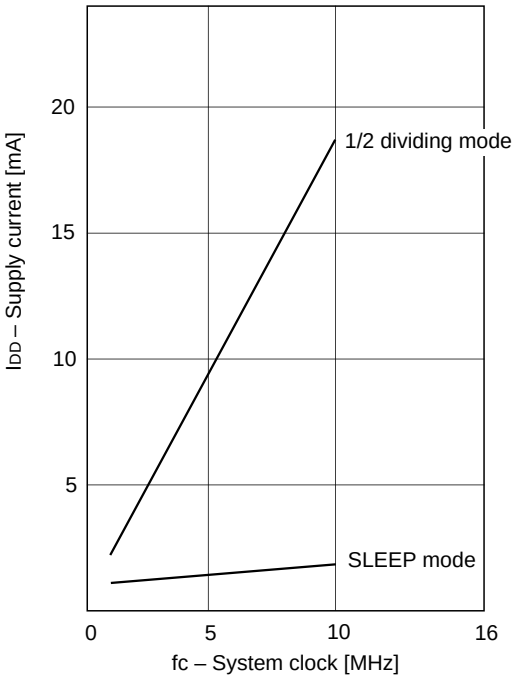
Product name	Package
CXP83408/83412/83416	80-pin plastic QFP/LQFP
CXP83409/83413/83417	80-pin plastic QFP (0.65mm pitch)

Characteristic Curves

IDD vs. VDD
(fc = 10MHz, Ta = 25°C, Typical)



IDD vs. fc
(VDD = 5V, Ta = 25°C, typical)

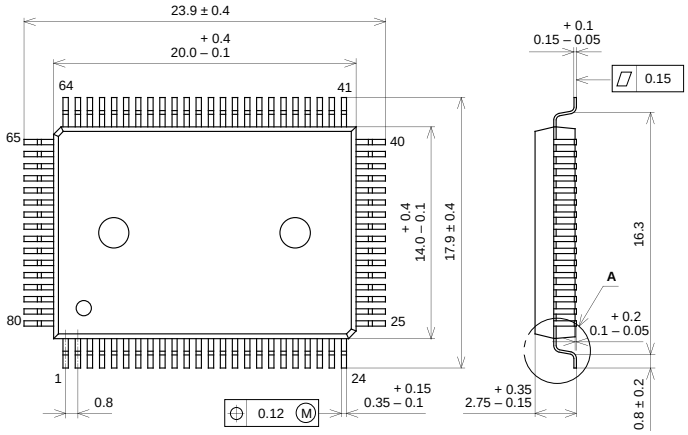


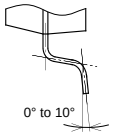
Package Outline

Unit : mm

CXP83408/83412/83416

80PIN QFP (PLASTIC)





DETAIL A

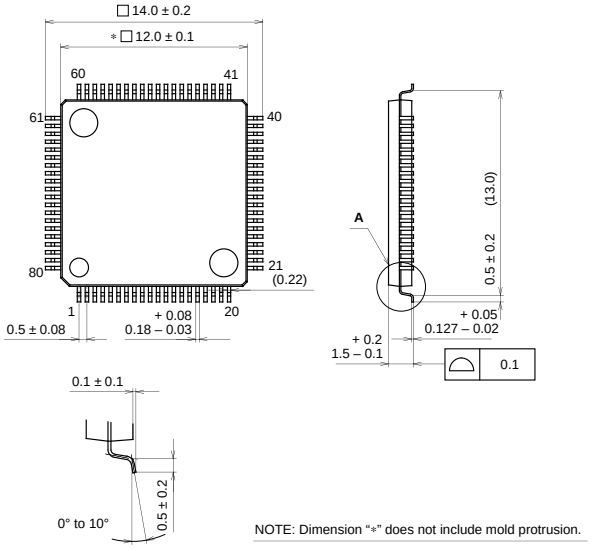
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	

CXP83408/83412/83416

80PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

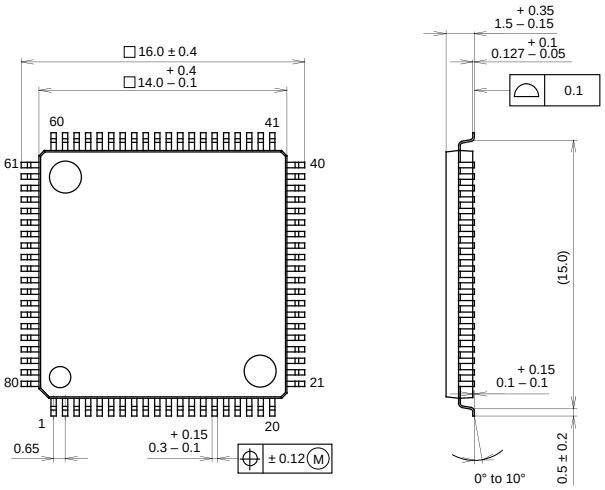
PACKAGE STRUCTURE

SONY CODE	LQFP-80P-L01
EIAJ CODE	∗QFP080-P-1212-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

CXP83409/83413/83417

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.6g