TC551001BPL/BFL/BFTL/BTRL-70L/85L

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

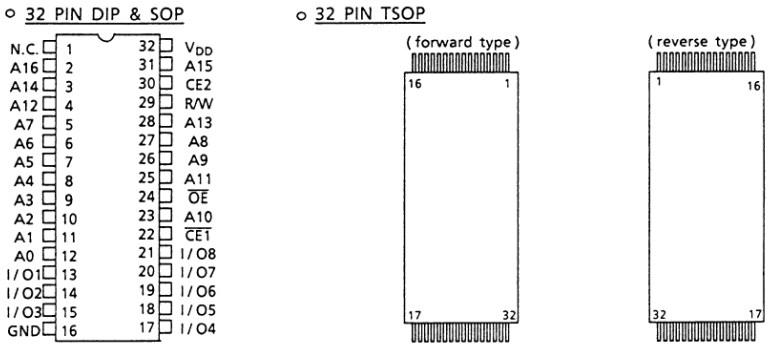
Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL	
	-70L	-85L
Access Time	70ns	85ns
$\overline{CE1}$ Access Time	70ns	85ns
CE2 Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC551001BPL : DIP32-P-600
  TC551001BFL : SOP32-P-525
  TC551001BFTL : TSOP32-P-0820
  TC551001BTRL : TSOP32-P-0820A

Pin Connection (Top View)



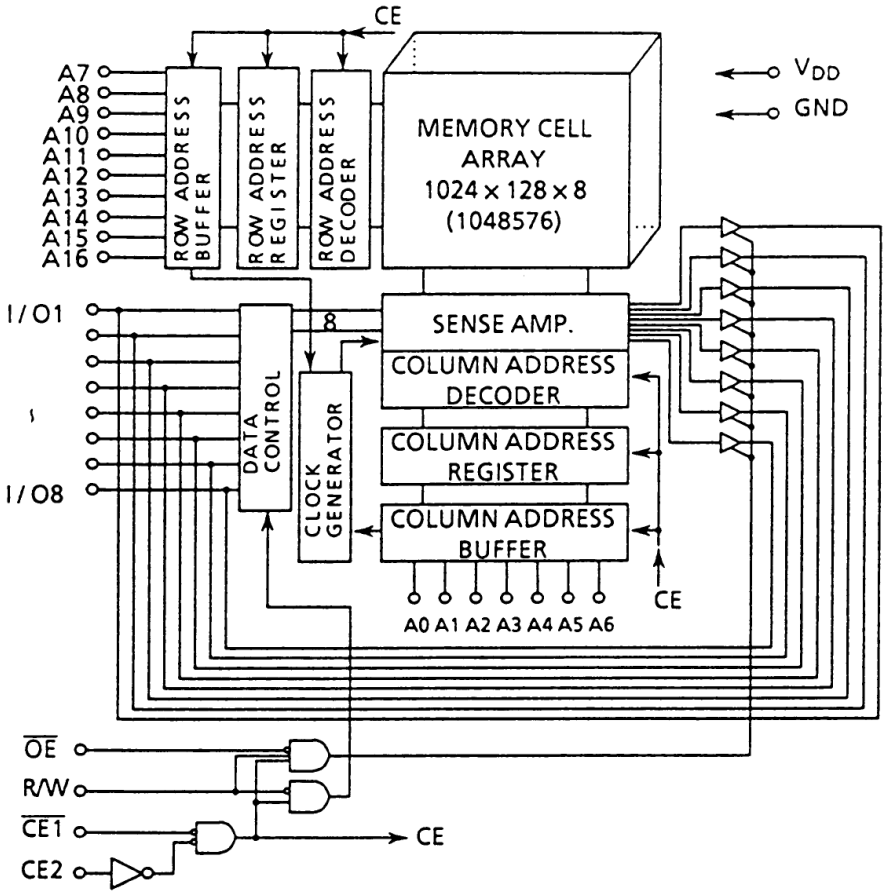
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width of 50ns Max
** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width of 50ns Max.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	70	mA
				1µs	–	–	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2V R/W = V_{DD} - 0.2V I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V/0.2V	t_{cycle}	Min.	–	–	60	
				1µs	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			–	–	3	mA
I_{DDS2}(1)		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C		–	–	30	µA
			Ta = 25°C		–	2	4	

Note: (1) In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, these specification limits are guaranteed under the condition of CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	
t_{CO2}	CE2 Access Time	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

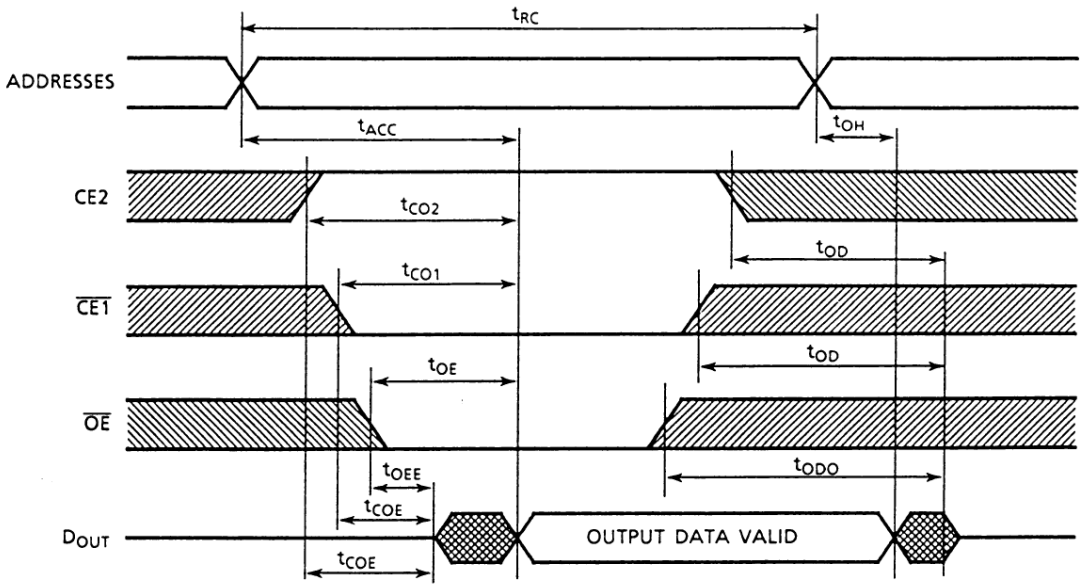
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	75	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

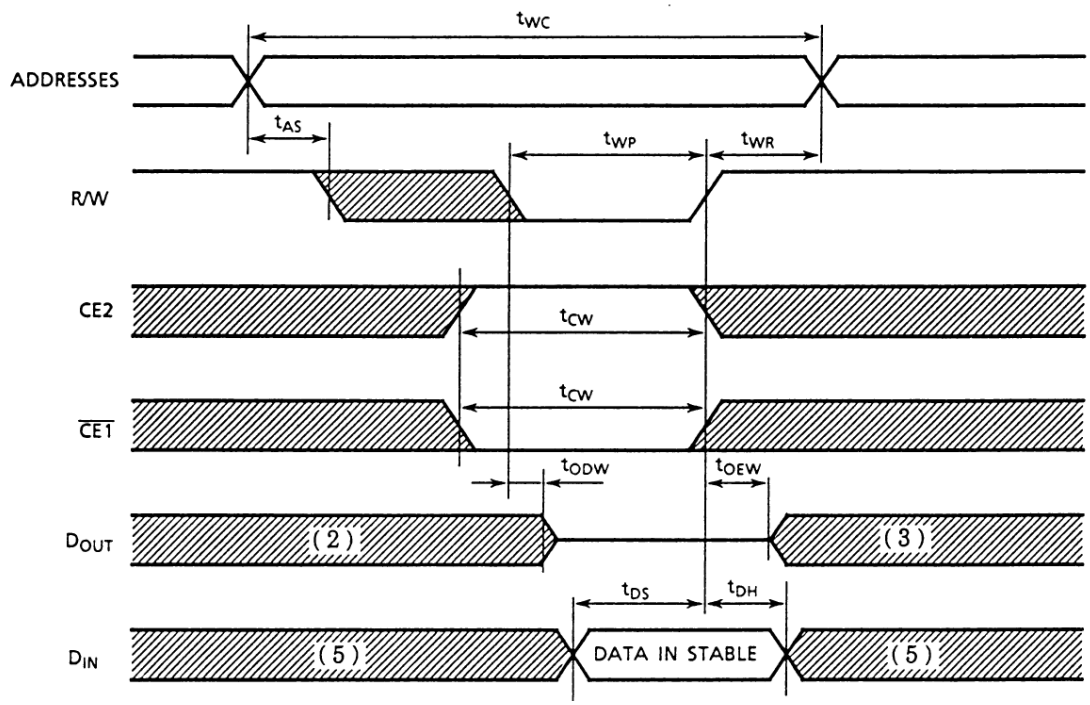
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

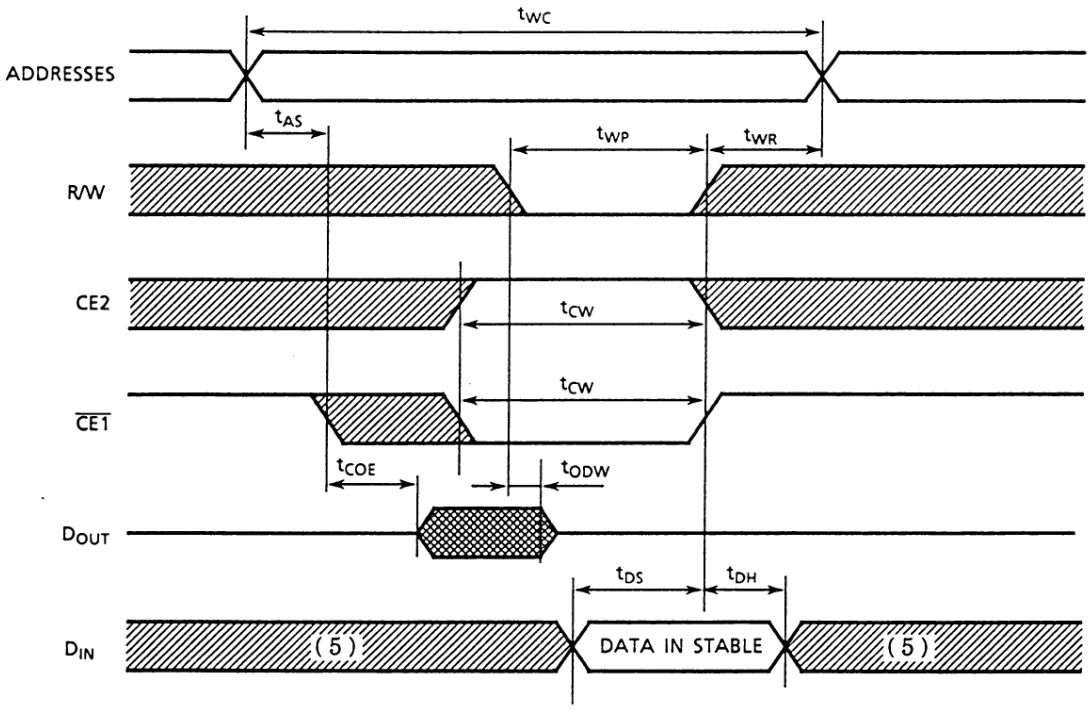
Read Cycle (1)



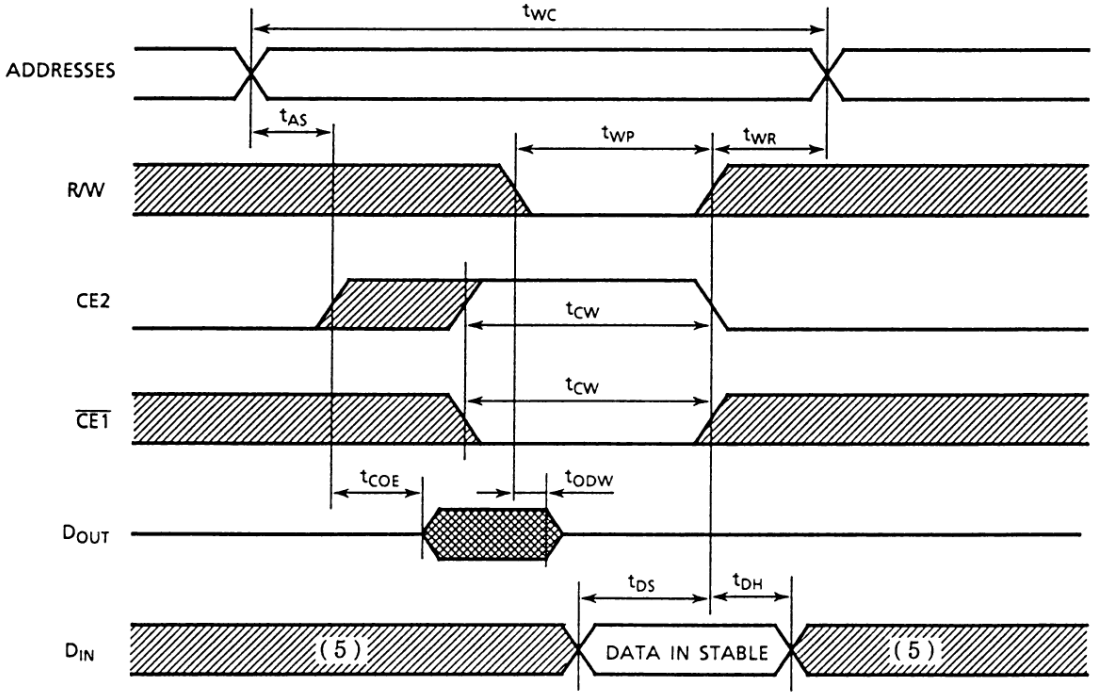
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [4] (CE2 Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W high transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.

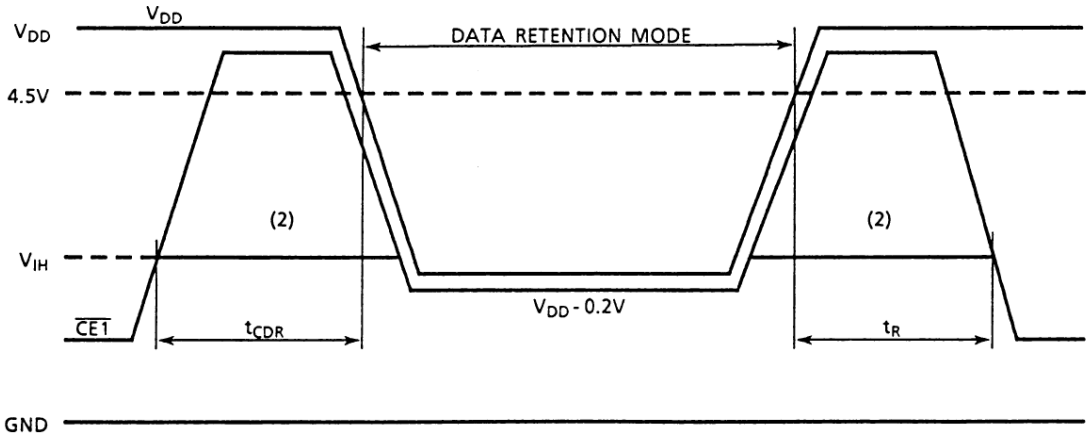
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

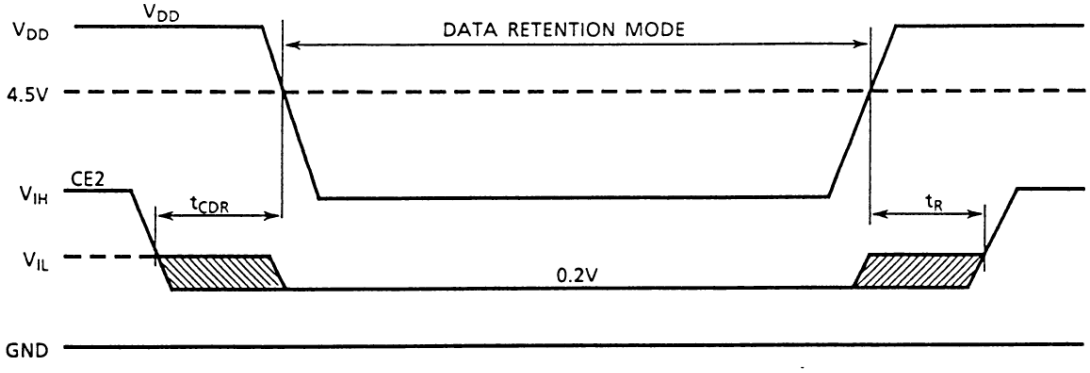
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	15*	µA
		V_{DD} = 5.5V	–	–	30	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*3µA (max.) Ta = 0 ~ 40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

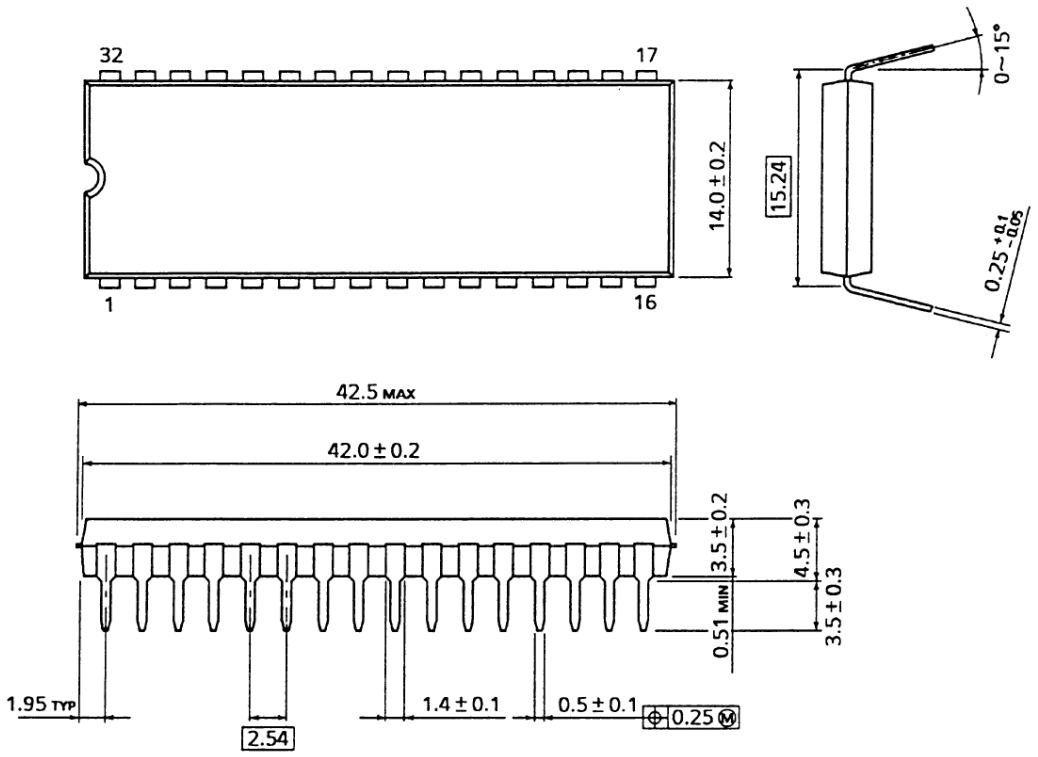
1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

2. If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V.

Outline Drawing

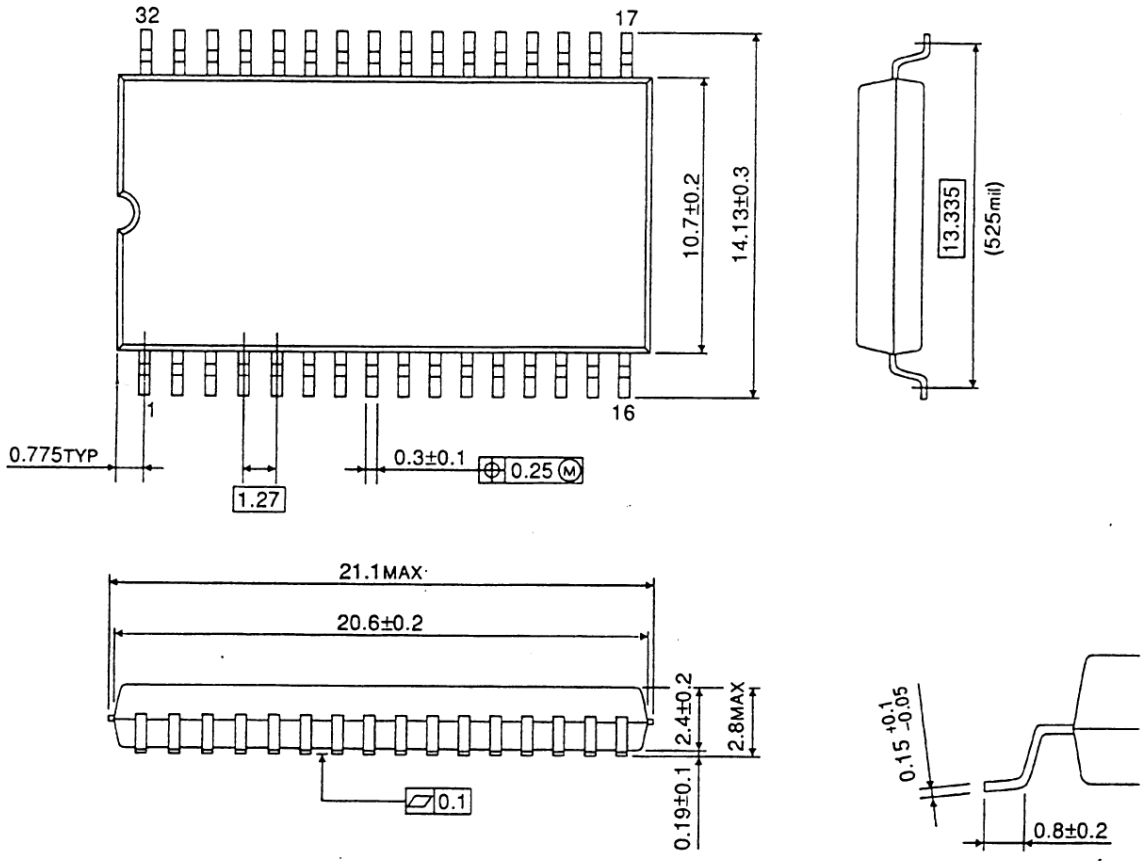
DIP32-P-600 Unit in mm



Weight : 4.45 g (Typ.)

Outline Drawing

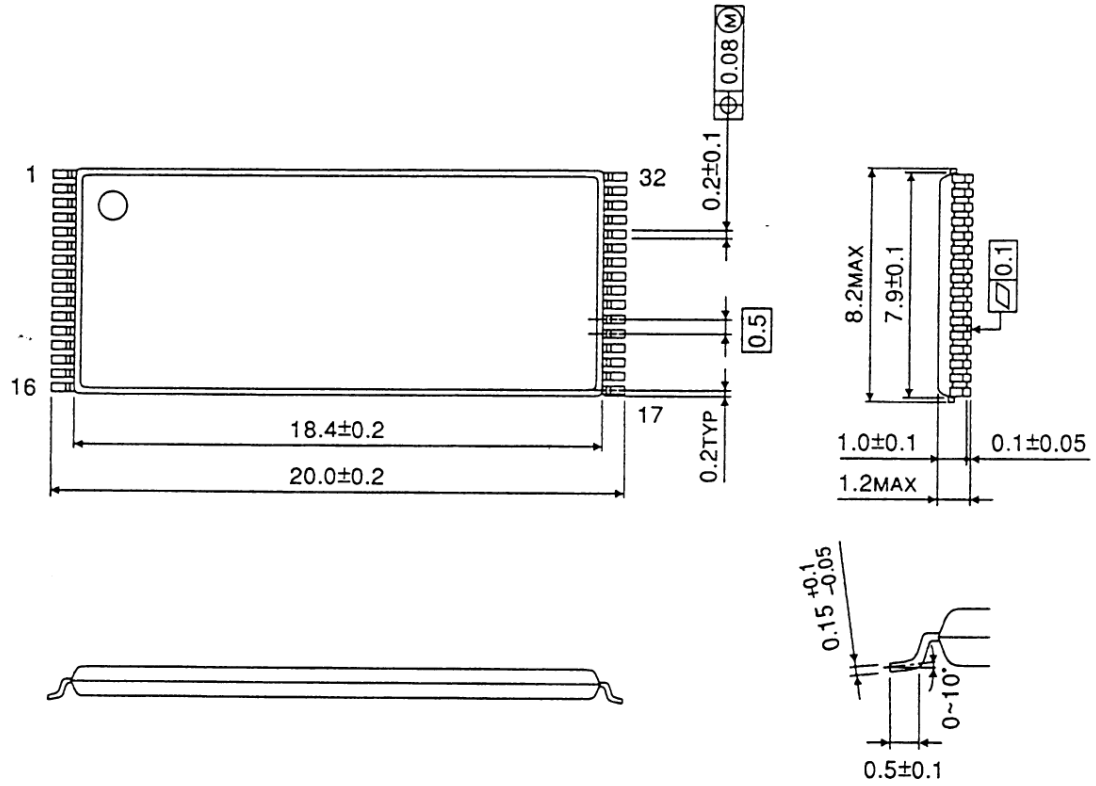
SOP32-P-525 Unit in mm



Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820 Unit in mm

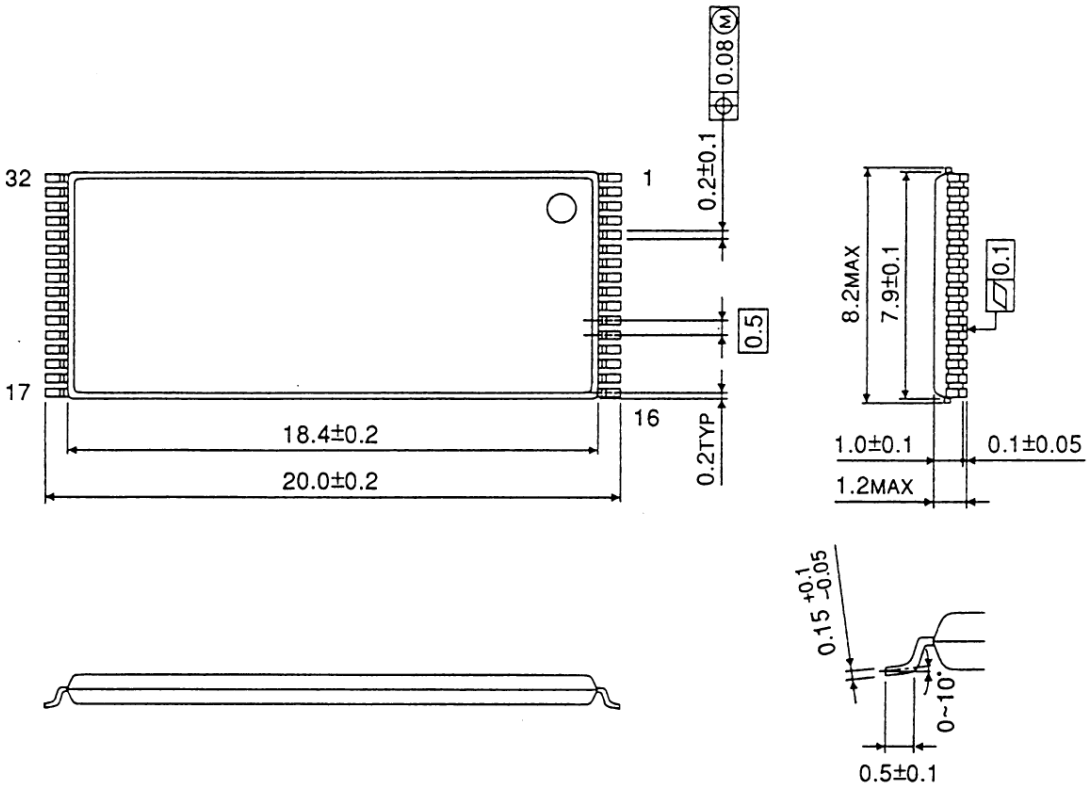


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

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